

## Radiation Hardened Octal D-Type Flip-Flop, Three-State, Positive Edge Triggered

Intersil's Satellite Applications Flow™ (SAF) devices are fully tested and guaranteed to 100kRAD total dose. These QML Class T devices are processed to a standard flow intended to meet the cost and shorter lead-time needs of large volume satellite manufacturers, while maintaining a high level of reliability.

The Intersil HCTS374T is a Radiation Hardened Non-Inverting Octal D-type, Positive Edge Triggered Flip-Flop with three-state outputs. The eight flip-flops enter data into their registers on the LOW-to-HIGH transition of the clock (CP). Data is also transferred to the outputs during this transition. The output enable ( $\overline{OE}$ ) controls the three-state outputs and is independent of the register operation. When the output enable is high, the outputs are in the high impedance state.

## Specifications

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed below must be used when ordering.

**Detailed Electrical Specifications for the HCTS374T are contained in SMD 5962-95748.** A "hot-link" is provided from our website for downloading.

[www.intersil.com/spacedefense/newsafclasst.asp](http://www.intersil.com/spacedefense/newsafclasst.asp)

Intersil's Quality Management Plan (QM Plan), listing all Class T screening operations, is also available on our website.

[www.intersil.com/quality/manuals.asp](http://www.intersil.com/quality/manuals.asp)

## Ordering Information

ORDERING NUMBER	PART NUMBER	TEMP. RANGE (°C)
5962R9574801TRC	HCTS374DTR	-55 to 125
5962R9574801TXC	HCTS374KTR	-55 to 125

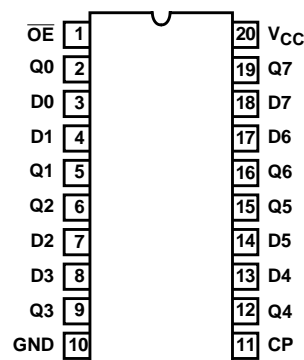
NOTE: **Minimum order quantity for -T is 150 units through distribution, or 450 units direct.**

## Features

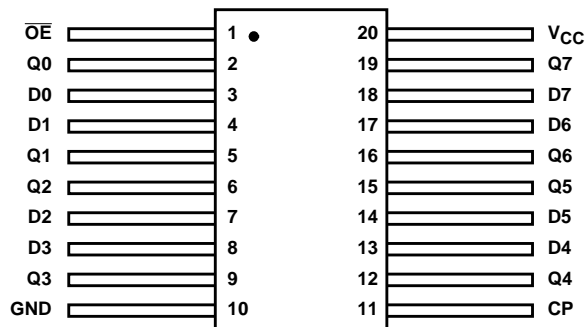
- QML Class T, Per MIL-PRF-38535
- Radiation Performance
  - Gamma Dose ( $\gamma$ )  $1 \times 10^5$  RAD(Si)
  - Latch-Up Free Under Any Conditions
  - SEP Effective LET No Upsets:  $>100$  MEV-cm<sup>2</sup>/mg
  - Single Event Upset (SEU) Immunity  $< 2 \times 10^{-9}$  Errors/Bit-Day (Typ)
- 3 Micron Radiation Hardened SOS CMOS
- Fanout (Over Temperature Range)
  - Bus Driver Outputs - 15 LSTTL Loads
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - $V_{IL} = 0.8V$  Max
  - $V_{IH} = V_{CC}/2$  Min
- Input Current Levels  $I_i \leq 5mA$  at  $V_{OL}$ ,  $V_{OH}$

## Pinouts

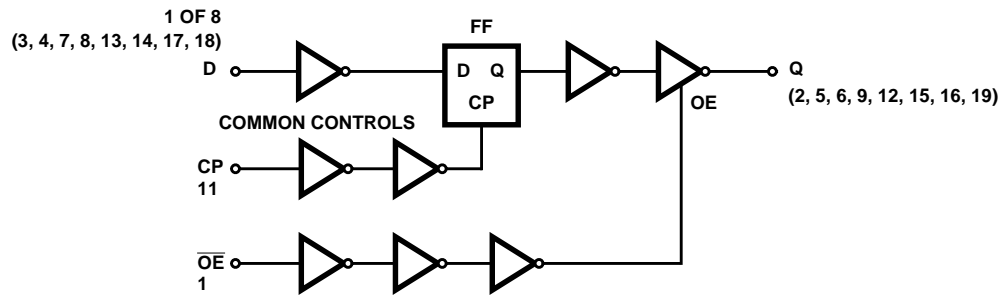
**HCTS374T (SBDIP), CDIP2-T20**  
TOP VIEW





**HCTS374T (FLATPACK), CDFP4-F20**  
TOP VIEW



## Functional Diagram



TRUTH TABLE


INPUTS			OUTPUTS
OE	CP	Dn	Qn
L		H	H
L		L	L
L	L	X	Q0
H	X	X	Z

H =High Level (Steady State).

L =Low Level (Steady State).

X =Immaterial.

Z =High Impedance.

 = Transition from Low to High Level.

Q0 =The level of Q before the indicated input conditions were established.

## Die Characteristics

### DIE DIMENSIONS:

(2743 $\mu$ m x 2692 $\mu$ m x 533 $\mu$ m  $\pm$ 51 $\mu$ m)  
108 x 106 x 21mils  $\pm$ 2mil

### METALLIZATION:

Type: Al Si  
Thickness: 11k $\text{\AA}$   $\pm$ 1k $\text{\AA}$

### SUBSTRATE POTENTIAL:

Unbiased (Silicon on Sapphire)

### BACKSIDE FINISH:

Sapphire

### PASSIVATION:

Type: Silox (SiO<sub>2</sub>)  
Thickness: 13k $\text{\AA}$   $\pm$ 2.6k $\text{\AA}$

### WORST CASE CURRENT DENSITY:

< 2.0e5 A/cm<sup>2</sup>

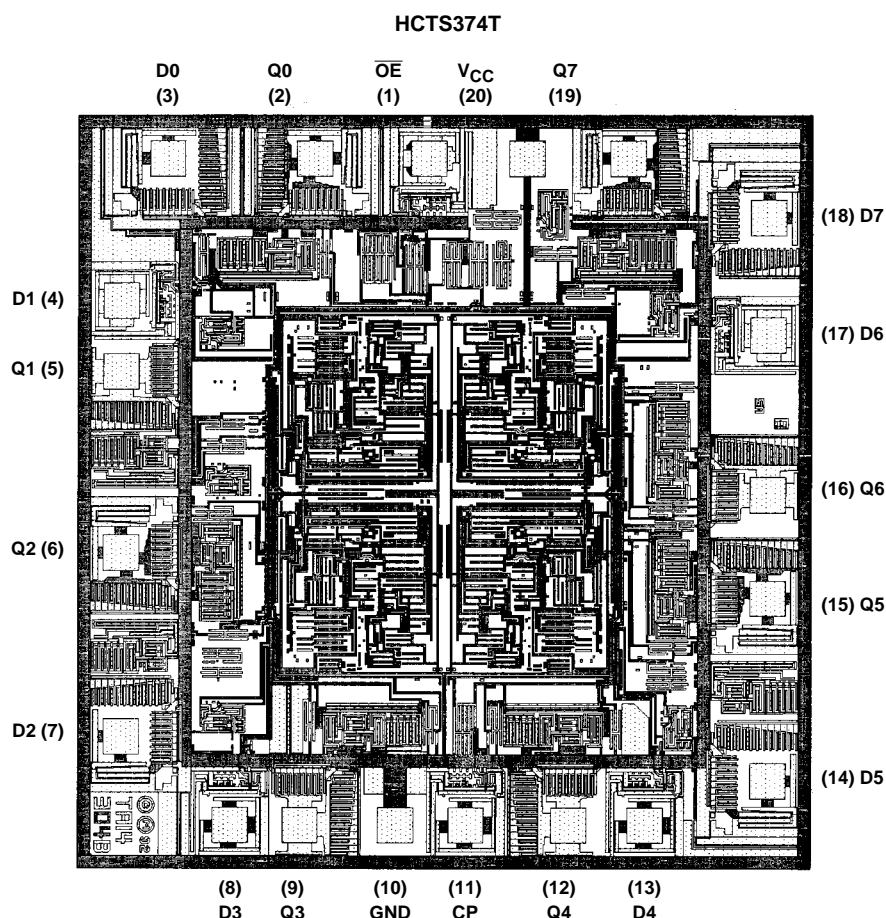
### TRANSISTOR COUNT:

468

### PROCESS:

CMOS SOS

## Metallization Mask Layout



NOTE: The die diagram is a generic plot from a similar HCS device. It is intended to indicate approximate die size and bond pad location. The mask series for the HCTS374 is TA14404A.

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