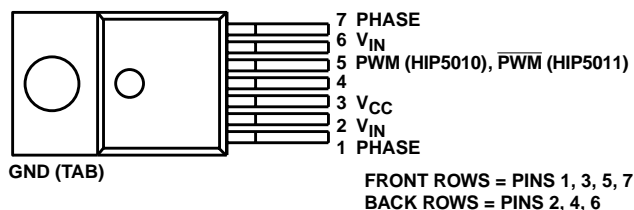


7V, 17A SynchroFET™ Complementary Drive Synchronous Half-Bridge

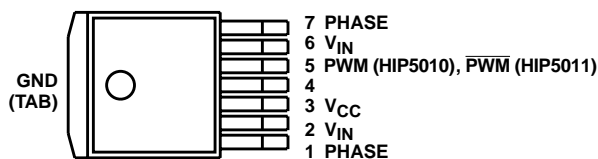
Designed with the P6 and Pentium® in mind, the Intersil SynchroFET™ family provides a new approach for implementing a synchronous rectified buck switching regulator. The SynchroFET replaces two power DMOSs, a Schottky diode, two gate drivers and synchronous control circuitry. The complementary drive circuit turns the upper FET on and the lower FET off when the input from the PWM is high. When the input from the PWM goes low the upper FET turns off and the lower FET turns on. The HIP5011 has a PWM pin that inverts the relationship from the input to PHASE. This architecture allows the designer to utilize a low cost single-ended PWM controller in either a current or voltage mode configuration. The SynchroFET operates in continuous conduction mode reducing EMI constraints and enabling high bandwidth operation. Several features ensure easy start-up. First, the supply currents stay below specification as the supply voltages ramp up; no unexpected surges occur that might perturb a soft-start or deplete a charge-pump. Second, any power-up sequence of the V_{CC} , V_{IN} , or PWM pins can be used without causing large currents. Third, the chip operates when V_{CC} is greater than 2V so V_{CC} can be created from a charge pump powered from V_{IN} .

Pinouts

HIP5010IS1, HIP5011IS1 (SIP - VERTICAL)
TOP VIEW



HIP5010IS, HIP5011IS (SIP - GULLWING)
TOP VIEW



Features

- Complementary Drive, Half-Bridge Power NMOS
- Use With Low-Cost Single-Output PWM Controllers
- Improve Efficiency Over Conventional Buck Converter with Schottky Clamp
- Minimum Deadtime Provided by Adaptive Shoot-Through Protection Eliminates External Schottky
- Grounded Case for Low EMI and Simple Heatsinking
- Low Operating Current
- Frequency Exceeding 1MHz
- Dual Polarity Input Options
- All Pins Surge Protected

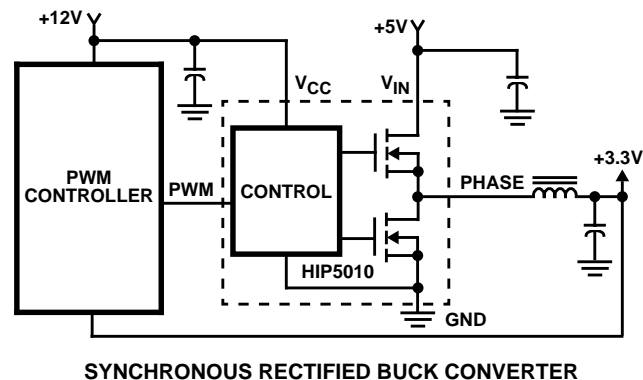
Applications

- 5V to ≤ 3.3 V Synchronous Buck Converters
- Pentium and P6 Power Supplies
- PowerPC™ Power Supplies
- Bus Terminations (BTL and GTL)
- Drive 5V Motors Directly from Microprocessor

Ordering Information

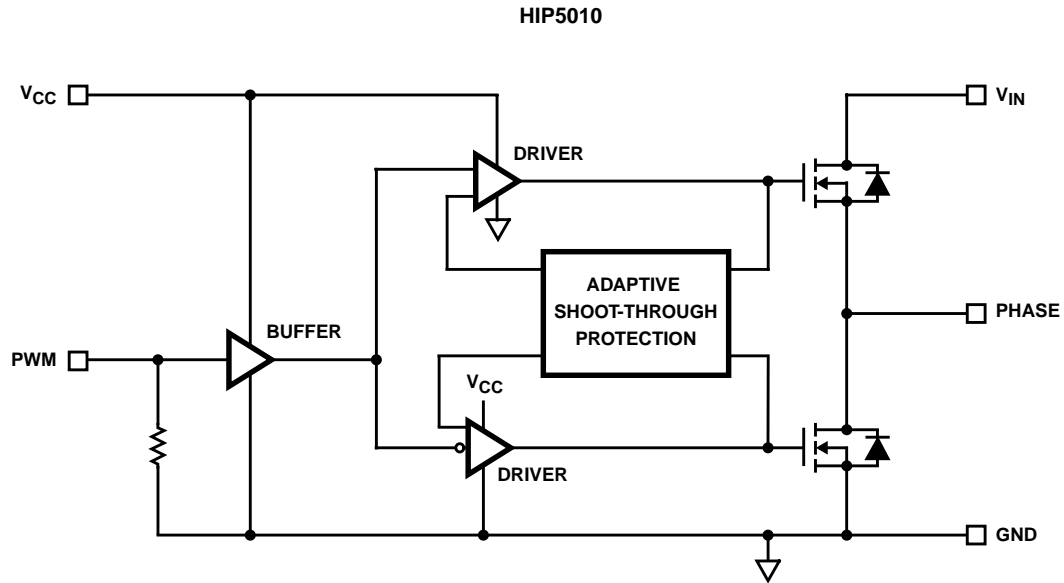
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HIP5010IS	-40 to 85	7 Ld Gullwing SIP	Z7.05B
HIP5010IS1	-40 to 85	7 Ld Staggered Vertical SIP	Z7.05C
HIP5011IS	-40 to 85	7 Ld Gullwing SIP	Z7.05B
HIP5011IS1	-40 to 85	7 Ld Staggered Vertical SIP	Z7.05C

Typical Application Block Diagram

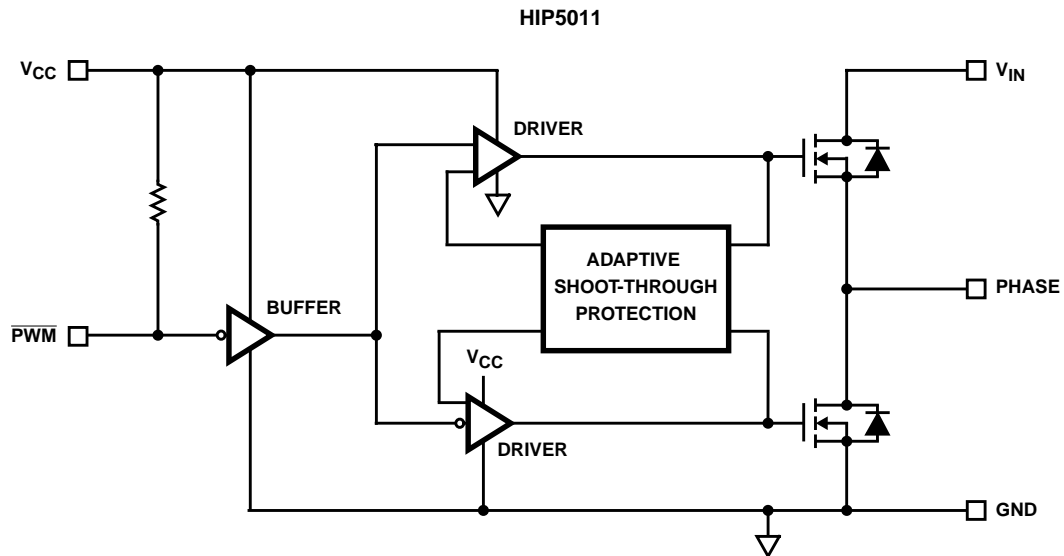


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PowerPC™ is a trademark of International Business Machines.
SynchroFET™ is a trademark of Intersil Corporation.

Non-Inverting SynchroFET Block Diagram



Inverting SynchroFET Block Diagram



HIP5010, HIP5011

Absolute Maximum Ratings

Supply Voltage, V_{CC} +16V
 Input Voltage V_{IN} +7V
 I_{PHASE} , I_{VIN} , I_{GND} ($T_J = 25^{\circ}C$) 17A (Repetitive Peak)
 I_{PHASE} , I_{VIN} , I_{GND} ($T_J = 150^{\circ}C$) 15A (Repetitive Peak)
 PWM Input -4V to +16V
 ESD Classification Class 3 (4kV)
 Lead Temperature (Soldering 10s) (Lead Tips Only) $300^{\circ}C$
 Storage Temperature Range $-65^{\circ}C$ to $150^{\circ}C$
 Junction Temperature Range $-40^{\circ}C$ to $150^{\circ}C$

Operating Conditions

Supply Voltage, V_{CC} +12V, 20%
 Input Voltage V_{IN} 0V to 5.5V
 Supply Voltage, V_{CC} , minimum for charge-pumped start-up +4.0V

Thermal Information (Typical)

Package	$\theta_{JC}^{\dagger\dagger}$ ($^{\circ}C/W$)	θ_{JA} ($^{\circ}C/W$) [†]				
		0	1	2	3	3 ^{†††}
SOIC (IB) ...	26	63	45	42	41	35
SIP (IS)	2	55	30	25	24	18
SIP (IS1)	2	-	-	-	-	-

† Versus additional square inches of 1 ounce copper on the printed circuit board.

†† θ_{JC} is measured to pin 12 for the SOIC. Printed circuit board had 1 square inch of copper. For SIP Packages value shown is typical with an infinite heat sink.

††† 200 linear feet per minute of air flow.

I_{PHASE} - SIPs: 11.5A(RMS), 11.2A(DC); SOIC: 7.4A(RMS), 7.4A(DC)
 I_{VIN} ... SIPs: 10.0A(RMS), 8.5A(DC); SOIC: 6.4A(RMS), 6.4A(DC)
 I_{GND} ... SIPs: 8.5A(RMS), 6.0A(DC); SOIC: 5.4A(RMS), 5.4A(DC)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the recommended operating conditions of this specification is not implied.

Electrical Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	$T_J = 25^{\circ}C$			$T_J = -40^{\circ}C$ $T_J = 150^{\circ}C$		UNITS
			MIN	TYP	MAX	MIN	MAX	
$r_{DS(ON)}$ Upper MOSFET	R_{DSU}	$V_{CC} = 12V$, $V_{IN} = 5V$	-	34	39	-	65	$m\Omega$
$r_{DS(ON)}$ Lower MOSFET	R_{DSL}	$V_{CC} = 12V$, $V_{IN} = 5V$	-	36	42	-	68	$m\Omega$
V_{IN} Operating Current	I_{VINO}	$V_{IN} = 5V$, No Load, 500kHz	-	5	8	-	10	mA
V_{IN} Quiescent Current	I_{VIN}	PWM or $\overline{PWM} = V_{CC}$ or GND	-	0.1	10	-	100	μA
V_{CC} Operating Current	I_{CCO}	$V_{CC} = 12V$, 500kHz	-	8	12	-	15	mA
V_{CC} Quiescent Current (HIP5010)	I_{CCIH}	PWM = V_{CC}	-	80	-	-	400	μA
V_{CC} Quiescent Current (HIP5010)	I_{CCIL}	PWM = GND	-	0.1	10	-	100	μA
V_{CC} Quiescent Current (HIP5011)	I_{CCNIH}	$\overline{PWM} = V_{CC}$	-	0.1	10	-	100	μA
V_{CC} Quiescent Current (HIP5011)	I_{CCNIL}	$\overline{PWM} = GND$	-	140	-	-	400	μA
Low Level PWM Input Voltage	V_{IL}		-	1.8	-	1	-	V
High Level PWM Input Voltage	V_{IH}		-	2.1	-	-	3	V
PWM Input Voltage Hysteresis	V_{IHYS}		-	0.3	-	-	-	V
Input Pulldown Resistance (HIP5010)	R_{PWM}		-	220	-	100	400	$k\Omega$
Input Pullup Resistance (HIP5011)	R_{PWM}		-	220	-	100	400	$k\Omega$

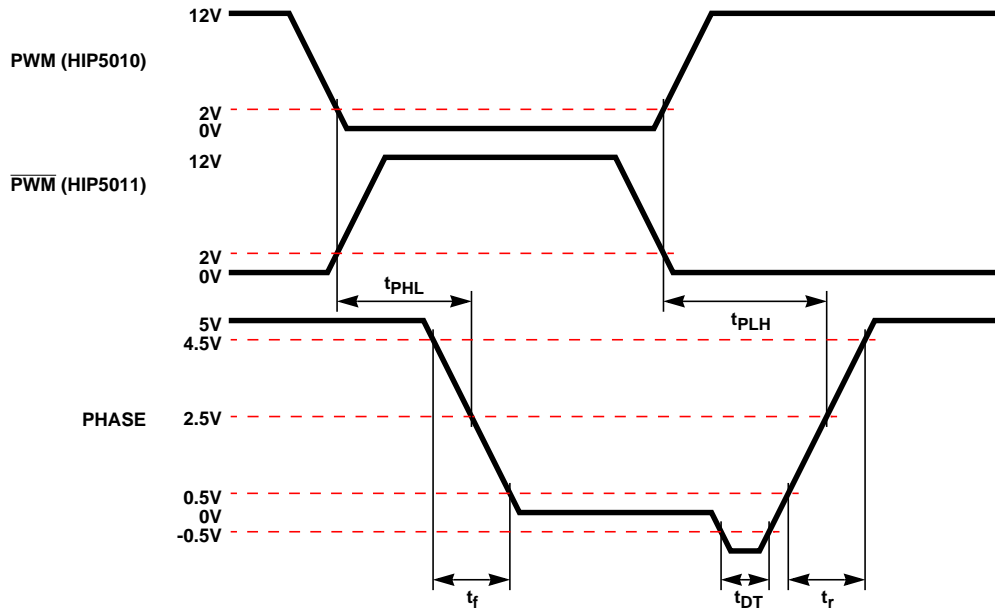
Switching Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	$T_J = 25^{\circ}C$			$T_J = -40^{\circ}C$ $T_J = 150^{\circ}C$		UNITS
			MIN	TYP	MAX	MIN	MAX	
Upper Device Turn-Off Delay	t_{PHL}	$V_{CC} = 12V$, $I_{PHASE} = -1A$	-	30	50	-	80	ns
Lower Device Turn-Off Delay	t_{PLH}	$V_{CC} = 12V$, $I_{PHASE} = +1A$	-	30	50	-	80	ns
Dead Time	t_{DT}	$V_{CC} = +12V$, $I_{PHASE} = -1A$	-	10	-	-	-	ns
Phase Rise-Time	t_r	$V_{CC} = 12V$, $I_{PHASE} = -1A$	-	20	-	-	-	ns
Phase Fall-Time	t_f	$V_{CC} = 12V$, $I_{PHASE} = +1A$	-	20	-	-	-	ns

Pin Descriptions

SYMBOL	DESCRIPTION
V_{CC}	Positive supply to control logic and gate drivers. De-couple this pin to GND.
V_{IN}	FET Switch Input Voltage. De-couple this pin to GND. Tie all V_{IN} terminals together.
PHASE	Output. Tie all phase terminals together.
PWM (HIP5010) PWM (HIP5011)	Single Ended Control Input. This input connects to the PWM controller output.
GND	System Ground.

Timing Diagram



NOTE: $I_{PHASE} = +1A$ for t_{PLH} and t_f , $I_{PHASE} = -1A$ for t_{PHL} , t_{DT} , and t_r .

FIGURE 1.

Typical Performance Curves

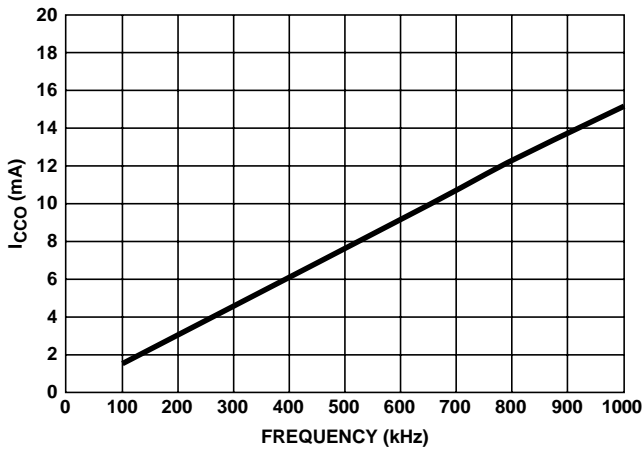


FIGURE 2. I_{CCO} vs FREQUENCY

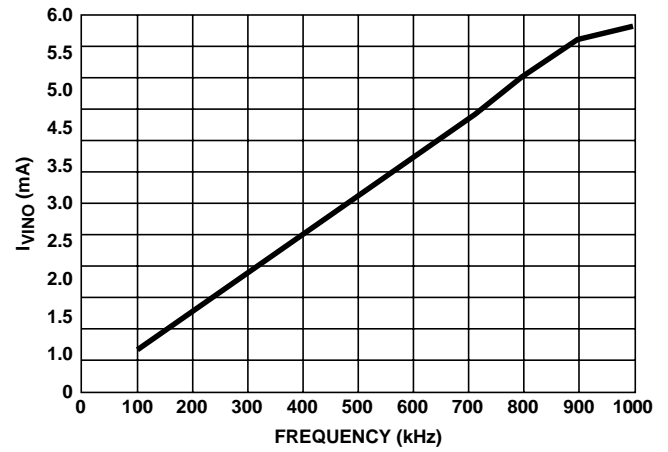


FIGURE 3. I_{VINO} vs FREQUENCY

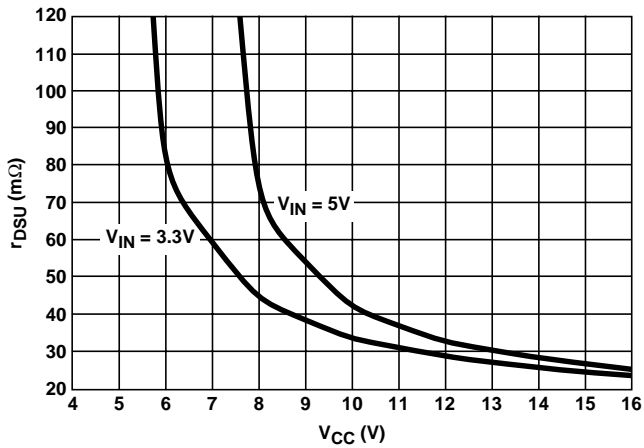


FIGURE 4. R_{DSU} vs V_{CC}

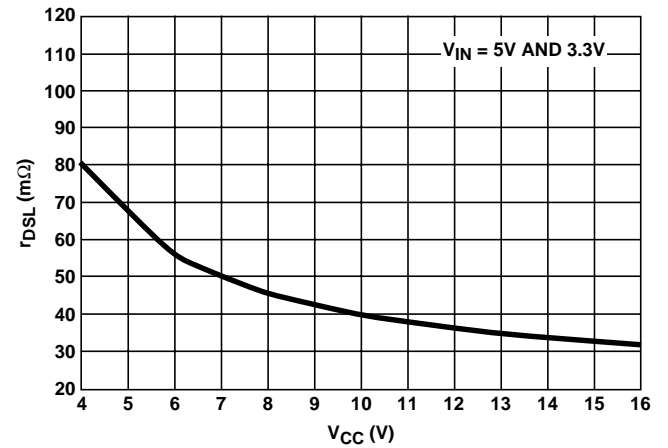


FIGURE 5. R_{DSL} vs V_{CC}

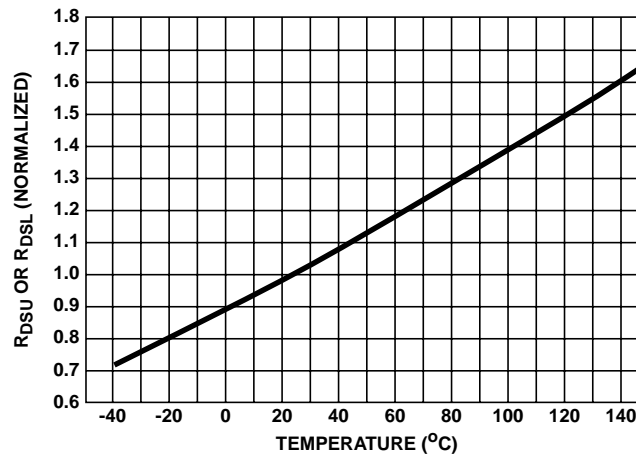


FIGURE 6. R_{DSU} OR R_{DSL} vs TEMPERATURE

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Sales Office Headquarters

NORTH AMERICA

Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

EUROPE

Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA

Intersil (Taiwan) Ltd.
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029