

## **-10A, -150V, 0.500 Ohm, P-Channel Power MOSFET**

This P-Channel enhancement mode silicon gate power field effect transistor is designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA9404.

### **Ordering Information**

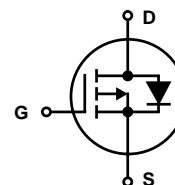
PART NUMBER	PACKAGE	BRAND
RFP10P15	TO-220AB	RFP10P15

NOTE: When ordering, include the entire part number.

### **Features**

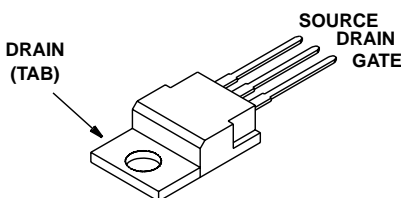
- -10A, -150V
- $r_{DS(ON)} = 0.500\Omega$
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- Related Literature
  - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

### **Symbol**



### **Packaging**

**TO-220AB**



**Absolute Maximum Ratings**  $T_C = 25^{\circ}\text{C}$ , Unless Otherwise Specified

	RFP10P15	UNITS
Drain to Source Voltage (Note 1) . . . . .	$V_{DS}$ -150	V
Drain to Gate Voltage ( $R_{GS} = 20\text{K}\Omega$ (Note 1) . . . . .	$V_{DGR}$ -150	V
Continuous Drain Current . . . . .	$I_D$ 10	A
Pulsed Drain Current (Note 3) . . . . .	$I_{DM}$ 30	A
Gate to Source Voltage . . . . .	$V_{GS}$ $\pm 20$	V
Maximum Power Dissipation . . . . .	$P_D$ 75	W
Linear Derating Factor . . . . .	0.6	W/ $^{\circ}\text{C}$
Operating and Storage Temperature . . . . .	$T_J, T_{STG}$ -55 to 150	$^{\circ}\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s . . . . .	$T_L$ 300	$^{\circ}\text{C}$
Package Body for 10s, See Techbrief 334 (for TO-220) . . . . .	$T_{pkg}$ 260	$^{\circ}\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

## NOTE:

1.  $T_J = 25^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ .

**Electrical Specifications**  $T_C = 25^{\circ}\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	$BV_{DSS}$	$I_D = 250\mu\text{A}$ , $V_{GS} = 0$	-150	-	-	V
Gate to Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$ , $I_D = 250\mu\text{A}$	-2	-	-4	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = \text{Rated } BV_{DSS}$ , $V_{GS} = 0\text{V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 0.8 \times \text{Rated } BV_{DSS}$ , $V_{GS} = 0\text{V}$ , $T_C = 125^{\circ}\text{C}$	-	-	25	$\mu\text{A}$
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20\text{V}$ , $V_{DS} = 0$	-	-	$\pm 100$	nA
Drain to Source On Voltage (Note 2)	$V_{DS(ON)}$	$I_D = 10\text{A}$ , $V_{GS} = -10\text{V}$	-	-	-5.0	V
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$I_D = 10\text{A}$ , $V_{GS} = -10\text{V}$ , (Figures 6, 7)	-	-	0.500	$\Omega$
Turn-On Delay Time	$t_{d(ON)}$	$I_D \approx 10\text{A}$ , $V_{DS} = -75\text{V}$ , $R_G = 50\Omega$ $R_L = 7.5\Omega$ , $V_{GS} = -10\text{V}$ (Figures 10, 11, 12)	-	24	50	ns
Rise Time	$t_r$		-	74	150	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	138	225	ns
Fall Time	$t_f$		-	61	100	ns
Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{V}$ , $V_{DS} = -25\text{V}$ $f = 1\text{MHz}$ (Figure 9)	-	-	1700	pF
Output Capacitance	$C_{OSS}$		-	-	600	pF
Reverse Transfer Capacitance	$C_{RSS}$		-	-	350	pF
Thermal Resistance, Junction to Case	$R_{\theta JC}$	RFM10P12, RFM10P15	-	-	1.25	$^{\circ}\text{C/W}$
		RFP10P12, RFP10P15			1.67	$^{\circ}\text{C/W}$

**Source to Drain Diode Specifications**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	$V_{SD}$	$I_{SD} = -10\text{A}$	-	-	1.4	V
Reverse Recovery Time	$t_{rr}$	$I_{SD} = -10\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	210	-	ns

## NOTES:

2. Pulsed: Pulse Duration = 300 $\mu\text{s}$  Max, Duty Cycle  $\leq 2\%$ .
3. Repetitive rating: pulse width limited by maximum junction temperature.

## Typical Performance Curves

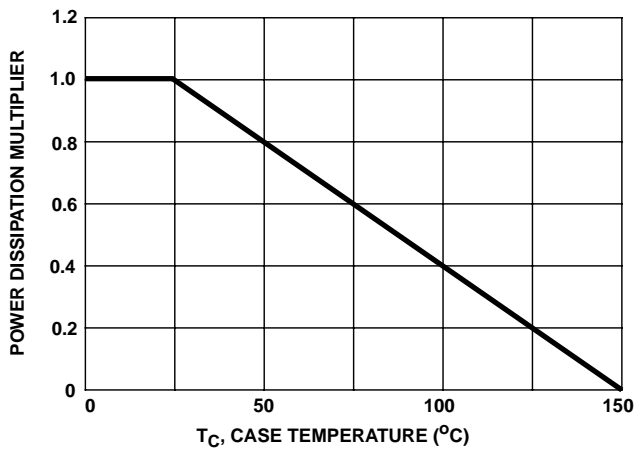


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

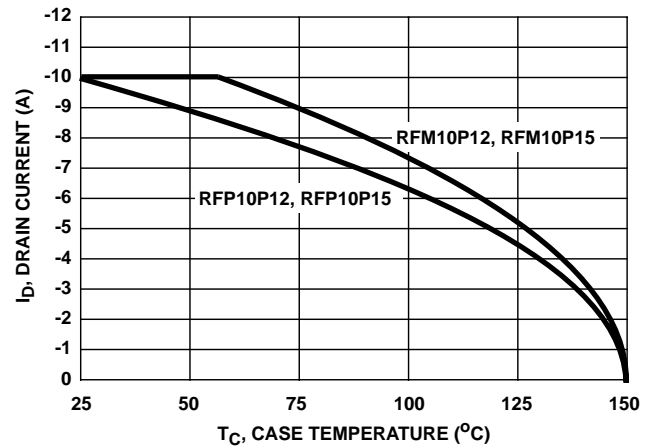


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

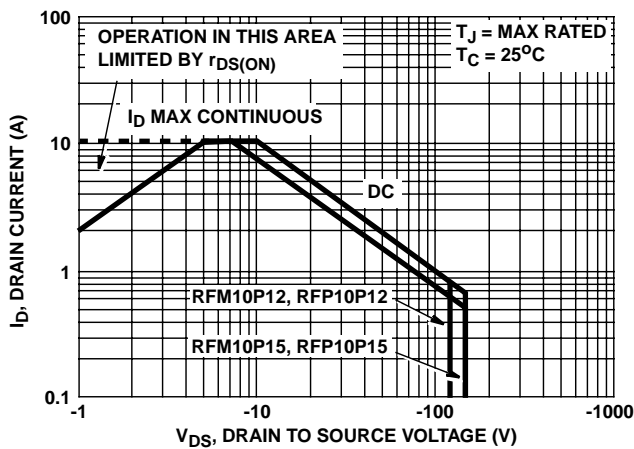


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

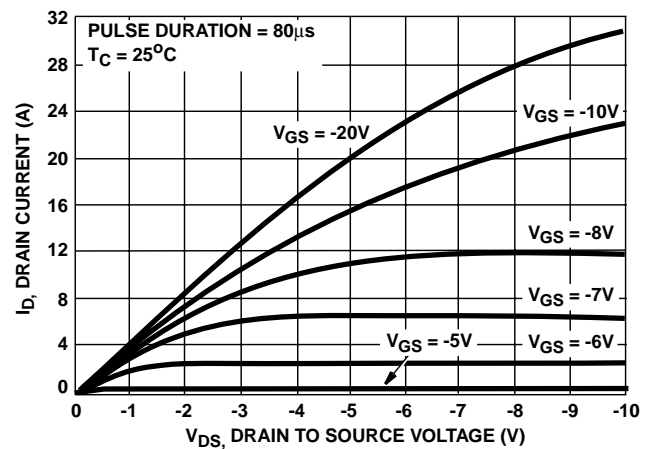


FIGURE 4. SATURATION CHARACTERISTICS

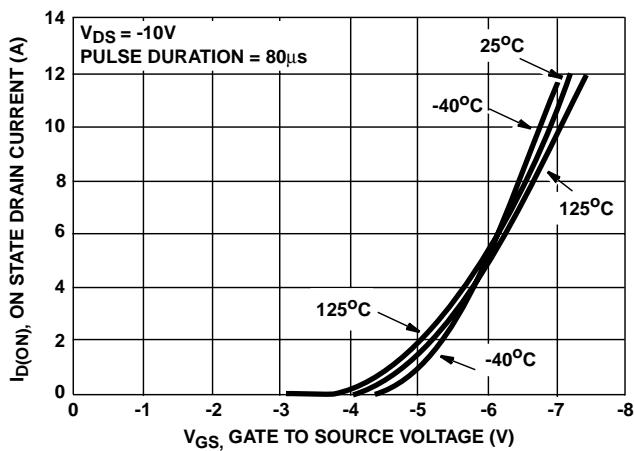


FIGURE 5. TRANSFER CHARACTERISTICS

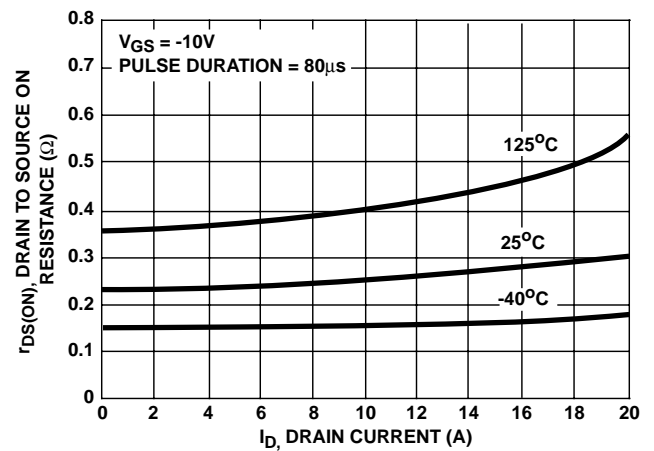


FIGURE 6. DRAIN TO SOURCE ON RESISTANCE vs DRAIN CURRENT

## Typical Performance Curves (Continued)

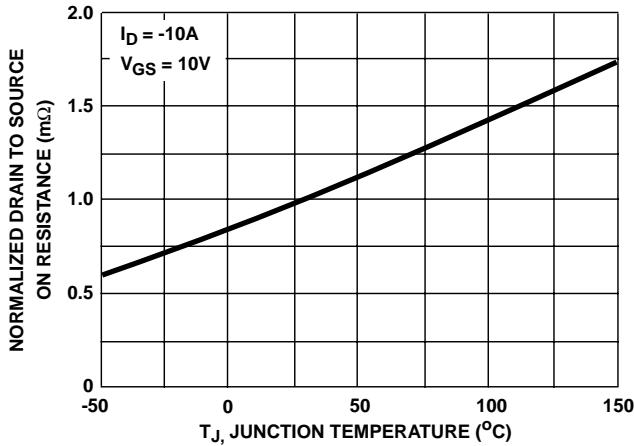


FIGURE 7. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

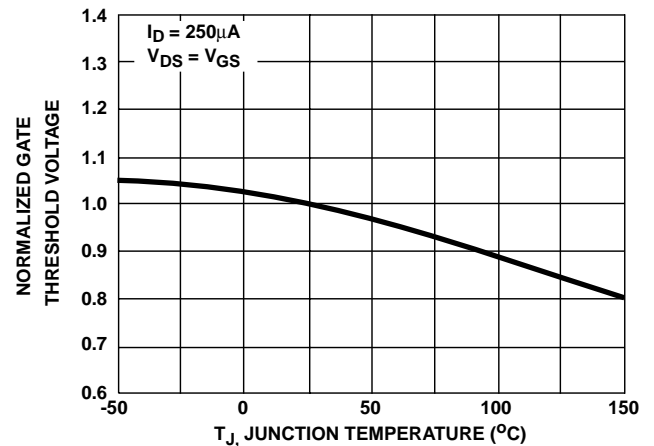


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

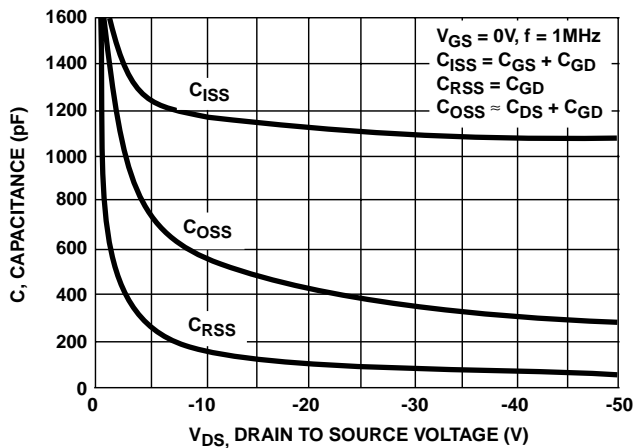
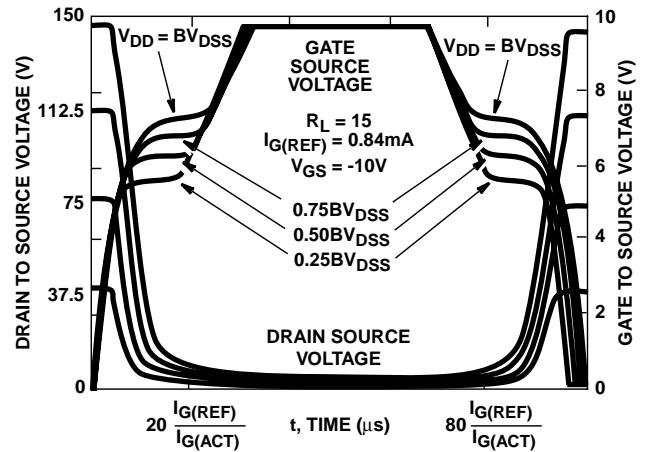


FIGURE 9. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Applications Notes AN7254 and AN7260

FIGURE 10. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

## Test Circuits and Waveforms

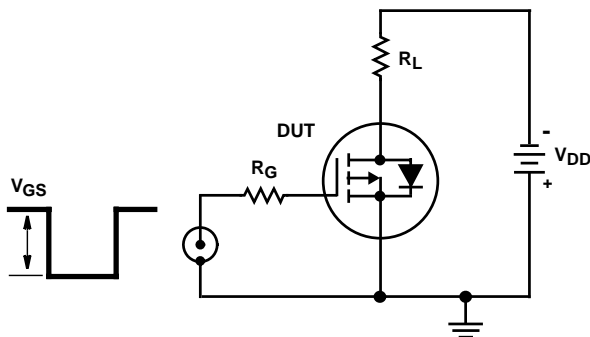


FIGURE 11. SWITCHING TIME TEST CIRCUIT

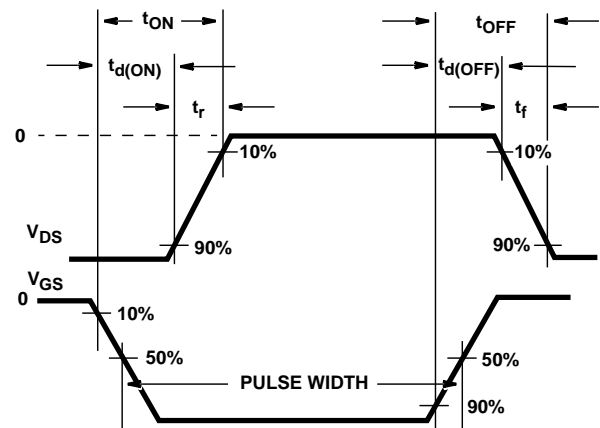


FIGURE 12. RESISTIVE SWITCHING WAVEFORMS

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