International
IOR Rectifier

Data Sheet No. PD-6.076

IR02H420

HIGH VOLTAGE HALF-BRIDGE

Features

- Output Power MOSFETs in half-bridge configuration
- 500V Rated Breakdown Voltage
- High side gate drive designed for bootstrap operation
- Matched propagation delay for both channels
- Independent high and low side output channels
- Undervoltage lockout
- 5V Schmitt-triggered input logic
- Half-Bridge output out of phase with $\overline{HIN}$

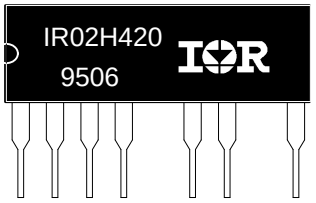
Description

The IR02H420 is a high voltage, high speed half bridge. Proprietary HVIC and latch immune CMOS technologies, along with the HEXFET® power MOSFET technology, enable ruggedized single package construction. The logic inputs are compatible with standard CMOS or LSTTL outputs. The front end features an independent high and low side driver in phase with the logic compatible input signals. The output features two HEXFETs in a half-bridge configuration with a high pulse current buffer stage designed for minimum cross-conduction in the half-bridge. Propagation delays for the high and low side power MOSFETs are matched to simplify use. The device can operate up to 500 volts.

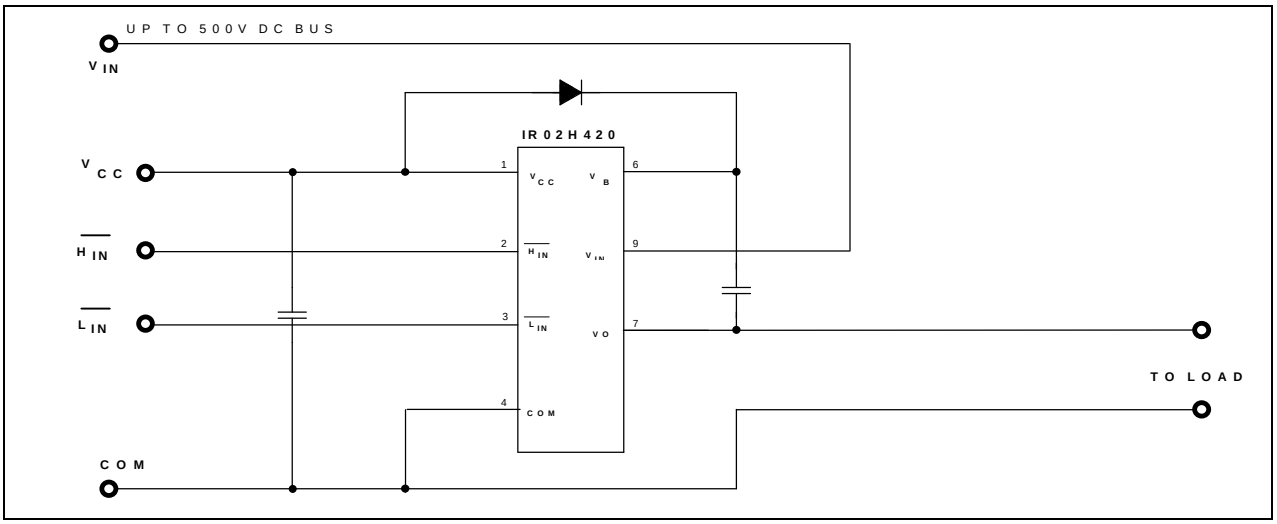
Product Summary

V_{IN} (max)	500V
$t_{on/off}$	130 ns
t_{rr}	270 ns
$R_{DS(on)}$	3.0Ω
P_D (T_A = 25 °C)	2.0W

Package



Typical Connection



Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Parameter Definition	Min.	Max.	Units
V_{IN}	High Voltage Supply	-0.3	500	V
V_B	High Side Floating Supply Absolute Voltage	-0.3	525	
VO	Half-Bridge Output Voltage	-0.3	V_{IN} + 0.3	
V_{IH}/V_{IL}	Logic Input Voltage ($\overline{HIN}$ & $\overline{LIN}$)	-0.3	V_{CC} + 0.3	
V_{CC}	Low Side and Logic Fixed Supply Voltage	-0.3	25	
dv/dt	Peak Diode Recovery dv/dt	---	3.5	V/ns
P_D	Package Power Dissipation @ $T_A \leq +25^oC$	---	2.00	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	---	60	$^oC/W$
T_J	Junction Temperature	-55	150	^oC
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	---	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions.

Symbol	Parameter Definition	Min.	Max.	Units
V_B	High Side Floating Supply Absolute Voltage	VO + 10	VO + 20	V
V_{IN}	High Voltage Supply	---	500	
VO	Half-Bridge Output Voltage	(note 1)	500	
V_{CC}	Low Side and Logic Fixed Supply Voltage	10	20	
V_{IH}/V_{IL}	Logic Input Voltage ($\overline{HIN}$ & $\overline{LIN}$)	0	V_{CC}	
I_D	Continuous Drain Current ($T_A = 25^oC$)	---	0.7	A
	($T_A = 85^oC$)	---	0.5	
T_A	Ambient Temperature	-40	125	^oC

Note 1: Logic operational for VO of -5 to 500 V. Logic state held for VO of -5 to - V_B.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_B) = 15V and T_A = 25ºC unless otherwise specified. Switching time waveform definitions are shown in figure 2.

Symbol	Parameter Definition	T_A = 25ºC Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-On Propagation Delay (see note 2)	---	130	200	ns	V_S = 0 V
t_{off}	Turn-Off Propagation Delay (see note 2)	---	90	200		V_S = 500 V
t_r	Turn-On Rise Time (see note 2)	---	80	120		
t_f	Turn-Off Fall Time (see note 2)	---	40	70		
MT	Delay Matching, HS & LS Turn-On/Off	---	30	---		
t_{rr}	Reverse Recovery Time (MOSFET Body Diode)	---	260	---		I_F = 0.7 A
Q_{rr}	Reverse Recovery Charge (MOSFET Body Diode)	---	0.7	---	µC	di/dt = 100A/µs

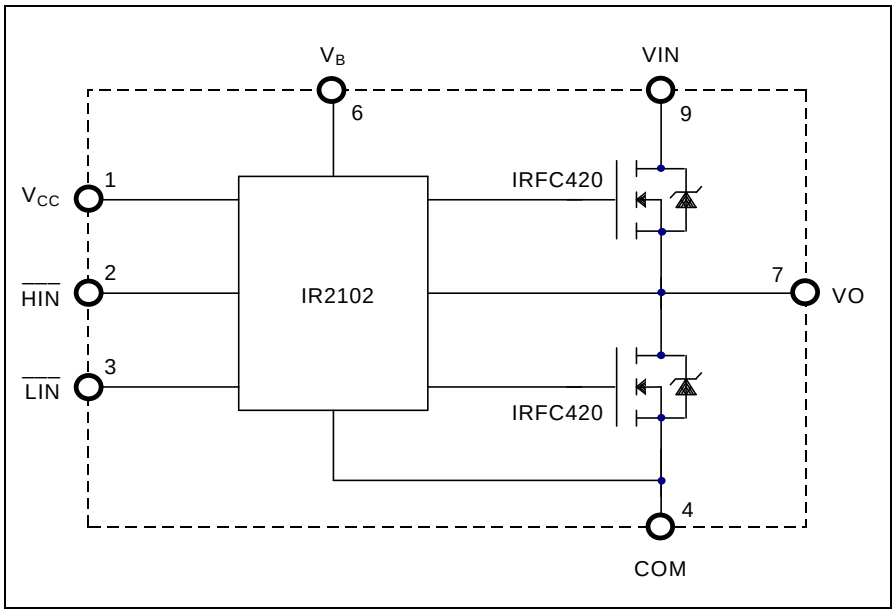
Note 2: Switching times as specified and illustrated in figure 2 are referenced to the MOSFET gate input voltage. This is shown as HO in figure 2.

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_B) = 15V and T_A = 25ºC unless otherwise specified. The Input voltage and current levels are referenced to COM.

Symbol	Parameter Definition	T_A = 25ºC Min.	Typ.	Max.	Units	Test Conditions
Supply Characteristics						
V_{CCUV+}	V_{CC} Supply Undervoltage Positive Going Threshold	8.8	9.3	9.8	V	
V_{CCUV-}	V_{CC} Supply Undervoltage Negative Going Threshold	7.5	8.2	8.6		
I_{QCC}	Quiescent V_{CC} Supply Current	---	140	240	µA	
I_{QBS}	Quiescent V_{BS} Supply Current	---	20	50		
I_{OS}	Offset Supply Leakage Current	---	---	50		V_B = V_S = 500V
Input Characteristics						
V_{IH}	Logic “1” Input Voltage	2.7	---	---	V	V_{CC} = 10V to 20V
V_{IL}	Logic “0” Input Voltage	---	---	0.8		
I_{IN+}	Logic “1” Input Bias Current	---	20	40	µA	
I_{IN-}	Logic “0” Input Bias Current	---	---	1.0	µA	
Output Characteristics						
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	---	3.0	---	Ω	I_D = 700mA
V_{SD}	Diode Forward Voltage	---	0.8	---	V	T_j = 150 ºC

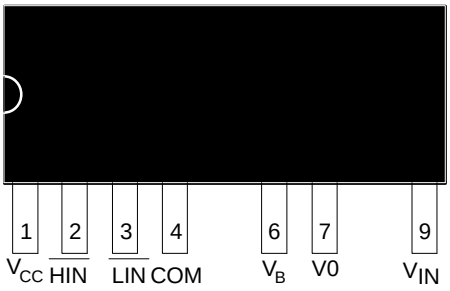
Functional Block Diagram



Lead Definitions

Symbol	Lead Description
V_{CC}	Logic and internal gate drive supply voltage.
$\overline{HIN}$	Logic input for high side Half Bridge output, out of phase
$\overline{LIN}$	Logic input for low side Half Bridge output, in phase
V_B	High side gate drive floating supply. For bootstrap operation a high voltage fast recovery diode is needed to feed from V_{CC} to V_B.
V_{IN}	High voltage supply.
VO	Half-Bridge output.
COM	Logic and low side of Half-Bridge return.

Lead Assignments



9 Lead SIP w/o Leads 5 & 8

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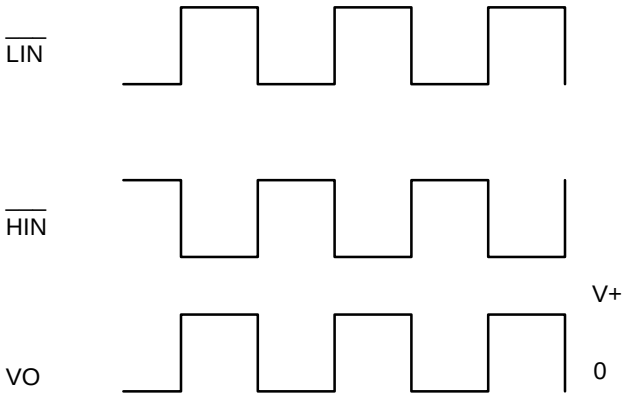

Figure 1. Input/Output Timing Diagram

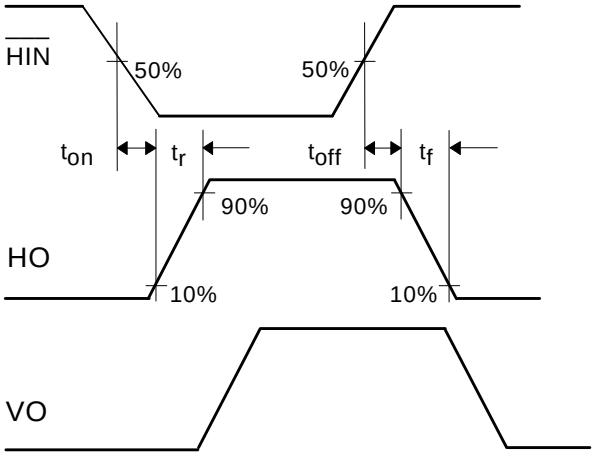

Figure 2. Switching Time Waveform Definitions

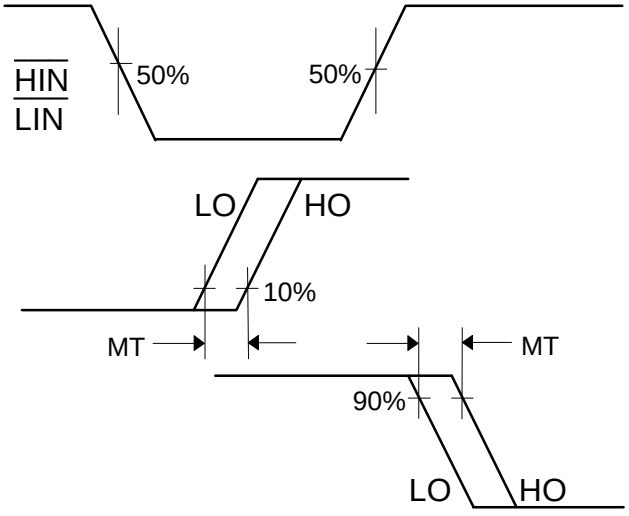

Figure 3. Delay Matching Waveform Definitions

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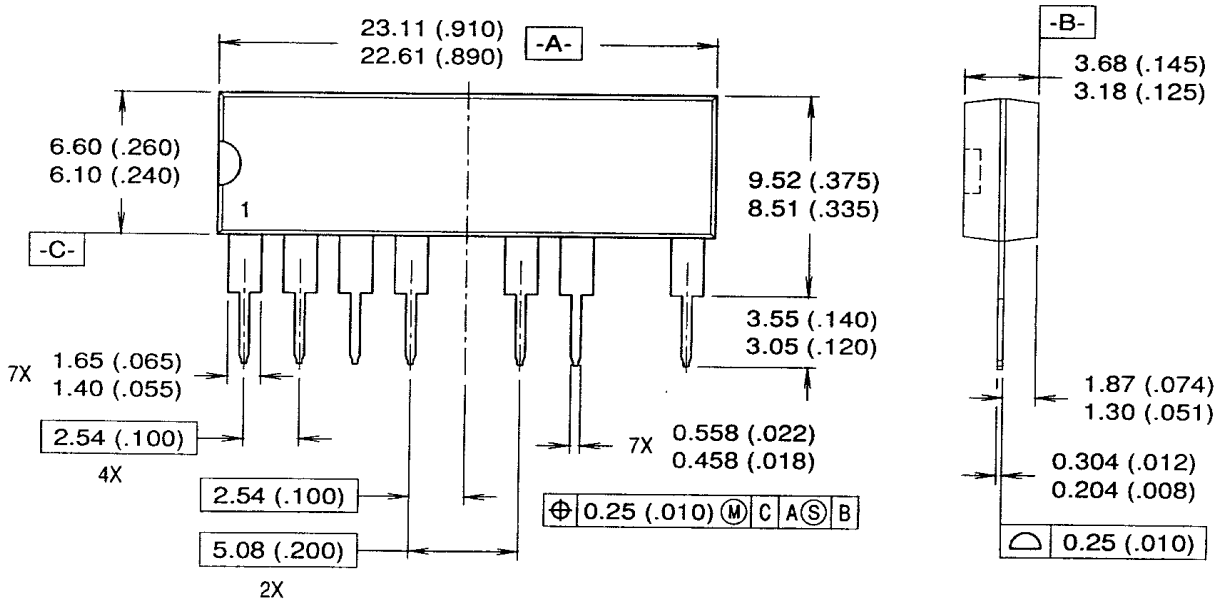

NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).

Package Outline

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EUROPEAN HEADQUARTERS: HURST GREEN, OXTED, SURREY RH8 9BB, UK • (44)0883 713215 • FAX (944)0883 714234 • TELEX 95219

Sales Offices, Agents and Distributors in Major Cities Throughout the World.

Data and specifications subject to change without notice.

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