

IR2010(S) & (PbF)

HIGH AND LOW SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
Fully operational to 200V
Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 3.3V logic compatible
Separate logic supply range from 3.3V to 20V
Logic and power ground $\pm 5V$ offset
- CMOS Schmitt-triggered inputs with pull-down
- Shut down input turns off both channels
- Matched propagation delay for both channels
- Outputs in phase with inputs
- Also available LEAD-FREE

Product Summary

V_{OFFSET}	200V max.
$I_{\text{O+/-}}$	3.0A / 3.0A typ.
V_{OUT}	10 - 20V
$t_{\text{on/off}}$	95 & 65 ns typ.
Delay Matching	15 ns max.

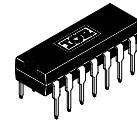
Applications

- Audio Class D amplifiers
- High power DC-DC SMPS converters
- Other high frequency applications

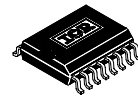
Description

The IR2010 is a high power, high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels, ideal for Audio Class D and DC-DC converter applications. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.0V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 200 volts. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction.

Packages

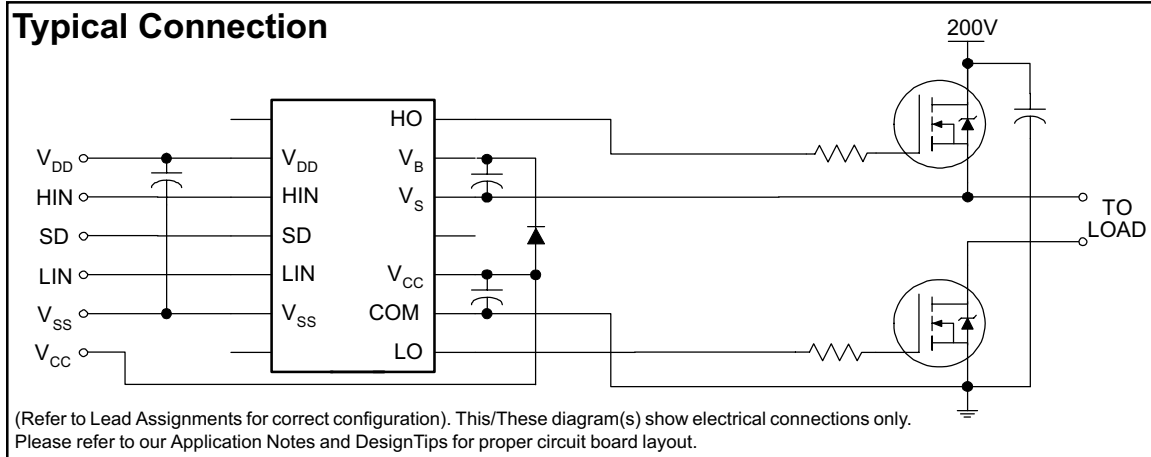


14-Lead PDIP



16-Lead SOIC

Typical Connection



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Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V _B	High side floating supply voltage	-0.3	225	V
V _S	High side floating supply offset voltage	V _B - 25	V _B + 0.3	
V _{HO}	High side floating output voltage	V _S - 0.3	V _B + 0.3	
V _{CC}	Low side fixed supply voltage	-0.3	25	
V _{LO}	Low side output voltage	-0.3	V _{CC} + 0.3	
V _{DD}	Logic supply voltage	-0.3	V _{SS} + 25	
V _{SS}	Logic supply offset voltage	V _{CC} - 25	V _{CC} + 0.3	
V _{IN}	Logic input voltage (HIN, LIN & SD)	V _{SS} - 0.3	V _{DD} + 0.3	
dV _S /dt	Allowable offset supply voltage transient (figure 2)	—	50	V/ns
P _D	Package power dissipation @ T _A ≤ +25°C (14 lead DIP)	—	1.6	W
	(16 lead SOIC)	—	1.25	
R _{THJA}	Thermal resistance, junction to ambient (14 lead DIP)	—	75	°C/W
	(16 lead SOIC)	—	100	
T _J	Junction temperature	—	150	°C
T _S	Storage temperature	-55	150	
T _L	Lead temperature (soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset ratings are tested with all supplies biased at 15V differential. Typical ratings at other bias conditions are shown in figures 24 and 25.

Symbol	Definition	Min.	Max.	Units
V _B	High side floating supply absolute voltage	V _S + 10	V _S + 20	V
V _S	High side floating supply offset voltage	Note 1	200	
V _{HO}	High side floating output voltage	V _S	V _B	
V _{CC}	Low side fixed supply voltage	10	20	
V _{LO}	Low side output voltage	0	V _{CC}	
V _{DD}	Logic supply voltage	V _{SS} + 3	V _{SS} + 20	
V _{SS}	Logic supply offset voltage	-5 (Note 2)	5	
V _{IN}	Logic input voltage (HIN, LIN & SD)	V _{SS}	V _{DD}	
T _A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of -4 to +200V. Logic state held for V_S of -4V to -V_{BS}.

Note 2: When V_{DD} < 5V, the minimum V_{SS} offset is limited to -V_{DD}.

(Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS} , V_{DD}) = 15V, C_L = 1000 pF, T_A = 25°C and V_{SS} = COM unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	7	50	95	135	ns	$V_S = 0V$
t_{off}	Turn-off propagation delay	8	30	65	105		$V_S = 200V$
t_{sd}	Shutdown propagation delay	9	35	70	105		$V_S = 200V$
t_r	Turn-on rise time	10	—	10	20		
t_f	Turn-off fall time	11	—	15	25		
MT	Delay matching, HS & LS turn-on/off	6	—	—	15		

Static Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS} , V_{DD}) = 15V, T_A = 25°C and V_{SS} = COM unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input leads: HIN, LIN and SD. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage	12	9.5	—	—	V	$V_{DD} = 15V$
V_{IL}	Logic "0" input voltage	13	—	—	6.0		
V_{IH}	Logic "1" input voltage	12	2	—	—		$V_{DD} = 3.3V$
V_{IL}	Logic "0" input voltage	13	—	—	1		
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	14	—	—	1.0		$I_O = 0A$
V_{OL}	Low level output voltage, V_O	15	—	—	0.1		$I_O = 0A$
I_{LK}	Offset supply leakage current	16	—	—	50	μA	$V_B = V_S = 200V$
I_{QBS}	Quiescent V_{BS} supply current	17	—	70	210		$V_{IN} = 0V$ or V_{DD}
I_{QCC}	Quiescent V_{CC} supply current	18	—	100	230		$V_{IN} = 0V$ or V_{DD}
I_{QDD}	Quiescent V_{DD} supply current	19	—	1	5		$V_{IN} = 0V$ or V_{DD}
I_{IN+}	Logic "1" input bias current	20	—	20	40		$V_{IN} = V_{DD}$
I_{IN-}	Logic "0" input bias current	21	—	—	1.0		$V_{IN} = 0V$
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	22	7.5	8.6	9.7	V	
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	23	7.0	8.2	9.4		
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	24	7.5	8.6	9.7		
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	25	7.0	8.2	9.4		
I_{O+}	Output high short circuit pulsed current	26	2.5	3.0	—	A	$V_O = 0V$, $V_{IN} = V_{DD}$ $PW \leq 10 \mu s$
I_{O-}	Output low short circuit pulsed current	27	2.5	3.0	—		$V_O = 15V$, $V_{IN} = 0V$ $PW \leq 10 \mu s$

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The schematic diagram illustrates a 3-bit digital-to-analog converter (DAC) circuit. The circuit is enclosed in a dashed box, indicating it is a single integrated circuit. The inputs are three digital signals: V_{DD} , V_{SS} , and V_{COM} . The outputs are three analog signals: V_B , V_S , and V_{CC} . The circuit consists of several key components:

- Input Stage:** Three input signals (V_{DD} , V_{SS} , and V_{COM}) are each connected to a resistor and a buffer (represented by a triangle with a circle). The outputs of these buffers are connected to three 3-bit digital-to-analog converter (DAC) cores.
- 3-bit DAC Cores:** Each core is a rectangular block with three inputs labeled V_{SS}/COM , V_{SS} , and V_{COM} . The outputs of these cores are connected to the V_{SS}/COM and V_{SS} inputs of a larger 3-bit DAC core.
- 3-bit DAC Core:** This is a large rectangular block with three inputs labeled V_{SS}/COM , V_{SS} , and V_{COM} . It has three outputs labeled V_B , V_S , and V_{CC} .
- Output Stage:** The outputs of the 3-bit DAC core are connected to three output buffers (represented by triangles with circles). The outputs of these buffers are connected to the V_{SS}/COM and V_{SS} inputs of a larger 3-bit DAC core.
- UV DETECT and DELAY:** Two blocks labeled "UV DETECT" and "DELAY" are connected to the V_{SS}/COM and V_{SS} inputs of the 3-bit DAC core. The "UV DETECT" block has an output labeled Q that is connected to the V_{SS}/COM input. The "DELAY" block has an output labeled Q that is connected to the V_{SS} input.

Symbol	Description
V _{DD}	Logic supply
HIN	Logic input for high side gate driver output (HO), in phase
SD	Logic input for shutdown
LIN	Logic input for low side gate driver output (LO), in phase
V _{SS}	Logic ground
V _B	High side floating supply
HO	High side gate drive output
V _S	High side floating supply return
V _{CC}	Low side supply
LO	Low side gate drive output
COM	Low side return

IR2010 Pin Configuration (14 Lead PDIP):

Pin	Function	Pin	Function
8	HO	7	
9	VDD	6	VB
10	HIN	5	VS
11	SD	4	
12	LIN	3	VCC
13	VSS	2	COM
14	LO	1	

IR2010S Pin Configuration (16 Lead SOIC (Wide Body)):

Pin	Function	Pin	Function
9	HO	8	
10		7	VB
11	VDD	6	VS
12	HIN		
13	SD		
14	LIN	3	VCC
15	VSS	2	COM
16	LO	1	

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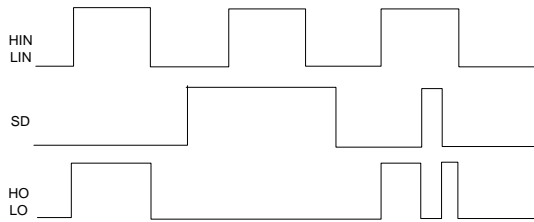


Figure 1. Input/Output Timing Diagram

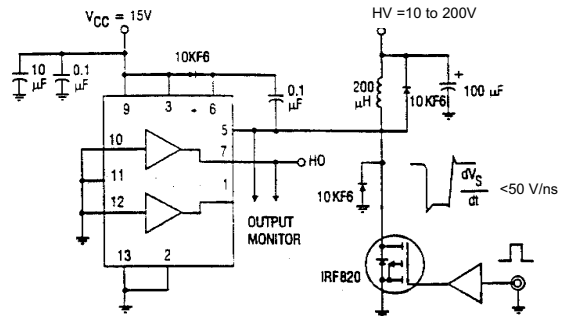


Figure 2. Floating Supply Voltage Transient Test Circuit

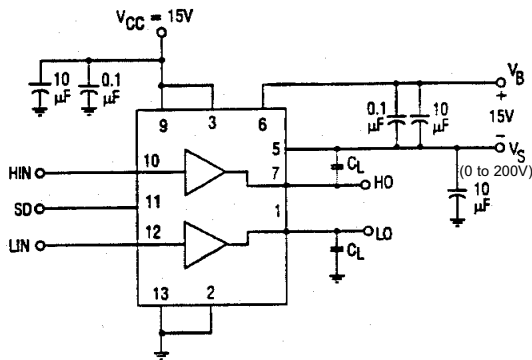


Figure 3. Switching Time Test Circuit

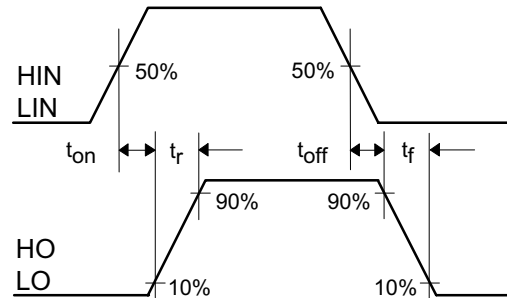


Figure 4. Switching Time Waveform Definition

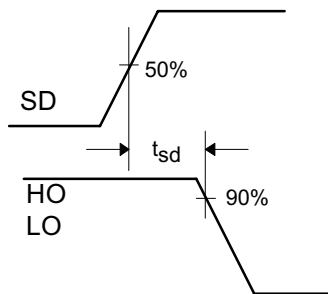


Figure 5. Shutdown Waveform Definitions

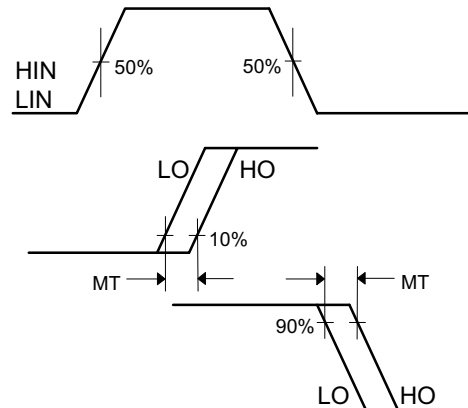


Figure 6. Delay Matching Waveform Definitions

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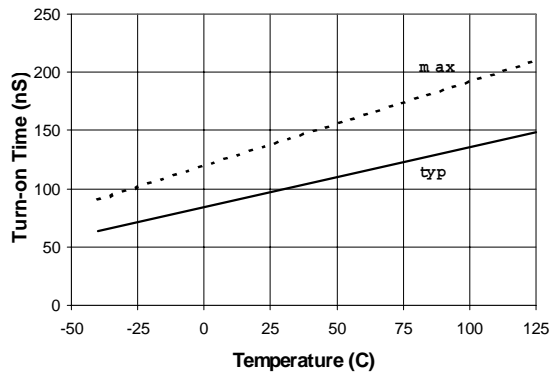


Figure 7A. Turn-on Time vs. Temperature

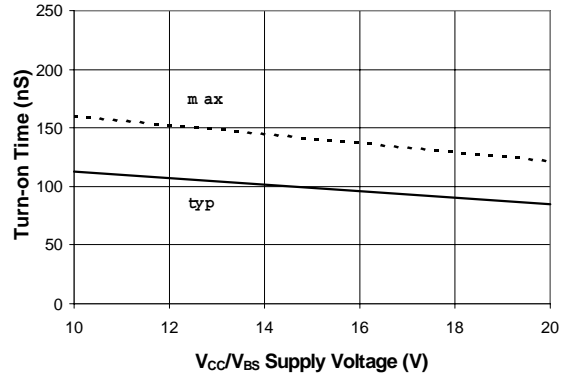


Figure 7B. Turn-on Time vs. Vcc/Vss Voltage

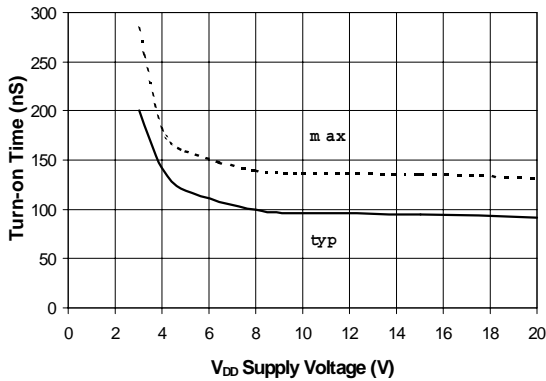


Figure 7C. Turn-on Time vs. VDD Voltage

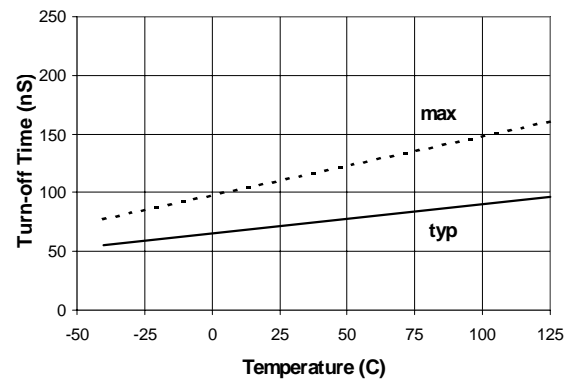


Figure 8A. Turn-off Time vs. Temperature

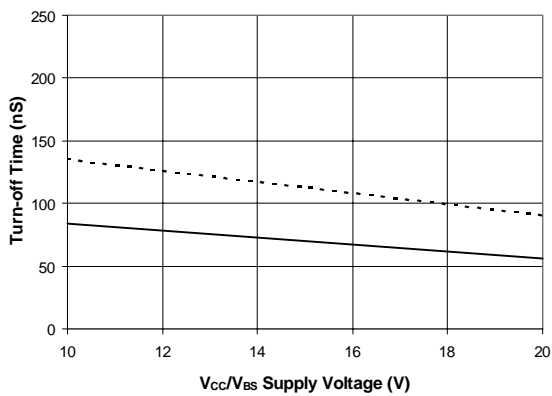


Figure 8B. Turn-off Time vs. Vcc/Vss Voltage

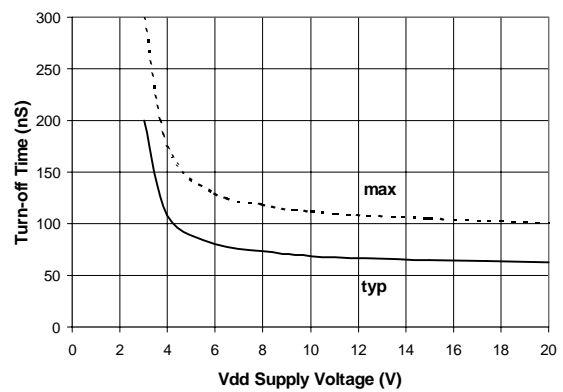


Figure 8C. Turn-off Time vs. VDD Voltage

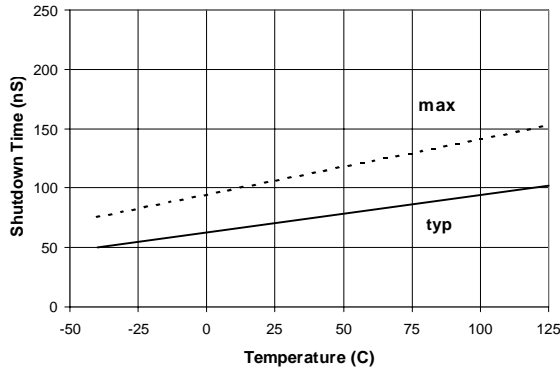


Figure 9A. Shutdown Time vs. Temperature

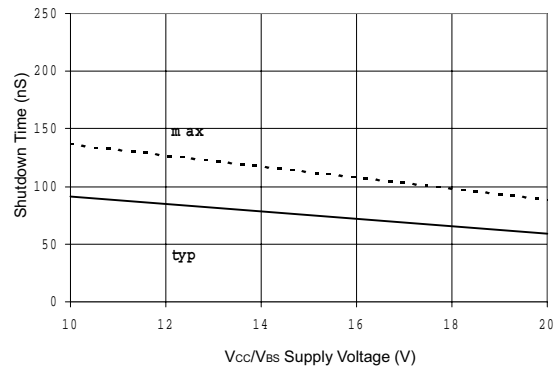


Figure 9B. Shutdown Time vs. Vcc/Vbs Voltage

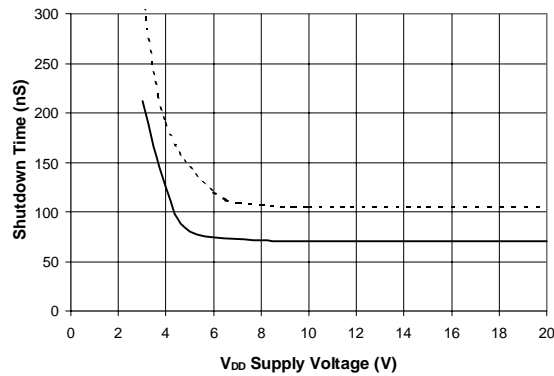


Figure 9C. Shutdown Time vs VDD Voltage

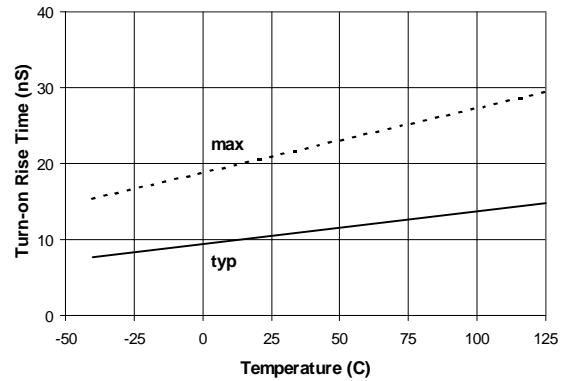


Figure 10A. Turn-on Rise Time vs. Temperature

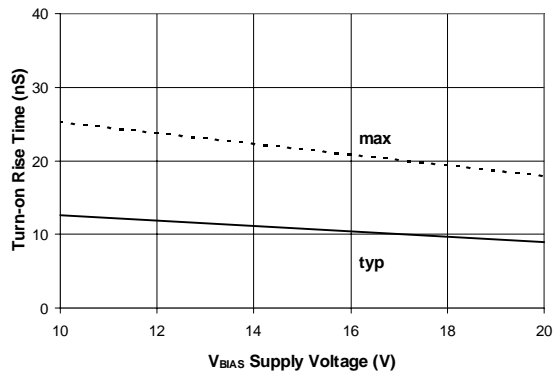


Figure 10B. Turn-on Rise Time vs. VBIAS (VCC=VBS=VDD) Voltage

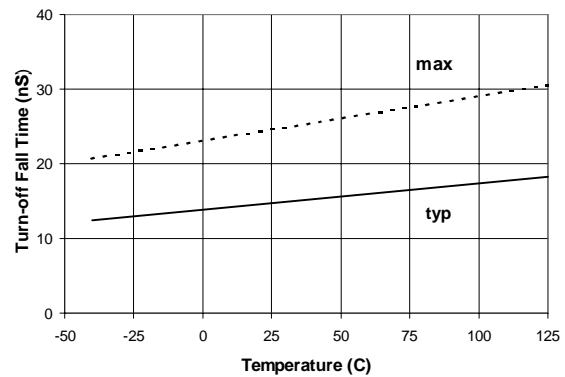


Figure 11A. Turn-off Fall Time vs. Temperature

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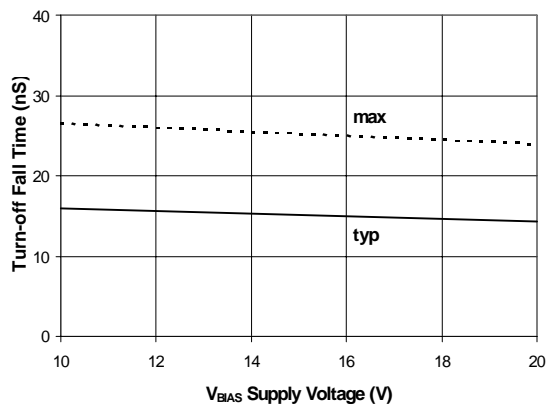


Figure 11B. Turn-Off Fall Time vs. V_{BIAS} (V_{CC}=V_{BS}=V_{DD}) Voltage

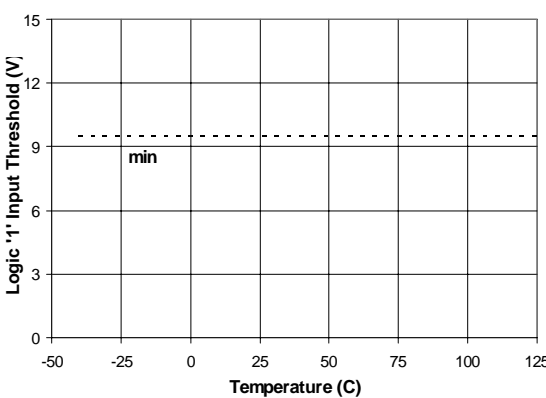


Figure 12A. Logic “1” Input Threshold vs. Temperature

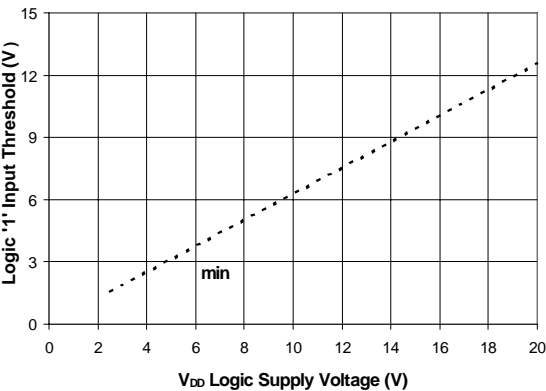


Figure 12B. Logic “1” Input Threshold vs. V_{DD} Voltage

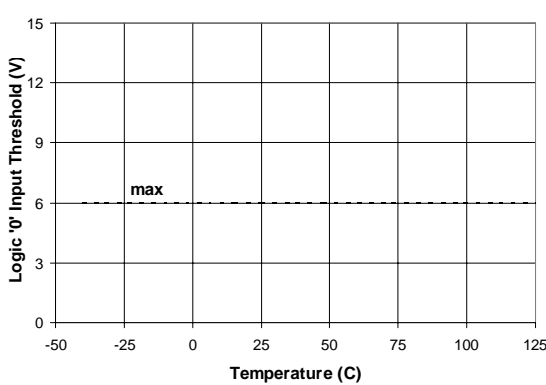


Figure 13A. Logic “0” Input Threshold vs. Temperature

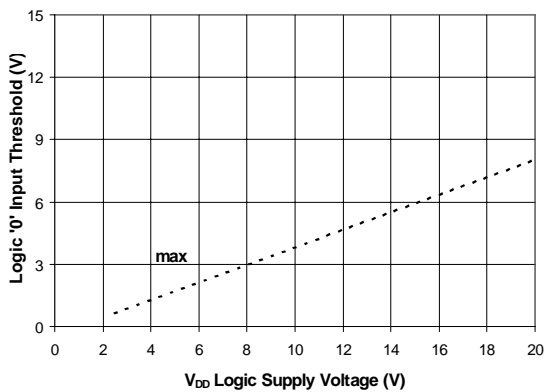


Figure 13B. Logic “0” Input Threshold vs. V_{DD} Voltage

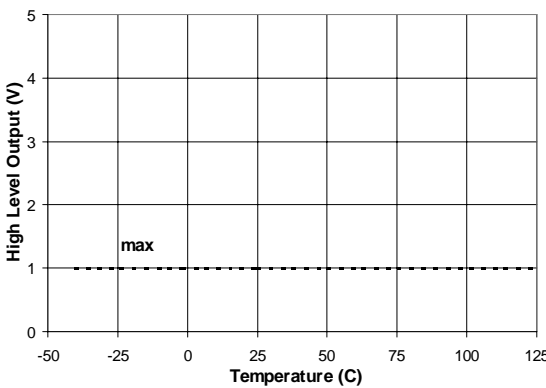


Figure 14A. High Level Output vs. Temperature

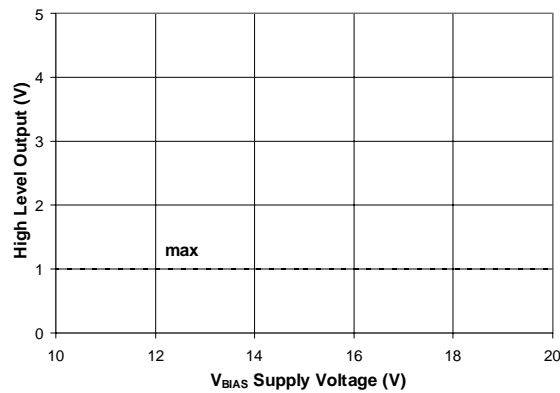


Figure 14B. High Level Output vs. V_{BIAS} Voltage

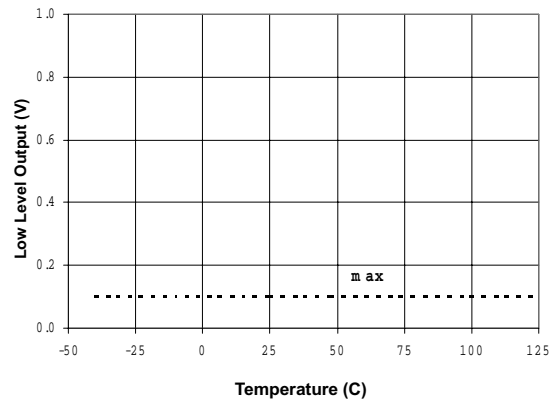


Figure 15A. Low Level Output vs. Temperature

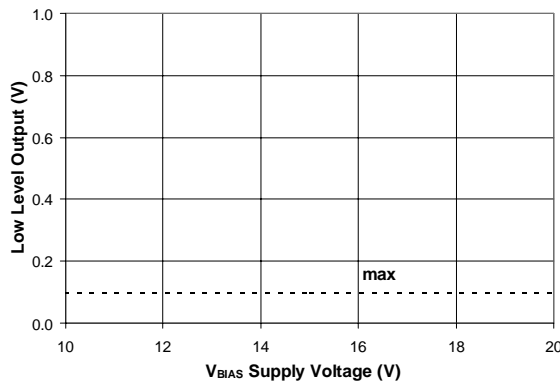


Figure 15B. Low Level Output vs. V_{BIAS} Voltage

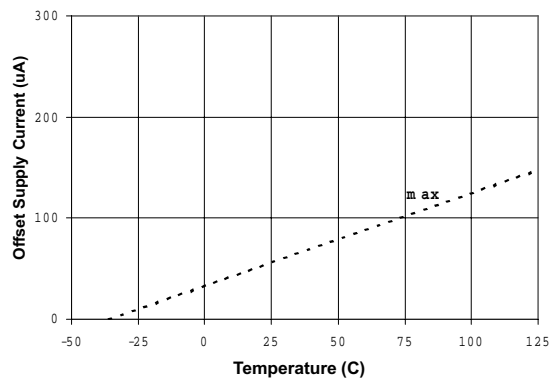


Figure 16A. Offset Supply Current vs. Temperature

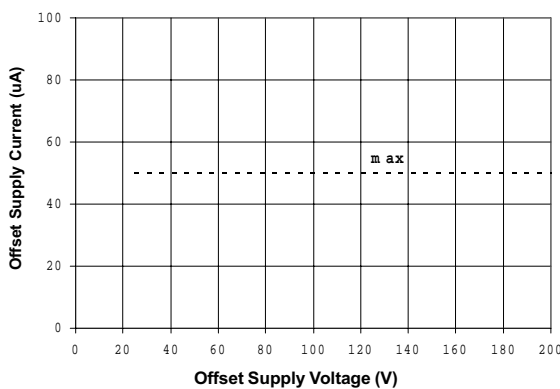


Figure 16B. Offset Supply Current vs. Offset Voltage

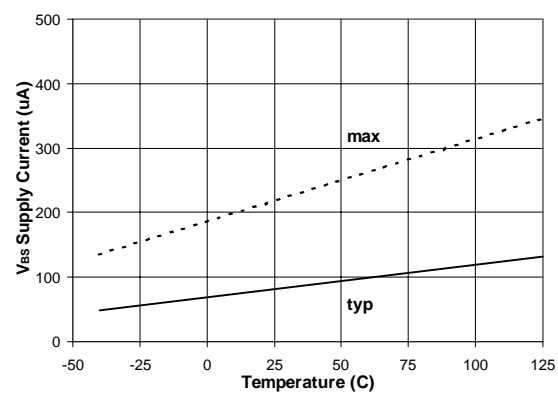


Figure 17A. V_{bs} Supply Current vs. Temperature

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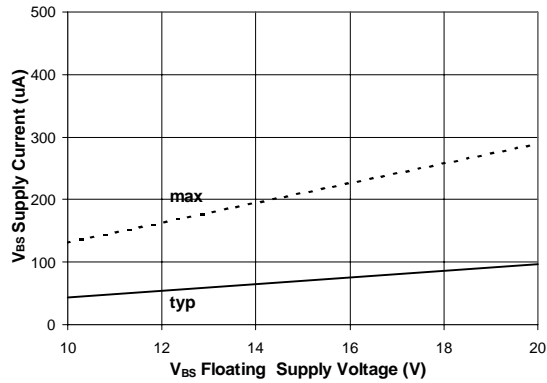


Figure 17B. Vbs Supply Current vs. Vbs Voltage

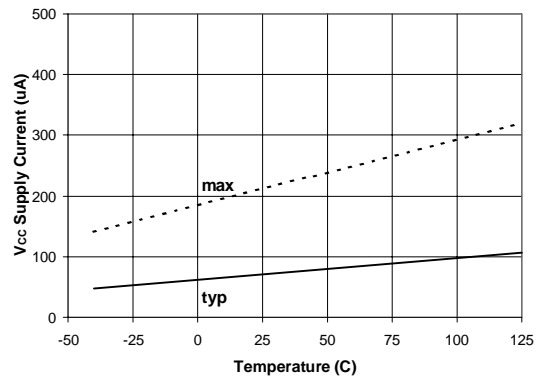


Figure 18A. Vcc Supply Current vs. Temperature

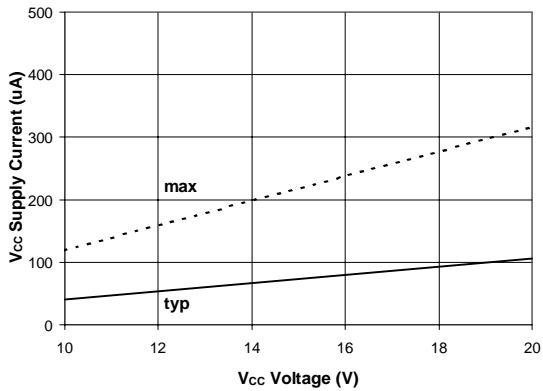


Figure 18B. Vcc Supply Current vs. Vcc Voltage

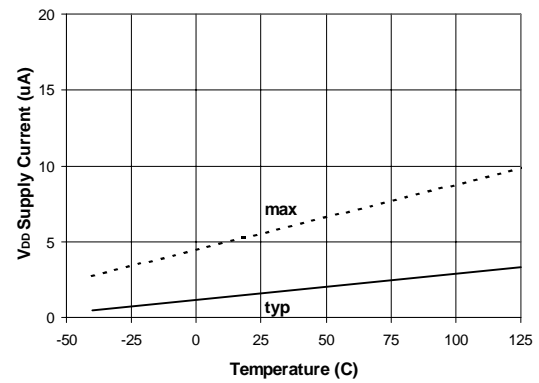


Figure 19A. Vdd Supply Current vs. Temperature

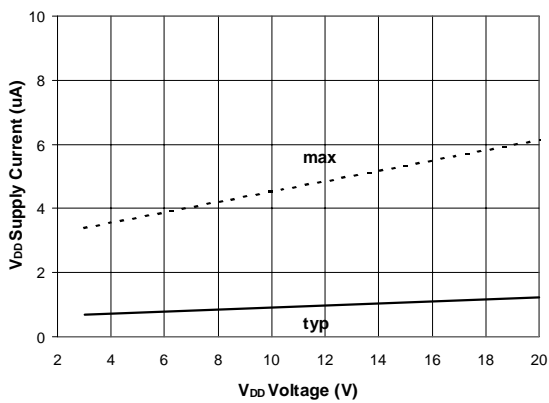


Figure 19B. Vdd Supply Current vs. Vdd Voltage

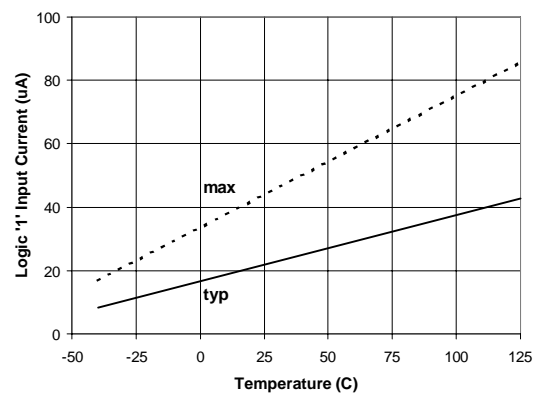


Figure 20A. Logic "1" Input Current vs. Temperature

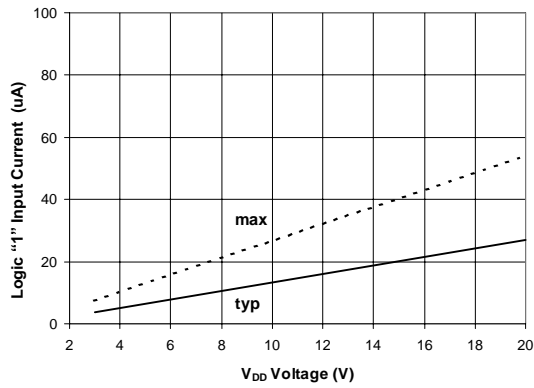


Figure 20B. Logic "1" Input Current vs. V_{DD} Voltage

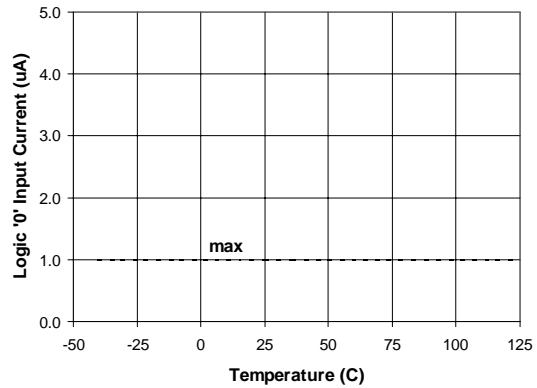


Figure 21A. Logic "0" Input Current vs. Temperature

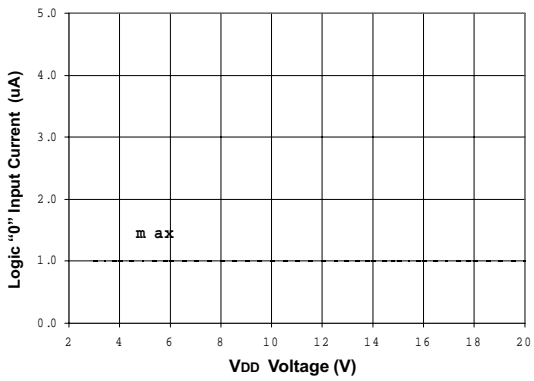


Figure 21B. Logic "0" Input Current vs. V_{DD} Voltage

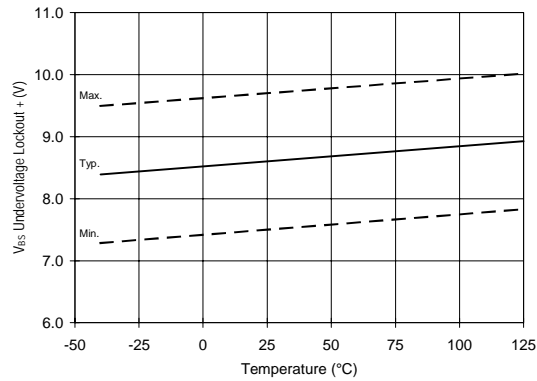


Figure 22. V_{BS} Undervoltage Lockout (+) vs. Temperature

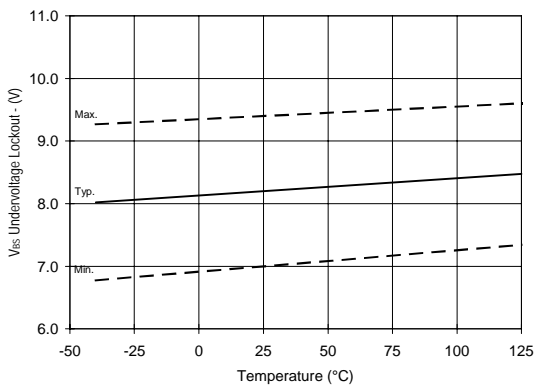


Figure 23. V_{BS} Undervoltage Lockout (-) vs. Temperature

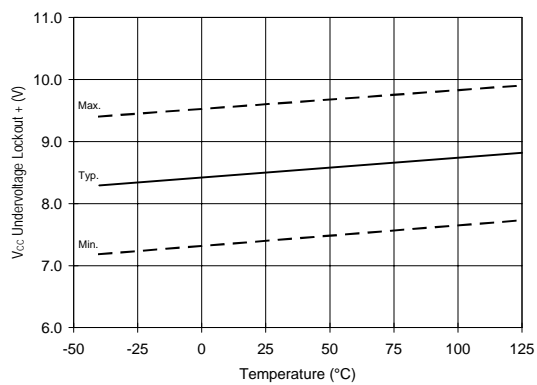


Figure 24. V_{CC} Undervoltage Lockout (+) vs. Temperature

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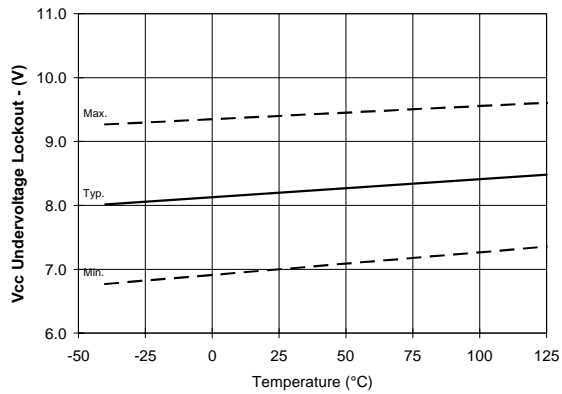


Figure 25. Vcc Undervoltage Lockout (-) vs. Temperature

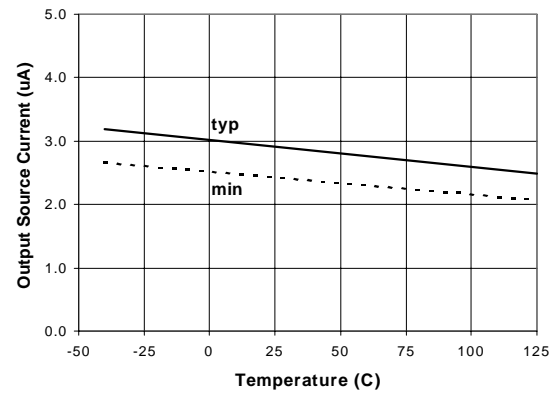


Figure 26A. Output Source Current vs. Temperature

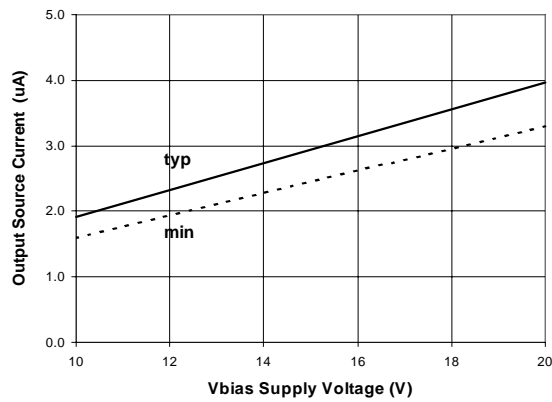


Figure 26B. Output Source Current vs. VBIAS Voltage

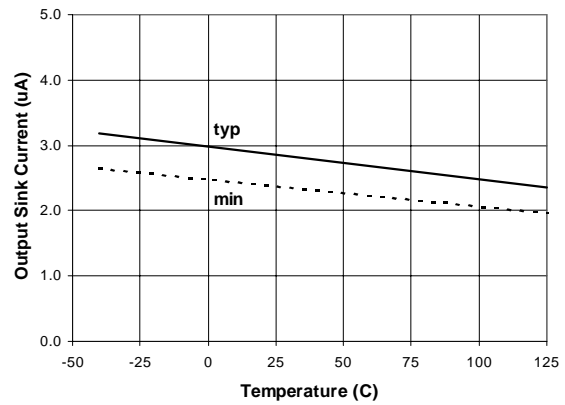


Figure 27A. Output Sink Current vs. Temperature

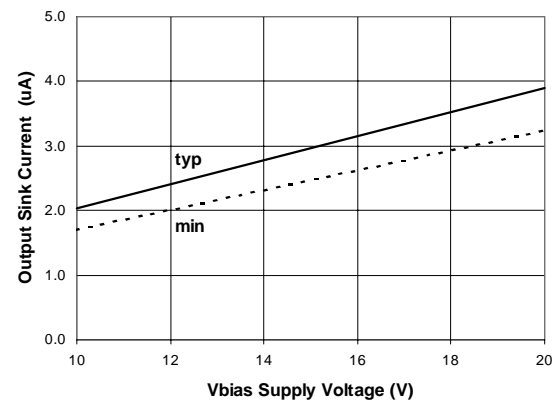


Figure 27B. Output Sink Current vs. VBIAS Voltage

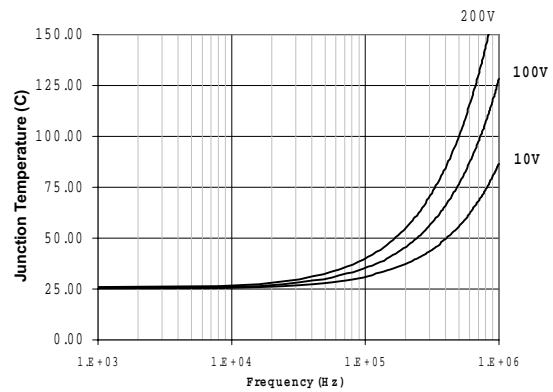


Figure 28. IR2010 Tj vs Frequency
 $R_{GATE} = 10 \text{ Ohm}$, $V_{CC} = 15V$ with IRFPE50

IR2010(s) & (PbF)

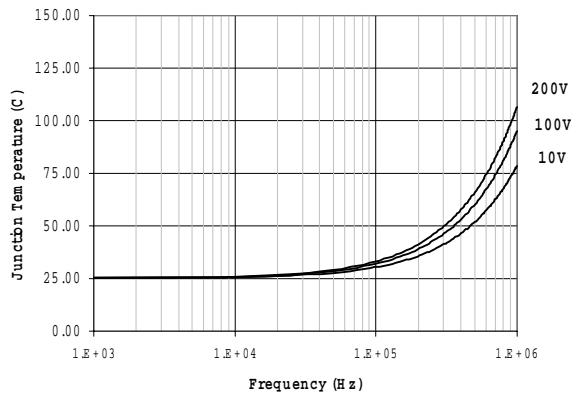


Figure 29. IR2010 Tj vs Frequency
R_{GATE} = 16 Ohm, V_{cc} = 15V with IRFBC40

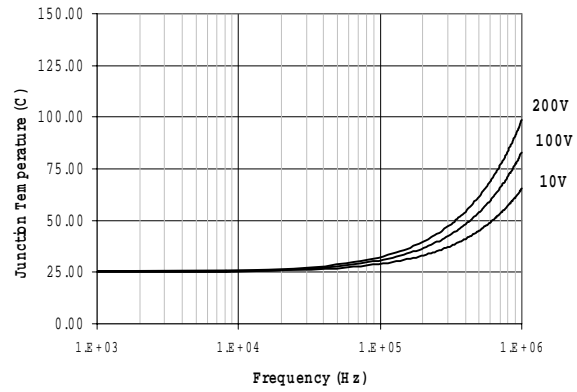


Figure 30. IR2010 Tj vs Frequency
R_{GATE} = 22 Ohm, V_{cc} = 15V with IRFBC30

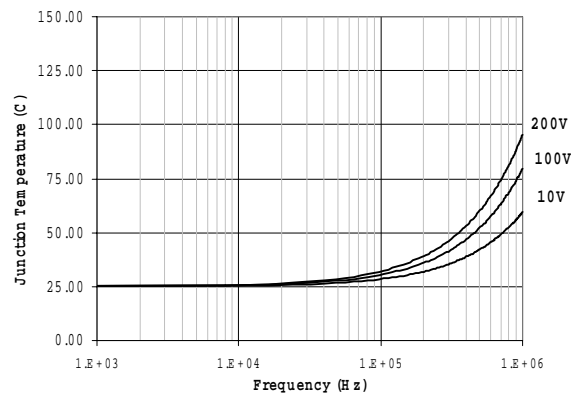


Figure 31. IR2010 Tj vs Frequency
R_{GATE} = 33 Ohm, V_{cc} = 15V with IRFBC20

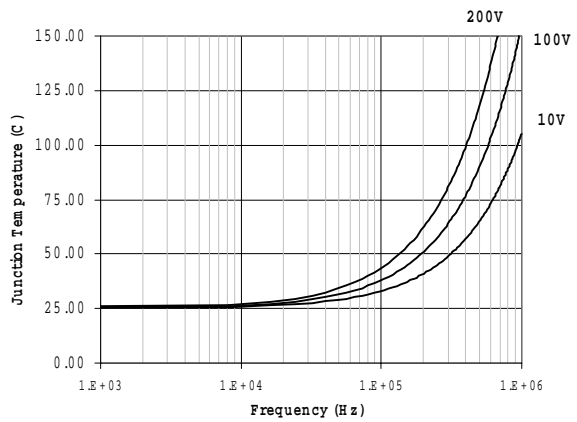


Figure 32. IR2010S Tj vs Frequency
R_{GATE} = 10 Ohm, V_{cc} = 15V with IRFPE50

IR2010(S) & (PbF)

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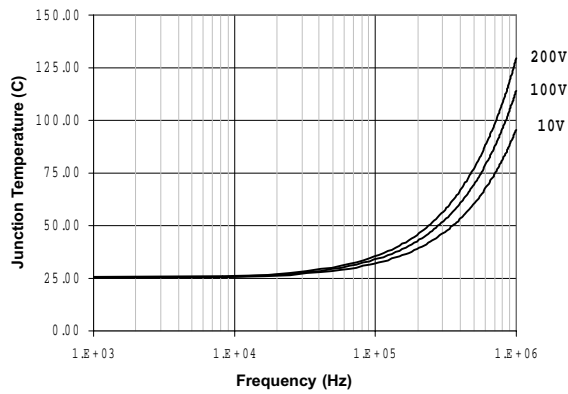


Figure 33. IR2010S Tj vs Frequency
R_{GATE} = 16 Ohm, V_{cc} = 15V with IRFBC40

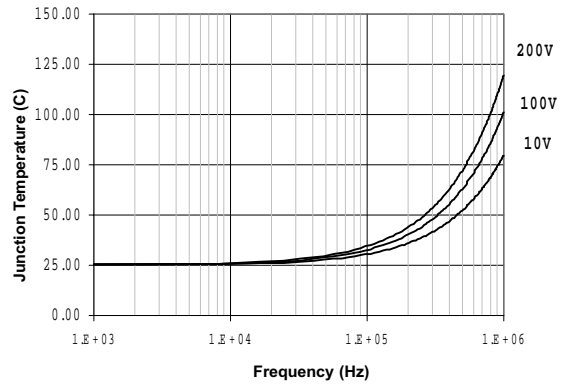


Figure 34. IR2010S Tj vs Frequency
R_{GATE} = 22 Ohm, V_{cc} = 15V with IRFBC30

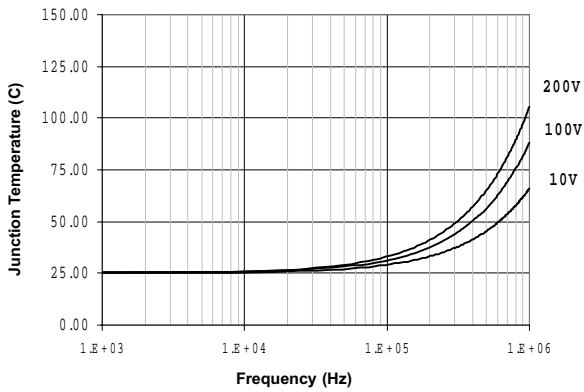
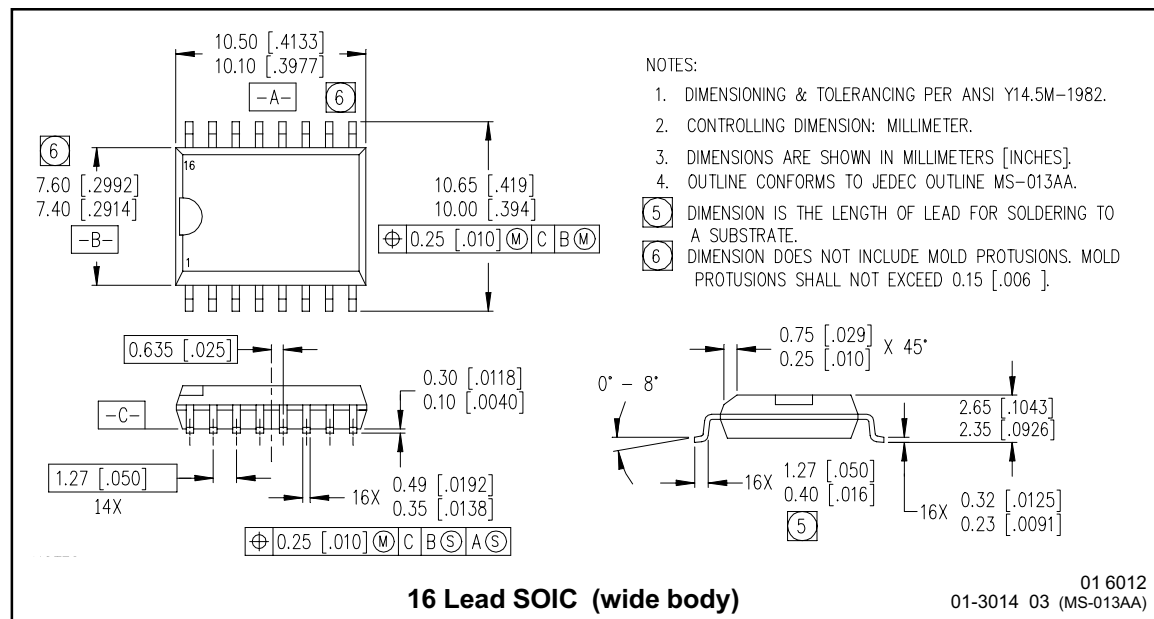
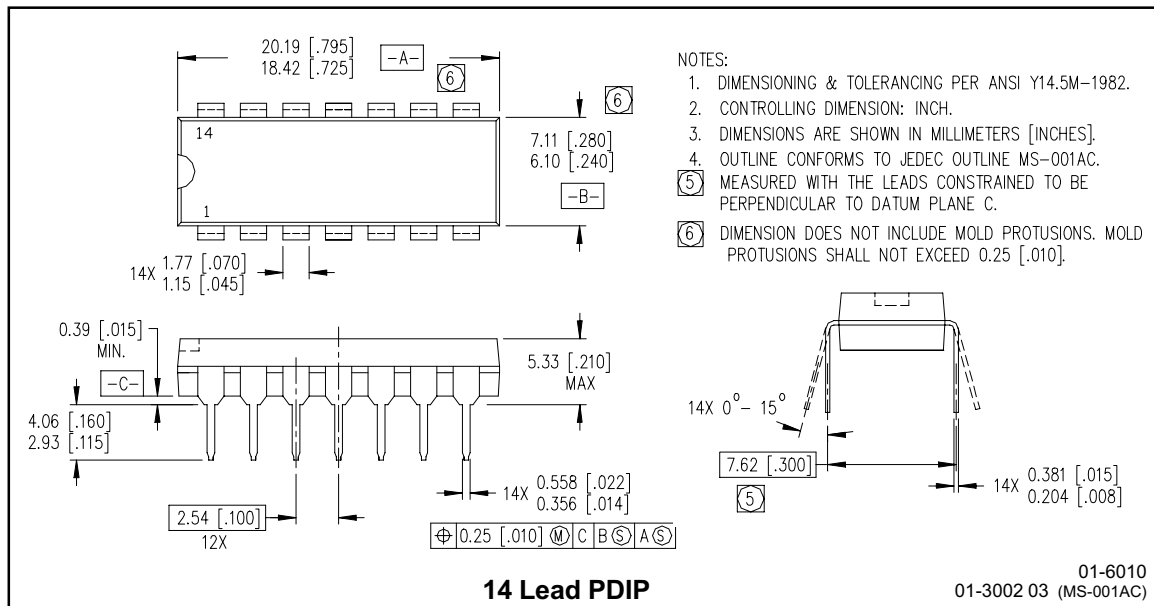


Figure 35. IR2010S Tj vs Frequency
R_{GATE} = 33 Ohm, V_{cc} = 15V with IRFBC20

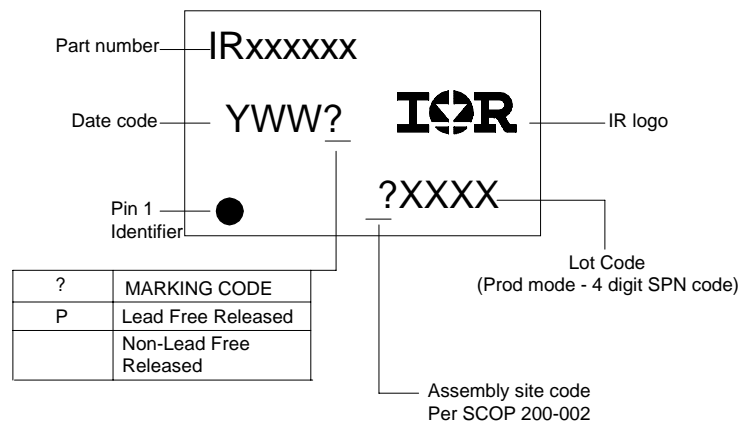
Case Outlines



IR2010(S) & (PbF)

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LEADFREE PART MARKING INFORMATION



ORDER INFORMATION

Basic Part (Non-Lead Free)

14-Lead PDIP IR2010 order IR2010

16-Lead SOIC IR2010S order IR2010S

Leadfree Part

14-Lead PDIP IR2010 order IR2010PbF

16-Lead SOIC IR2010S order IR2010SPbF

International
IOR Rectifier

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This product has been qualified per industrial level

Data and specifications subject to change without notice. 9/12/2004