

RADIATION HARDENED POWER MOSFET SURFACE MOUNT(LCC-18)

IRHE7130
JANSR2N7261U
100V, N-CHANNEL

REF: MIL-PRF-19500/601

RAD Hard™ HEXFET® TECHNOLOGY

Product Summary

Part Number	Radiation Level	RDS(on)	ID	QPL Part Number
IRHE7130	100K Rads (Si)	0.18Ω	8.0A	JANSR2N7261U
IRHE3130	300K Rads (Si)	0.18Ω	8.0A	JANSF2N7261U
IRHE4130	600K Rads (Si)	0.18Ω	8.0A	JANSG2N7261U
IRHE8130	1000K Rads (Si)	0.18Ω	8.0A	JANSH2N7261U



International Rectifier's RADHard HEXFET® technology provides high performance power MOSFETs for space applications. This technology has over a decade of proven performance and reliability in satellite applications. These devices have been characterized for both Total Dose and Single Event Effects (SEE). The combination of low Rdson and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching, ease of paralleling and temperature stability of electrical parameters.

Features:

- Single Event Effect (SEE) Hardened
- Low RDS(on)
- Low Total Gate Charge
- Proton Tolerant
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Surface Mount
- Light Weight

Absolute Maximum Ratings

Pre-Irradiation

	Parameter		Units
ID @ VGS = 12V, TC = 25°C	Continuous Drain Current	8.0	A
ID @ VGS = 12V, TC = 100°C	Continuous Drain Current	5.0	
IDM	Pulsed Drain Current ①	32	
PD @ TC = 25°C	Max. Power Dissipation	25	W
	Linear Derating Factor	0.20	W/°C
VGS	Gate-to-Source Voltage	±20	V
EAS	Single Pulse Avalanche Energy ②	130	mJ
IAR	Avalanche Current ①	—	A
EAR	Repetitive Avalanche Energy ①	—	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.5	V/ns
TJ	Operating Junction	-55 to 150	°C
TSTG	Storage Temperature Range		
	Package Mounting Surface Temperature	300 (for 5s)	
	Weight	0.42 (Typical)	g

For footnotes refer to the last page

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{GS} = 0V, I_D = 1.0mA$
$\Delta BV_{DSS}/\Delta T_J$	Temperature Coefficient of Breakdown Voltage	—	0.10	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1.0mA$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.18	Ω	$V_{GS} = 12V, I_D = 5.0A$ ④
		—	—	0.185		$V_{GS} = 12V, I_D = 8.0A$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 1.0mA$
g_{fs}	Forward Transconductance	2.5	—	—	S (③)	$V_{DS} > 15V, I_{DS} = 5.0A$ ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	25	μA	$V_{DS} = 80V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 80V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	$V_{GS} = 20V$
I_{GSS}	Gate-to-Source Leakage Reverse	—	—	-100		$V_{GS} = -20V$
Q_g	Total Gate Charge	—	—	50	nC	$V_{GS} = 12V, I_D = 8.0A$ $V_{DS} = 50V$
Q_{gs}	Gate-to-Source Charge	—	—	12		
Q_{gd}	Gate-to-Drain ('Miller') Charge	—	—	20		
$t_{d(on)}$	Turn-On Delay Time	—	—	25	ns	$V_{DD} = 50V, I_D = 8.0A$ $V_{GS} = 12V, R_G = 7.5\Omega$
t_r	Rise Time	—	—	55		
$t_{d(off)}$	Turn-Off Delay Time	—	—	55		
t_f	Fall Time	—	—	45		
$L_S + L_D$	Total Inductance	—	6.1	—	nH	Measured from the center of drain pad to center of source pad
C_{iss}	Input Capacitance	—	1100	—	pF	$V_{GS} = 0V, V_{DS} = 25V$ $f = 1.0MHz$
C_{oss}	Output Capacitance	—	310	—		
C_{rss}	Reverse Transfer Capacitance	—	55	—		

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	8.0	A	T _j = 25°C, I _S = 8.0A, V _{GS} = 0V ④
I _{SM}	Pulse Source Current (Body Diode) ①	—	—	32		
V _{SD}	Diode Forward Voltage	—	—	1.5	V	T _j = 25°C, I _F = 8.0A, di/dt ≤ 100A/μs V _{DD} ≤ 50V ④
t _{rr}	Reverse Recovery Time	—	—	350	nS	
Q _{RR}	Reverse Recovery Charge	—	—	3.0	μC	
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .				

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R_{thJC}	Junction-to-Case	—	—	5.0	$^\circ\text{C/W}$	
R_{thJPCB}	Junction-to-PC Board	—	19	—		Soldered to a copper clad PC board

Note: Corresponding Spice and Saber models are available on the G&S Website.

For footnotes refer to the last page

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table 1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

	Parameter	100K Rads (Si) ¹		300 - 1000K Rads (Si) ²		Units	Test Conditions
		Min	Max	Min	Max		
BVDSS	Drain-to-Source Breakdown Voltage	100	—	100	—	V	V _{GS} = 0V, I _D = 1.0mA
V _{GS(th)}	Gate Threshold Voltage	2.0	4.0	1.25	4.5		V _{GS} = V _{DS} , I _D = 1.0mA
I _{GSS}	Gate-to-Source Leakage Forward	—	100	—	100	nA	V _{GS} = 20V
I _{GSS}	Gate-to-Source Leakage Reverse	—	-100	—	-100		V _{GS} = -20 V
I _{DSS}	Zero Gate Voltage Drain Current	—	25	—	50	μA	V _{DS} =80V, V _{GS} =0V
R _{DS(on)}	Static Drain-to-Source ④ On-State Resistance (TO-3)	—	0.18	—	0.24	Ω	V _{GS} = 12V, I _D =5.0A
R _{DS(on)}	Static Drain-to-Source ④ On-State Resistance (LCC-18)	—	0.18	—	0.24	Ω	V _{GS} = 12V, I _D =5.0A
V _{SD}	Diode Forward Voltage ④	—	1.5	—	1.5	V	V _{GS} = 0V, I _S = 8.0A

1. Part numbers IRHE7130, (JANSR2N7261U)

2. Part number IRHE8130, IRHE3130, and IRHE4130(JANSF2N7261U, JANSF2N7261U, JANSH2N7261U)

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Single Event Effect Safe Operating Area

Ion	LET MeV/(mg/cm ²))	Energy (MeV)	Range (μm)	V _{DS} (V)				
				@V _{GS} =0V	@V _{GS} =-5V	@V _{GS} =-10V	@V _{GS} =-15V	@V _{GS} =-20V
Cu	28	285	43	100	100	100	80	60
Br	36.8	305	39	100	90	70	50	—

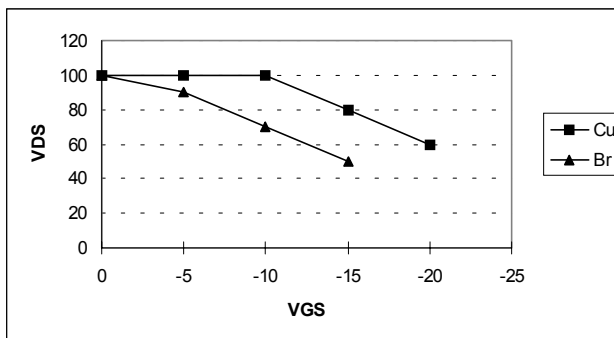


Fig a. Single Event Effect, Safe Operating Area

For footnotes refer to the last page

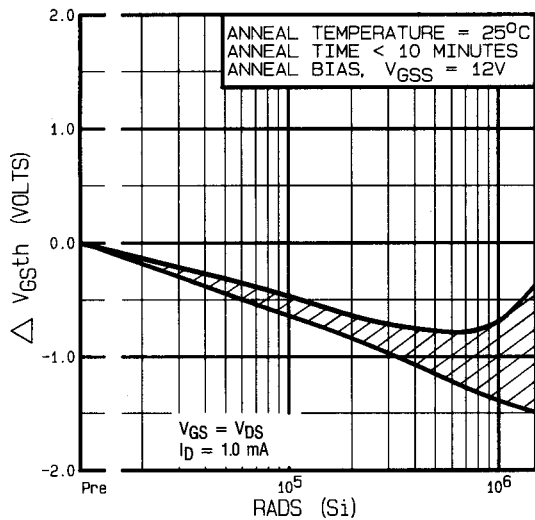


Fig 1. Typical Response of Gate Threshold Voltage Vs. Total Dose Exposure

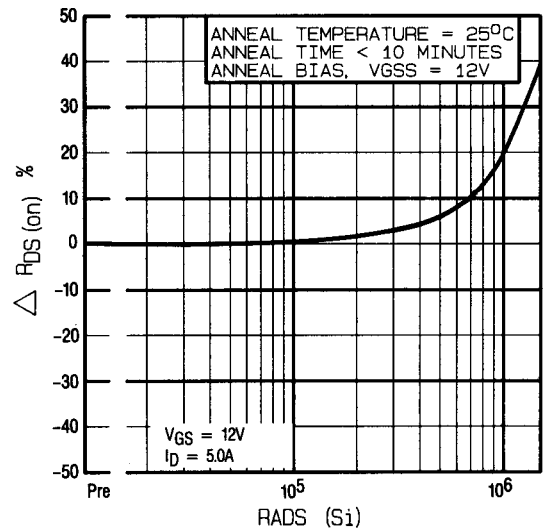


Fig 2. Typical Response of On-State Resistance Vs. Total Dose Exposure

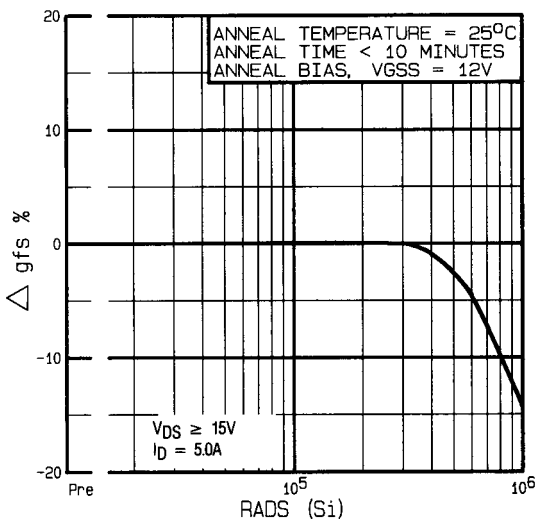


Fig 3. Typical Response of Transconductance Vs. Total Dose Exposure

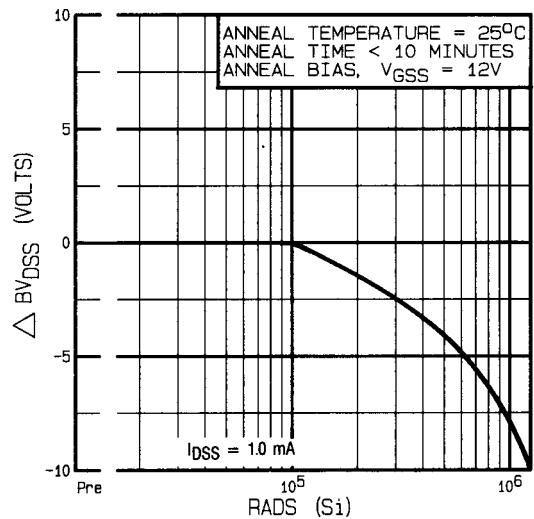


Fig 4. Typical Response of Drain to Source Breakdown Vs. Total Dose Exposure

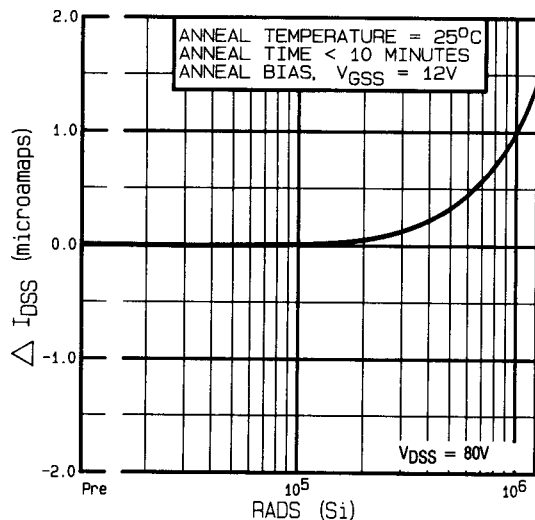


Fig 5. Typical Zero Gate Voltage Drain Current Vs. Total Dose Exposure

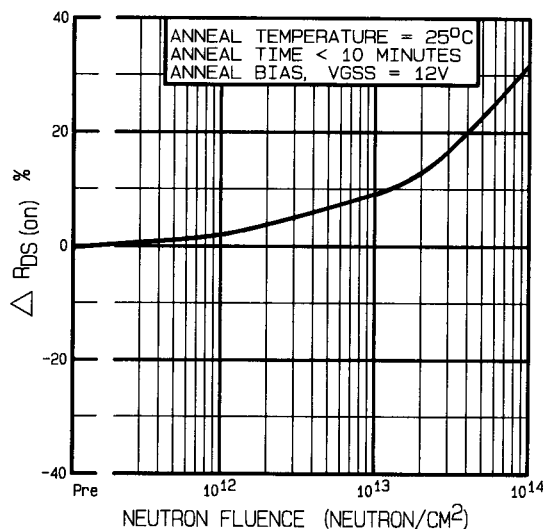


Fig 6. Typical On-State Resistance Vs. Neutron Fluence Level

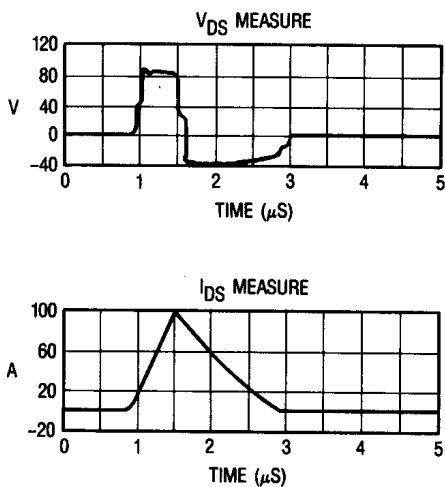


Fig 7. Typical Transient Response of Rad Hard HEXFET During 1×10^{12} Rad (Si)/Sec Exposure

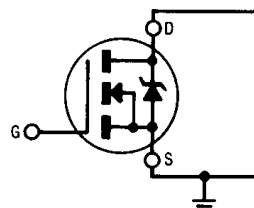


Fig 8a. Gate Stress of V_{GSS} Equals 12 Volts During Radiation

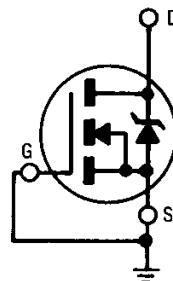


Fig 8b. V_{DS} Stress Equals 80% of B_{VDS} During Radiation

Note: Bias Conditions during radiation: $V_{GS} = 12\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$

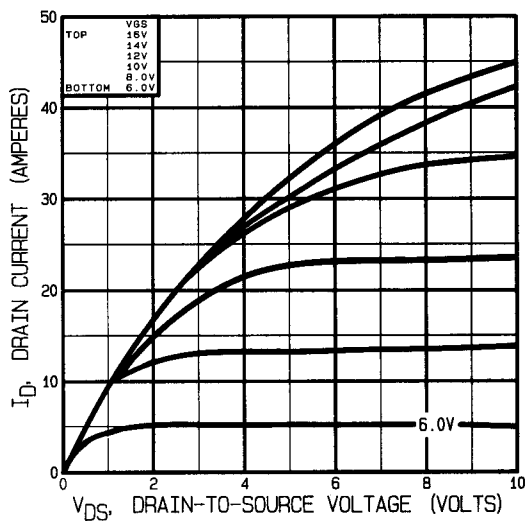


Fig 9. Typical Output Characteristics
Pre-Irradiation

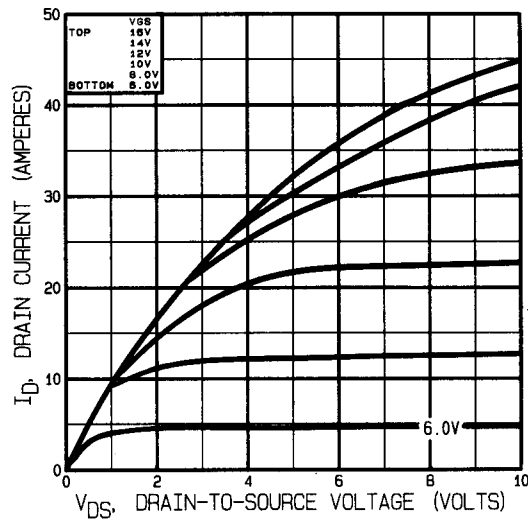


Fig 10. Typical Output Characteristics
Post-Irradiation 100K Rads (Si)

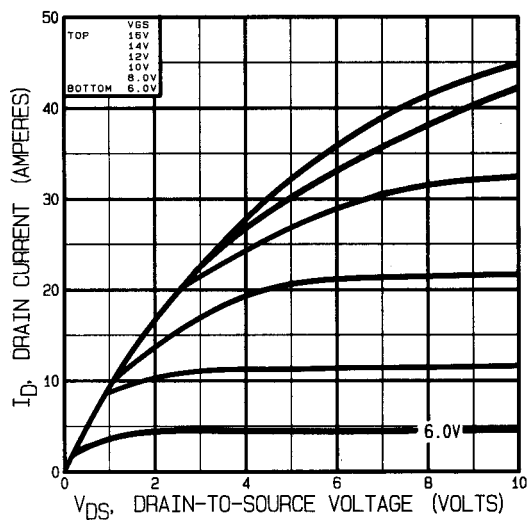


Fig 11. Typical Output Characteristics
Post-Irradiation 300K Rads (Si)

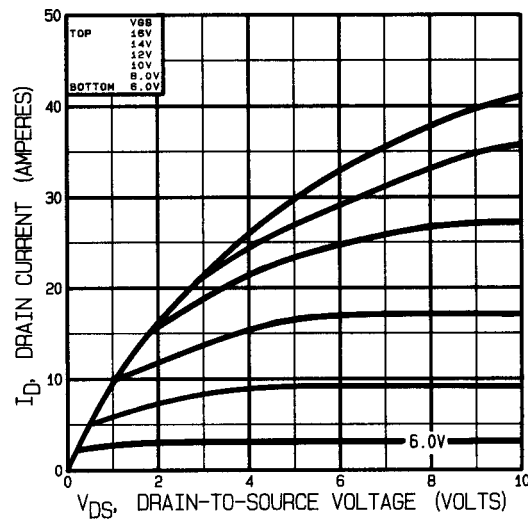


Fig 12. Typical Output Characteristics
Post-Irradiation 1 Mega Rads (Si)

Note: Bias Conditions during radiation: $V_{GS} = 0$ Vdc, $V_{DS} = 80$ Vdc

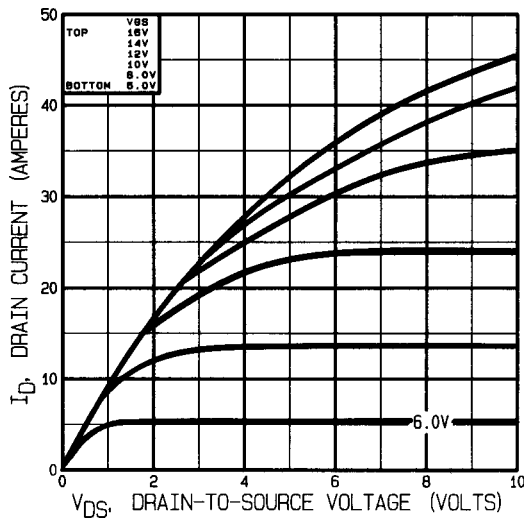


Fig 13. Typical Output Characteristics
Pre-Irradiation

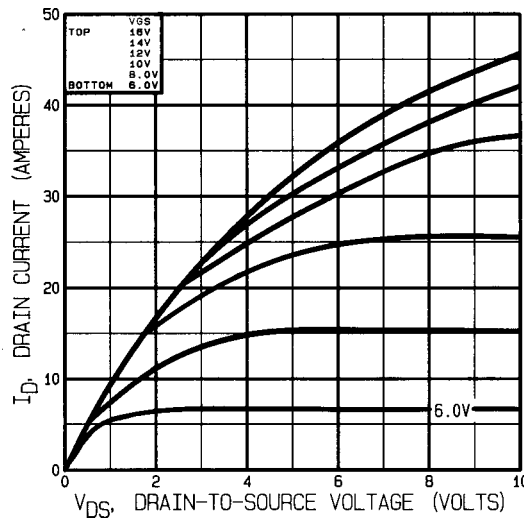


Fig 14. Typical Output Characteristics
Post-Irradiation 100K Rads (Si)

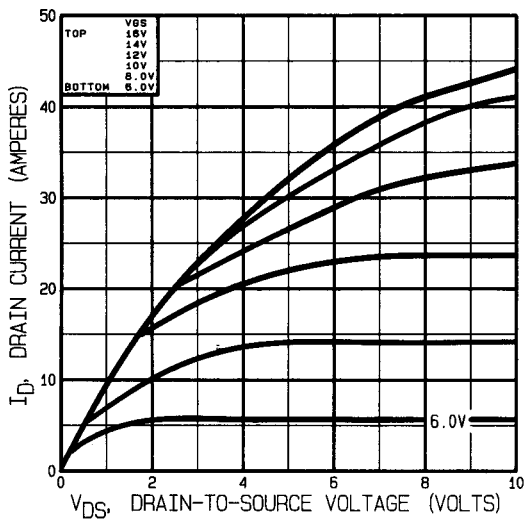


Fig 15. Typical Output Characteristics
Post-Irradiation 300K Rads (Si)

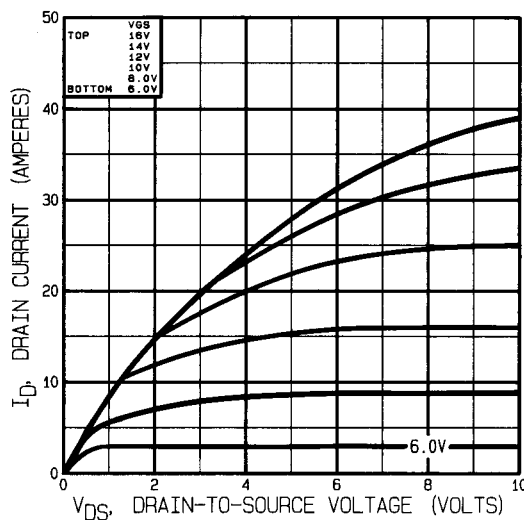


Fig 16. Typical Output Characteristics
Post-Irradiation 1 Mega Rads (Si)

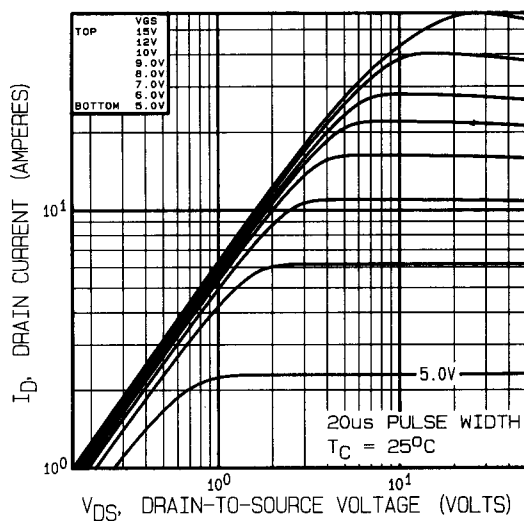


Fig 17. Typical Output Characteristics

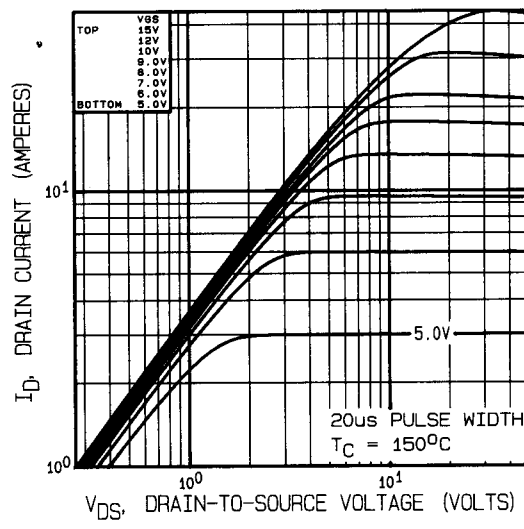


Fig 18. Typical Output Characteristics

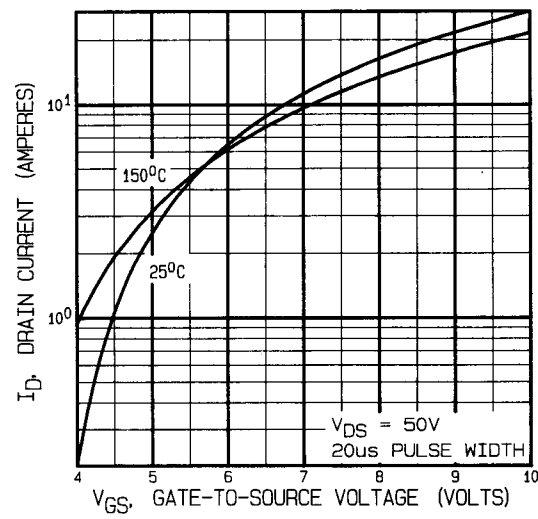


Fig 19. Typical Transfer Characteristics

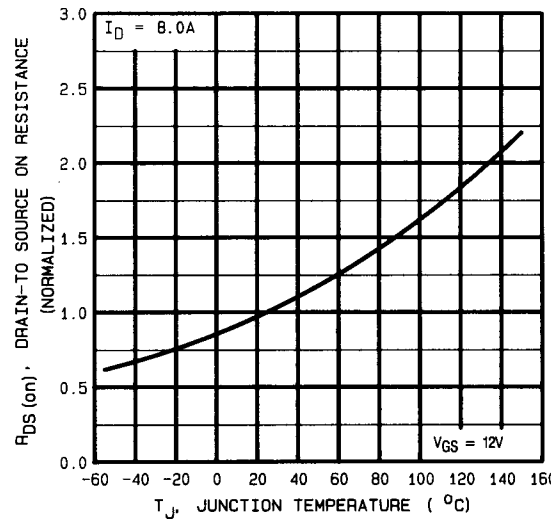


Fig 20. Normalized On-Resistance Vs. Temperature

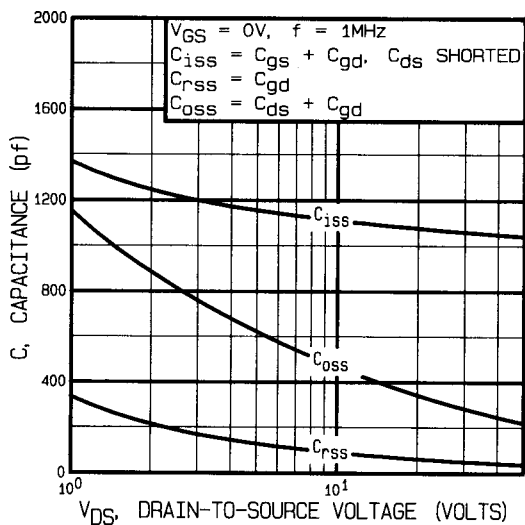


Fig 21. Typical Capacitance Vs. Drain-to-Source Voltage

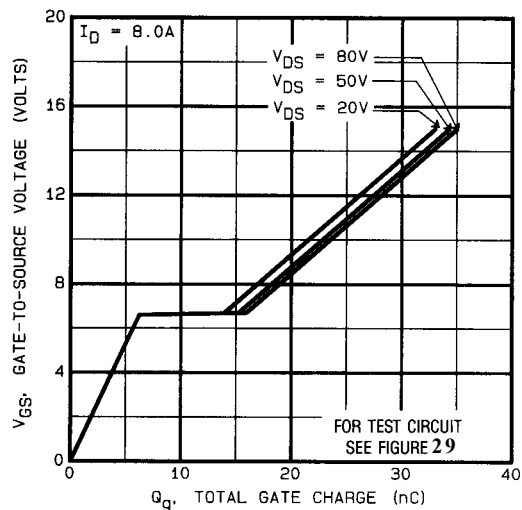


Fig 22. Typical Gate Charge Vs. Gate-to-Source Voltage

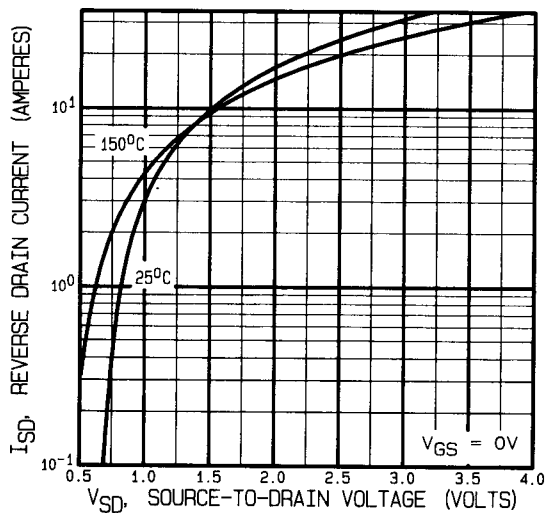


Fig 23. Typical Source-Drain Diode Forward Voltage

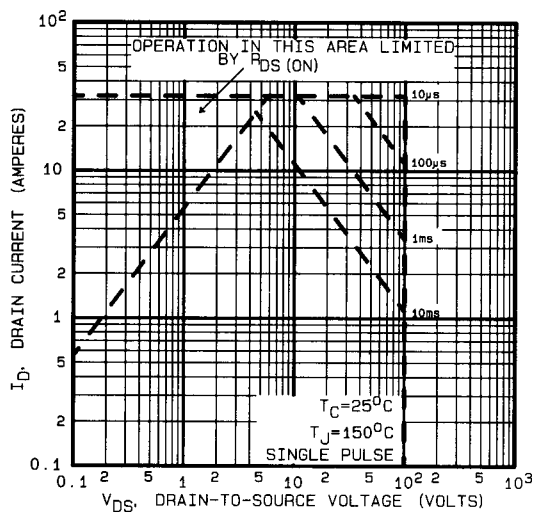


Fig 24. Maximum Safe Operating Area

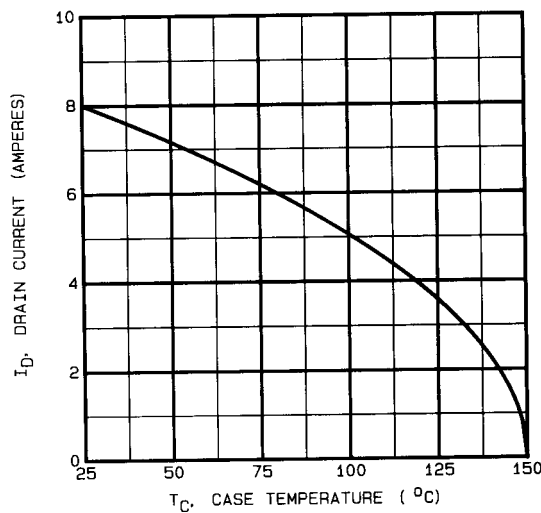


Fig 25. Maximum Drain Current Vs. Case Temperature

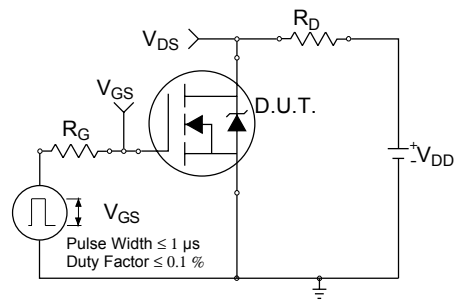


Fig 26a. Switching Time Test Circuit

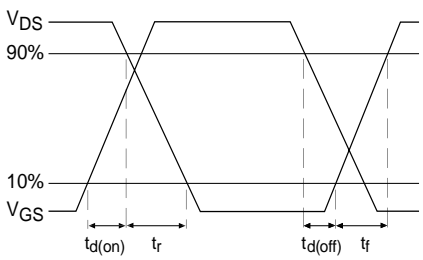


Fig 26b. Switching Time Waveforms

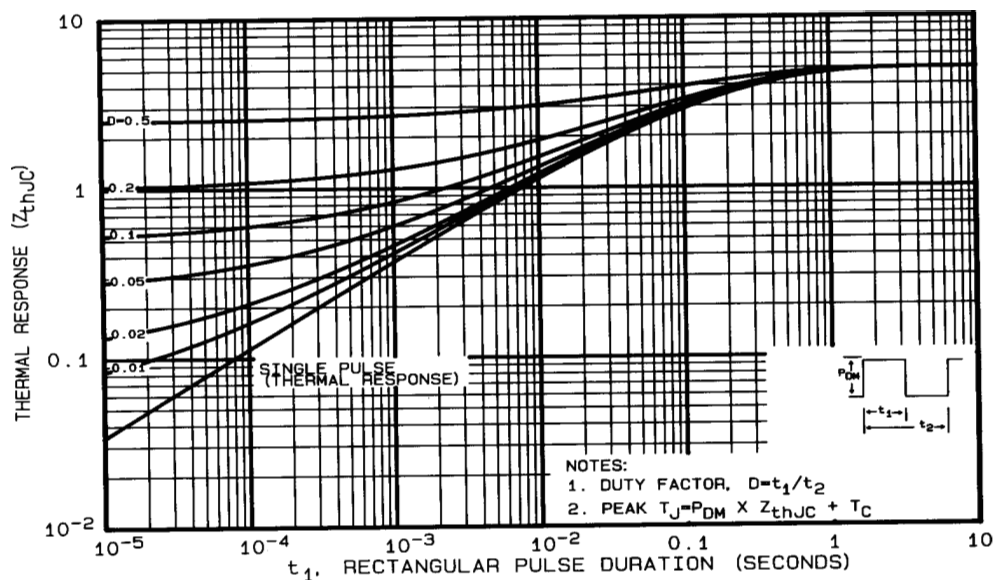


Fig 27. Maximum Effective Transient Thermal Impedance, Junction-to-Case

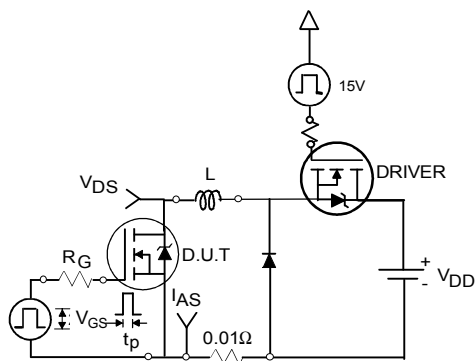


Fig 28a. Unclamped Inductive Test Circuit

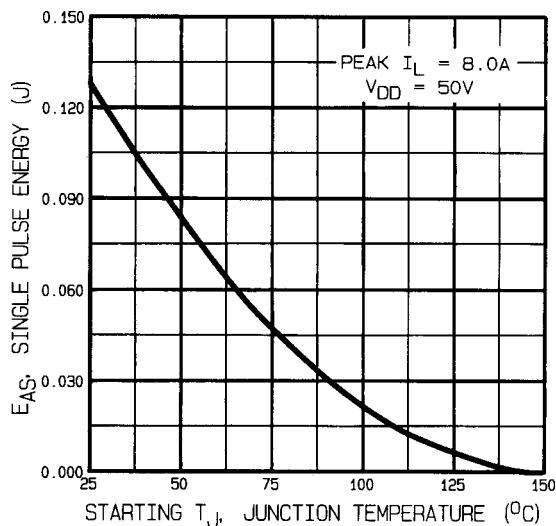


Fig 28c. Maximum Avalanche Energy Vs. Drain Current

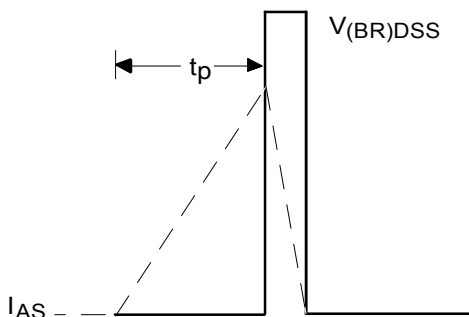


Fig 28b. Unclamped Inductive Waveforms

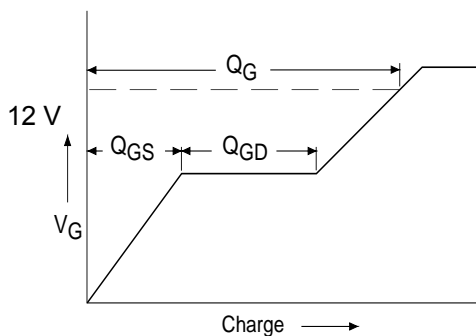


Fig 29a. Basic Gate Charge Waveform

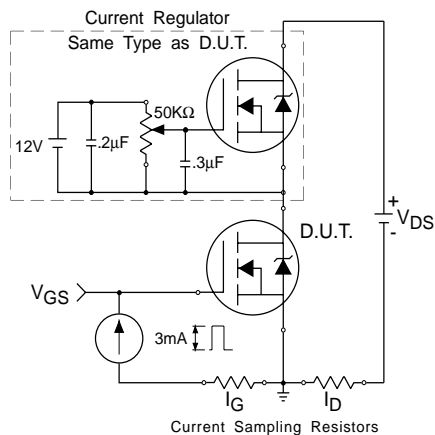
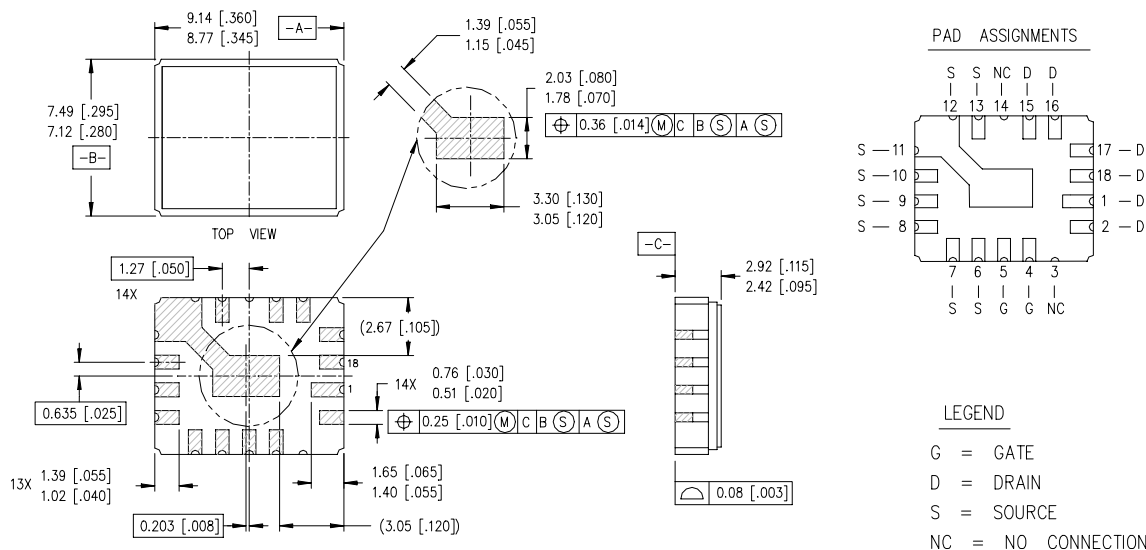


Fig 29b. Gate Charge Test Circuit

Foot Notes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② $V_{DD} = 25V$, starting $T_J = 25^\circ C$, $L = 4.1mH$
Peak $I_L = 8.0A$, $V_{GS} = 12V$
- ③ $ISD \leq 8.0A$, $di/dt \leq 140A/\mu s$,
 $V_{DD} \leq 100V$, $T_J \leq 150^\circ C$
- ④ Pulse width $\leq 300 \mu s$; Duty Cycle $\leq 2\%$
- ⑤ **Total Dose Irradiation with V_{GS} Bias.**
12 volt V_{GS} applied and $V_{DS} = 0$ during irradiation per MIL-STD-750, method 1019, condition A.
- ⑥ **Total Dose Irradiation with V_{DS} Bias.**
80 volt V_{DS} applied and $V_{GS} = 0$ during irradiation per MIL-STD-750, method 1019, condition A.

Case Outline and Dimensions — LCC-18



NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

International
IR Rectifier

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