

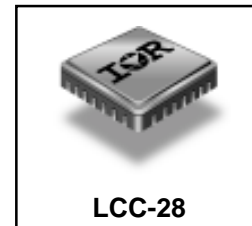
**RADIATION HARDENED 100V, Combination 2N-2P-CHANNEL
POWER MOSFET
SURFACE MOUNT (LCC-28)**

IRHQ567110

**RAD-Hard™ HEXFET®
TECHNOLOGY**

Product Summary

Part Number	Radiation Level	RDS(on)	Id	CHANNEL
IRHQ567110	100K Rads (Si)	0.27Ω	4.6A	N
IRHQ563110	300K Rads (Si)	0.29Ω	4.6A	N
IRHQ567110	100K Rads (Si)	0.96Ω	-2.8A	P
IRHQ563110	300K Rads (Si)	0.98Ω	-2.8A	P



International Rectifier's RAD-Hard™ HEXFET® MOSFET Technology provides high performance power MOSFETs for space applications. This technology has over a decade of proven performance and reliability in satellite applications. These devices have been characterized for both Total Dose and Single Event Effects (SEE). The combination of low RDS(on) and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching, ease of paralleling and temperature stability of electrical parameters.

Features:

- Single Event Effect (SEE) Hardened
- Low RDS(on)
- Low Total Gate Charge
- Proton Tolerant
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Ceramic Package
- Surface Mount
- Light Weight

Absolute Maximum Ratings (Per Die)

Pre-Irradiation

	Parameter	N-Channel	P-Channel	Units
I _D @ V _{GS} = ±12V, T _C = 25°C	Continuous Drain Current	4.6	-2.8	A
I _D @ V _{GS} = ±12V, T _C = 100°C	Continuous Drain Current	2.9	-1.8	
I _{DM}	Pulsed Drain Current ①	18.4	-11.2	
P _D @ T _C = 25°C	Max. Power Dissipation	12	12	W
	Linear Derating Factor	0.1	0.1	W/°C
V _{GS}	Gate-to-Source Voltage	±20	±20	V
E _{AS}	Single Pulse Avalanche Energy	47 ②	70 ⑦	mJ
I _{AR}	Avalanche Current ①	4.6	-2.8	A
E _{AR}	Repetitive Avalanche Energy ①	1.2	1.2	mJ
dv/dt	Peak Diode Recovery dv/dt	6.1 ③	7.1 ⑧	V/ns
T _J	Operating Junction	-55 to 150		°C
T _{STG}	Storage Temperature Range			
	Pckg. Mounting Surface Temp.	300 (for 5s)		
	Weight	0.89 (Typical)		

For footnotes refer to the last page

Electrical Characteristics For Each N-Channel Device @ T_j = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	V _{GS} = 0V, I _D = 1.0mA
ΔBV _{DSS} /ΔT _J	Temperature Coefficient of Breakdown Voltage	—	0.13	—	V/°C	Reference to 25°C, I _D = 1.0mA
R _{DS(on)}	Static Drain-to-Source On-State Resistance	—	—	0.31	Ω	V _{GS} = 12V, I _D = 4.6A ④
		—	—	0.27		V _{GS} = 12V, I _D = 2.9A
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 1.0mA
g _{fs}	Forward Transconductance	3.3	—	—	S (r)	V _{DS} > 15V, I _{DS} = 2.9A ④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	10	μA	V _{DS} = 80V, V _{GS} = 0V
		—	—	25		V _{DS} = 80V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V _{GS} = 20V
I _{GSS}	Gate-to-Source Leakage Reverse	—	—	-100		V _{GS} = -20V
Q _g	Total Gate Charge	—	—	13	nC	V _{GS} = 12V, I _D = 4.6A
Q _{gs}	Gate-to-Source Charge	—	—	4.0		V _{DS} = 50V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	3.9		
t _{d(on)}	Turn-On Delay Time	—	—	20	ns	V _{DD} = 50V, I _D = 4.6A, V _{GS} = 12V, R _G = 7.5Ω
t _r	Rise Time	—	—	24		
t _{d(off)}	Turn-Off Delay Time	—	—	32		
t _f	Fall Time	—	—	90		
LS + LD	Total Inductance	—	6.1	—	nH	Measured from the center of drain pad to center of source pad
C _{iss}	Input Capacitance	—	371	—	pF	V _{GS} = 0V, V _{DS} = 25V
C _{oss}	Output Capacitance	—	108	—		f = 1.0MHz
C _{rss}	Reverse Transfer Capacitance	—	3.0	—		

Source-Drain Diode Ratings and Characteristics (Per Die)

	Parameter	Min	Typ	Max	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	4.6	A	
I _{SM}	Pulse Source Current (Body Diode) ①	—	—	18.4		
V _{SD}	Diode Forward Voltage	—	—	1.2	V	T _j = 25°C, I _S = 4.6A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	—	173	nS	T _j = 25°C, I _F = 4.6A, di/dt ≤ 100A/μs
Q _{RR}	Reverse Recovery Charge	—	—	863	nC	V _{DD} ≤ 50V ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by LS + LD.				

Thermal Resistance (Per Die)

	Parameter	Min	Typ	Max	Units	Test Conditions
R _{thJC}	Junction-to-Case	—	—	11.8	°C/W	
R _{thJA}	Junction-to-Ambient	—	—	60		Typical socket mount

Note: Corresponding Spice and Saber models are available on the G&S Website.

For footnotes refer to the last page

Electrical Characteristics For Each P-Channel Device @ T_j = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
B _V D _{SS}	Drain-to-Source Breakdown Voltage	-100	—	—	V	V _{GS} = 0V, I _D = -1.0mA
ΔB _V D _{SS} /ΔT _J	Temperature Coefficient of Breakdown Voltage	—	-0.13	—	V/°C	Reference to 25°C, I _D = -1.0mA
R _{DS(on)}	Static Drain-to-Source On-State Resistance	—	—	1.2 0.96	Ω	V _{GS} = -12V, I _D = -2.8A ④ V _{GS} = -12V, I _D = -1.8A
V _{GS(th)}	Gate Threshold Voltage	-2.0	—	-4.0	V	V _{DS} = V _{GS} , I _D = -1.0mA
g _{fs}	Forward Transconductance	1.9	—	—	S (r)	V _{DS} > -15V, I _{DS} = -1.8A ④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	-10 -25	μA	V _{DS} = -80V, V _{GS} = 0V V _{DS} = -80V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	V _{GS} = -20V
I _{GSS}	Gate-to-Source Leakage Reverse	—	—	100	nA	V _{GS} = 20V
Q _g	Total Gate Charge	—	—	11	nC	V _{GS} = -12V, I _D = -2.8A V _{DS} = -50V
Q _{gs}	Gate-to-Source Charge	—	—	3.0	nC	
Q _{gd}	Gate-to-Drain ('Miller') Charge	—	—	4.2	nC	
t _{d(on)}	Turn-On Delay Time	—	—	20	ns	V _{DD} = -50V, I _D = -2.8A, V _{GS} = -12V, R _G = 7.5Ω
t _r	Rise Time	—	—	24	ns	
t _{d(off)}	Turn-Off Delay Time	—	—	32	ns	
t _f	Fall Time	—	—	90	ns	
L _S + L _D	Total Inductance	—	6.1	—	nH	Measured from the center of drain pad to center of source pad
C _{iss}	Input Capacitance	—	377	—	pF	V _{GS} = 0V, V _{DS} = -25V f = 1.0MHz
C _{oss}	Output Capacitance	—	102	—	pF	
C _{rss}	Reverse Transfer Capacitance	—	7.0	—	pF	

Source-Drain Diode Ratings and Characteristics (Per Die)

	Parameter	Min	Typ	Max	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	-2.8	A	
I _{SM}	Pulse Source Current (Body Diode) ①	—	—	-11.2	A	
V _{SD}	Diode Forward Voltage	—	—	-5.0	V	T _J = 25°C, I _S = -2.8A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	—	138	nS	T _J = 25°C, I _F = -2.8A, di/dt ≤ -100A/μs
Q _{RR}	Reverse Recovery Charge	—	—	555	nC	V _{DD} ≤ -50V ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .				

Thermal Resistance (Per Die)

	Parameter	Min	Typ	Max	Units	Test Conditions
R _{thJC}	Junction-to-Case	—	—	11.8	°C/W	
R _{thJA}	Junction-to-Ambient	—	—	60	°C/W	Typical socket mount

For footnotes refer to the last page

IRHQ567110

Pre-Irradiation

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table 1. Electrical Characteristics For Each N-Channel Device @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

	Parameter	100K Rads(Si) ¹		300K Rads(Si) ²		Units	Test Conditions
		Min	Max	Min	Max		
BV _{DSS}	Drain-to-Source Breakdown Voltage	100	—	100	—	V	V _{GS} = 0V, I _D = 1.0mA
V _{GS(th)}	Gate Threshold Voltage	2.0	4.0	2.0	4.0		V _{GS} = V _{DS} , I _D = 1.0mA
I _{GSS}	Gate-to-Source Leakage Forward	—	100	—	100	nA	V _{GS} = 20V
I _{GSS}	Gate-to-Source Leakage Reverse	—	-100	—	-100		V _{GS} = -20 V
I _{DSS}	Zero Gate Voltage Drain Current	—	10	—	10	μA	V _{DS} = 80V, V _{GS} = 0V
R _{DS(on)}	Static Drain-to-Source ④ On-State Resistance (TO-39)	—	0.226	—	0.246	Ω	V _{GS} = 12V, I _D = 2.9A
R _{DS(on)}	Static Drain-to-Source ④ On-State Resistance (LCC-28)	—	0.27	—	0.29	Ω	V _{GS} = 12V, I _D = 2.9A
V _{SD}	Diode Forward Voltage ④	—	1.2	—	1.2	V	V _{GS} = 0V, I _S = 4.6A

1. Part number IRHQ567110

2. Part number IRHQ563110

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Single Event Effect Safe Operating Area (Per Die)

Ion	LET MeV/(mg/cm ²)	Energy (MeV)	Range (μm)	V _{DS} (V)					
				@ V _{GS} =0V	@ V _{GS} =-5V	@ V _{GS} =-8V	@ V _{GS} =-10V	@ V _{GS} =-15V	@ V _{GS} =-20V
Br	36.7	309	39.5	100	100	100	100	100	100
I	59.8	341	32.5	100	100	100	100	35	25
Au	82.3	350	28.4	100	100	100	80	25	—

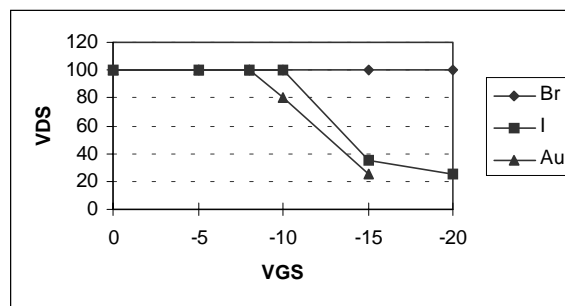


Fig a. Single Event Effect, Safe Operating Area

For footnotes refer to the last page

Pre-Irradiation

IRHQ567110

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table 1. Electrical Characteristics For Each P-Channel Device @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

	Parameter	100K Rads(Si) ¹		300K Rads(Si) ²		Units	Test Conditions
		Min	Max	Min	Max		
BV _{DSS}	Drain-to-Source Breakdown Voltage	-100	—	-100	—	V	V _{GS} = 0V, I _D = -1.0mA
V _{GS(th)}	Gate Threshold Voltage	-2.0	-4.0	-2.0	-4.0		V _{GS} = V _{DS} , I _D = -1.0mA
I _{GSS}	Gate-to-Source Leakage Forward	—	-100	—	-100	nA	V _{GS} = -20V
I _{GSS}	Gate-to-Source Leakage Reverse	—	100	—	100		V _{GS} = 20 V
I _{DSS}	Zero Gate Voltage Drain Current	—	-10	—	-10	μA	V _{DS} = -80V, V _{GS} = 0V
R _{DS(on)}	Static Drain-to-Source ④ On-State Resistance (TO-39)	—	0.916	—	0.936	Ω	V _{GS} = -12V, I _D = -1.8A
R _{DS(on)}	Static Drain-to-Source ④ On-State Resistance (LCC-28)	—	0.96	—	0.98	Ω	V _{GS} = -12V, I _D = -1.8A
V _{SD}	Diode Forward Voltage ④	—	-5.0	—	-5.0	V	V _{GS} = 0V, I _S = -2.8A

1. Part number IRHQ567110

2. Part number IRHQ563110

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Single Event Effect Safe Operating Area (Per Die)

Ion	LET MeV/(mg/cm ²)	Energy (MeV)	Range (μm)	V _{DS} (V)					
				@ V _{GS} =0V	@ V _{GS} =5V	@ V _{GS} =10V	@ V _{GS} =15V	@ V _{GS} =17.5V	@ V _{GS} =20V
Br	37.3	285	36.8	-100	-100	-100	-100	-100	-100
I	59.9	344	32.7	-100	-100	-100	-100	-75	-25
Au	82.3	351	28.5	-100	-100	-100	-30	—	—

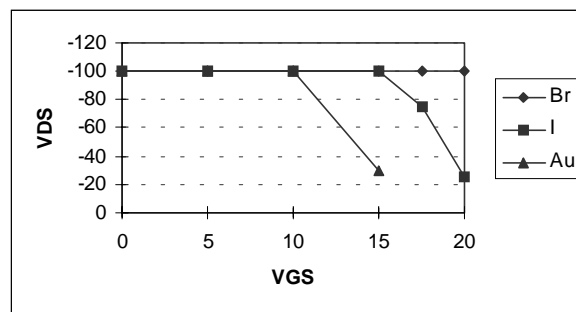
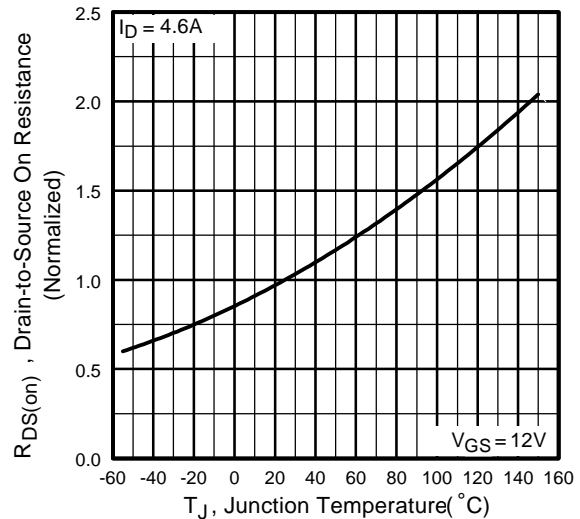
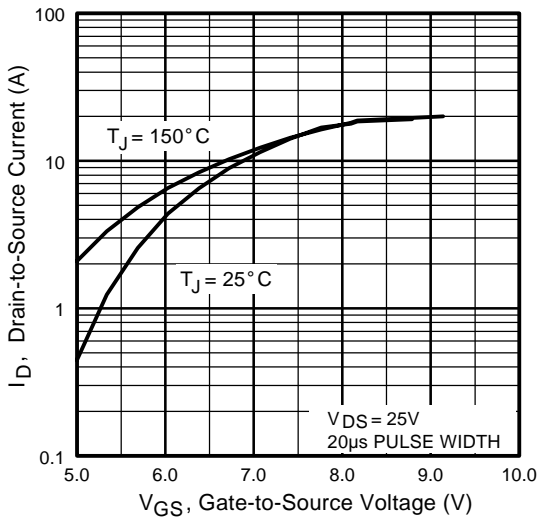
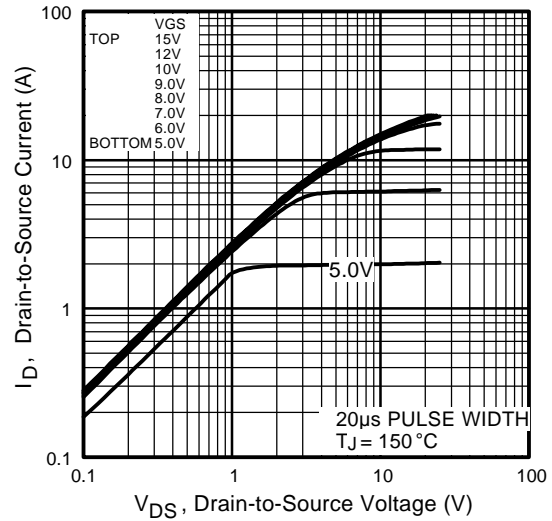
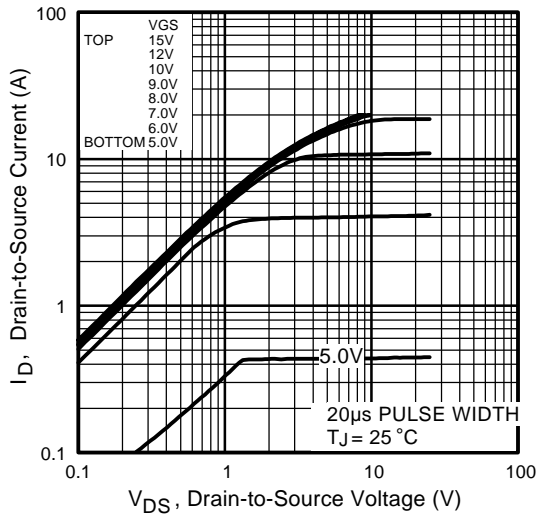


Fig a. Single Event Effect, Safe Operating Area

For footnotes refer to the last page

N-Channel Q1,Q4



N-Channel Q1,Q4

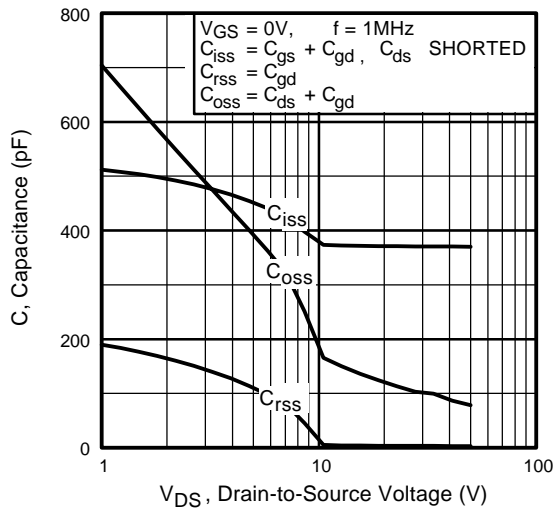


Fig 5. Typical Capacitance Vs.
Drain-to-Source Voltage

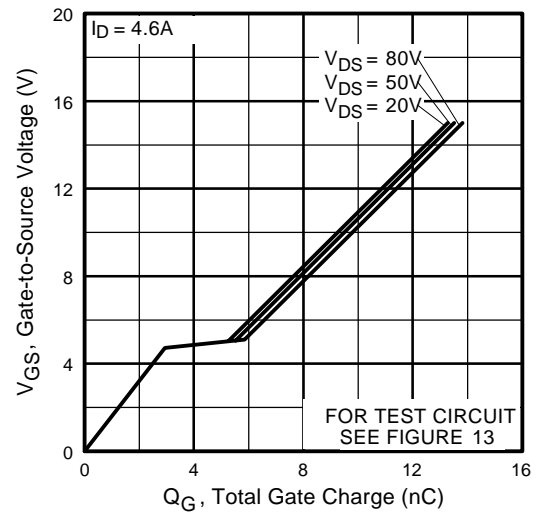


Fig 6. Typical Gate Charge Vs.
Gate-to-Source Voltage

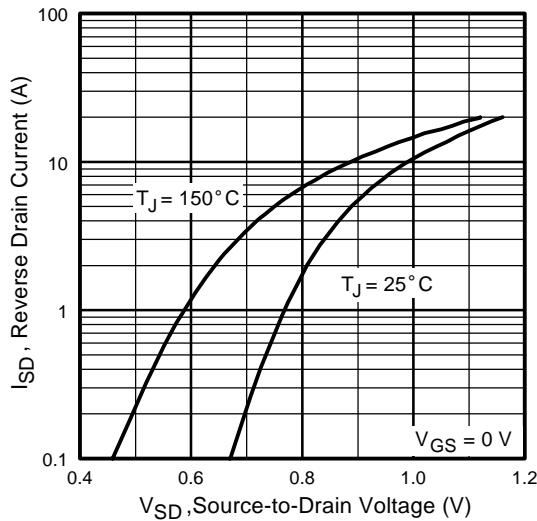


Fig 7. Typical Source-Drain Diode
Forward Voltage

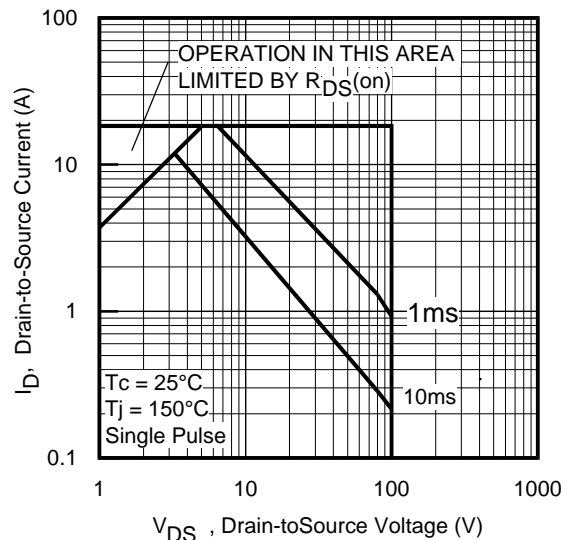


Fig 8. Maximum Safe Operating Area

N-Channel Q1,Q4

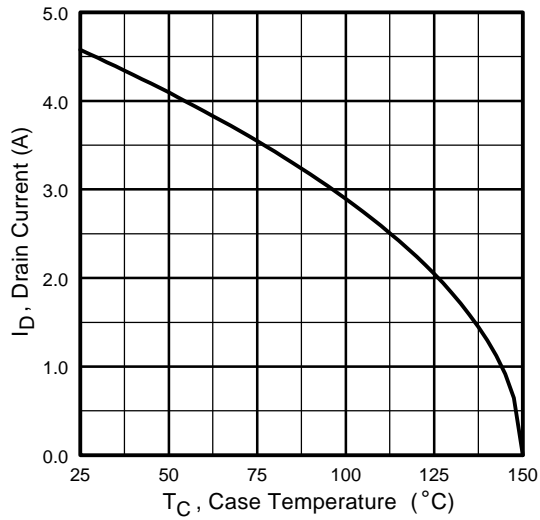


Fig 9. Maximum Drain Current Vs. Case Temperature

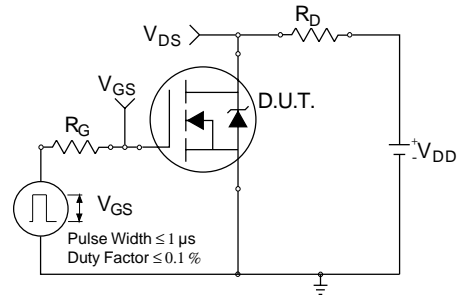


Fig 10a. Switching Time Test Circuit

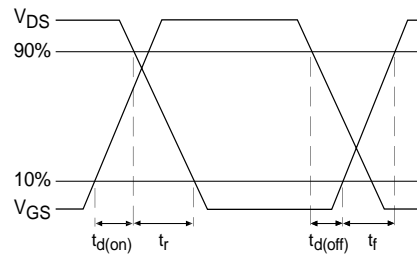


Fig 10b. Switching Time Waveforms

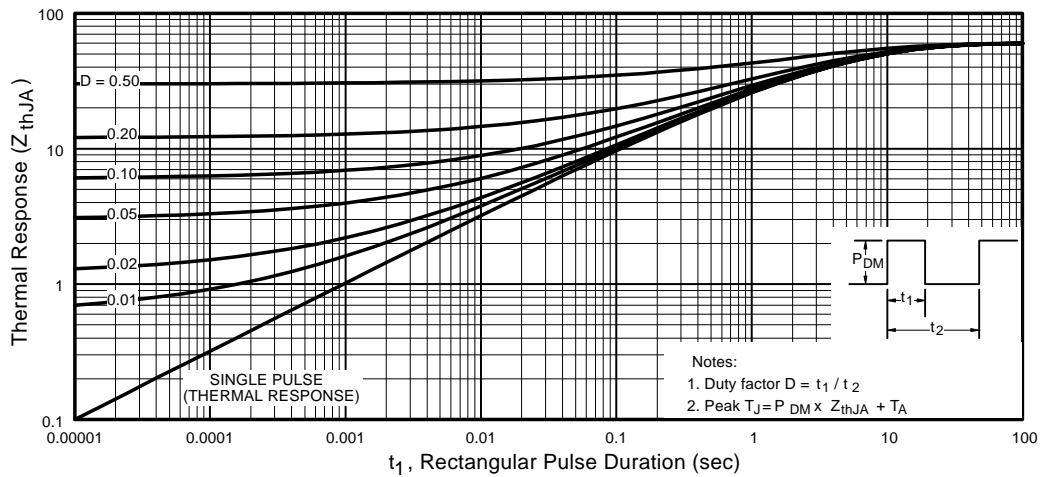


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

P-Channel Q2,Q3

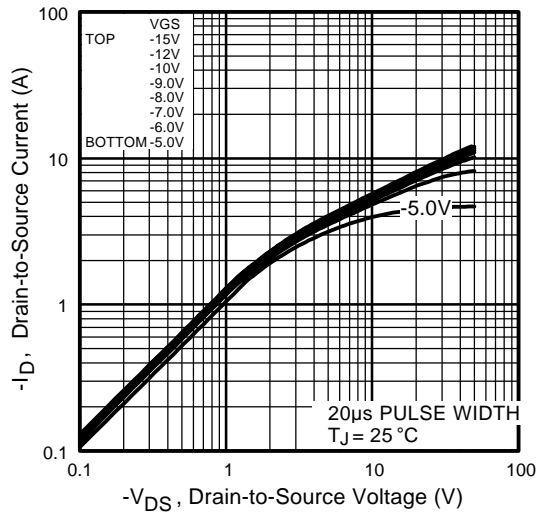


Fig 1. Typical Output Characteristics

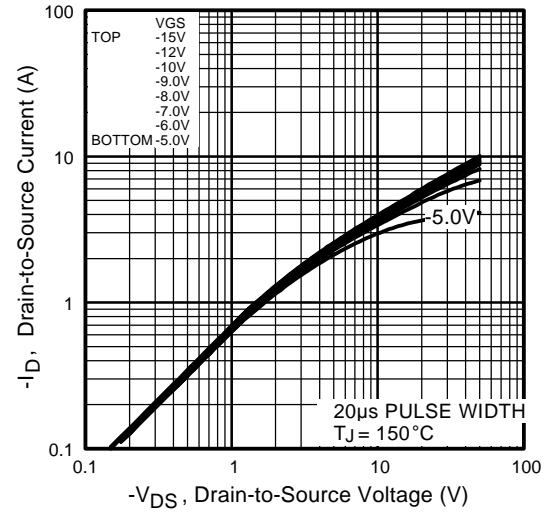


Fig 2. Typical Output Characteristics

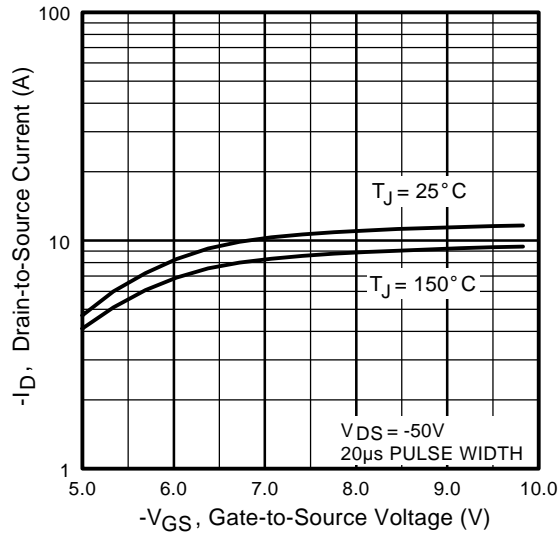


Fig 3. Typical Transfer Characteristics

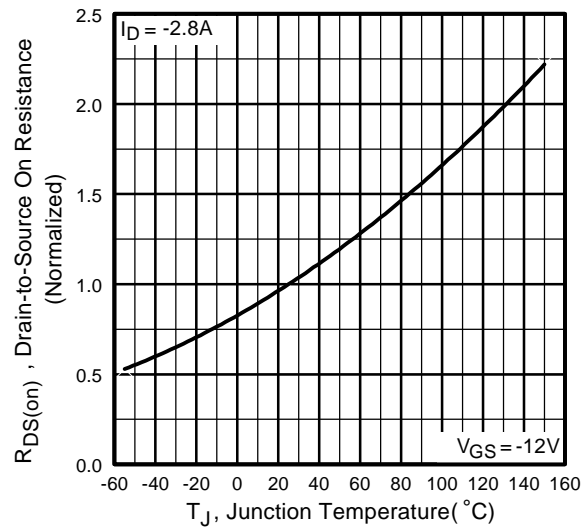


Fig 4. Normalized On-Resistance
Vs. Temperature

P-Channel Q2,Q3

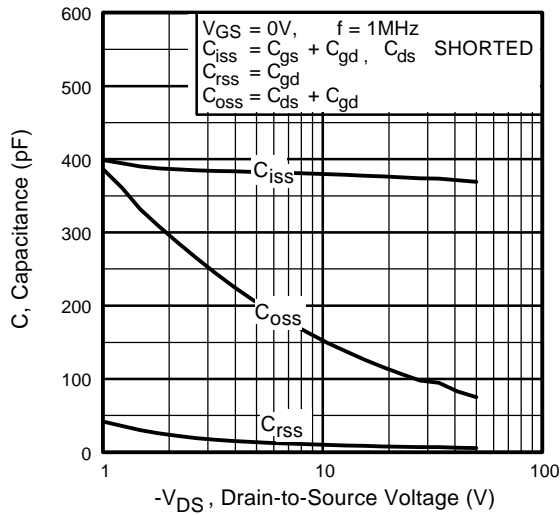


Fig 5. Typical Capacitance Vs.
Drain-to-Source Voltage

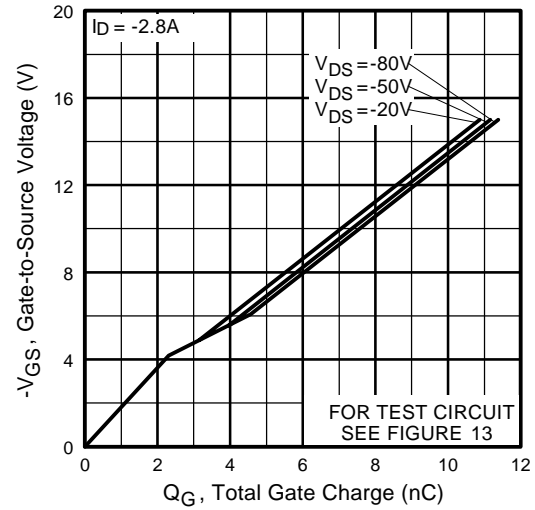


Fig 6. Typical Gate Charge Vs.
Gate-to-Source Voltage

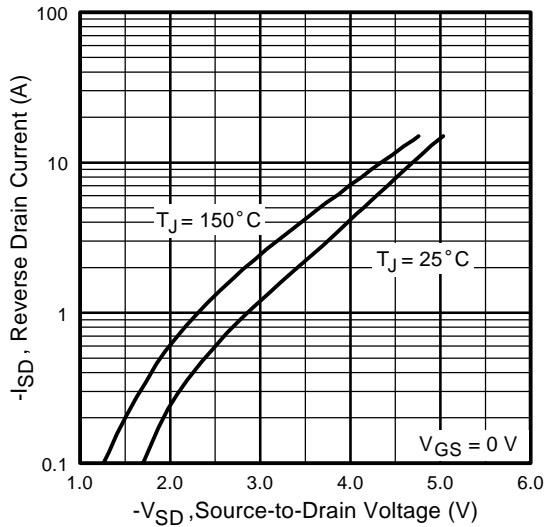


Fig 7. Typical Source-Drain Diode
Forward Voltage

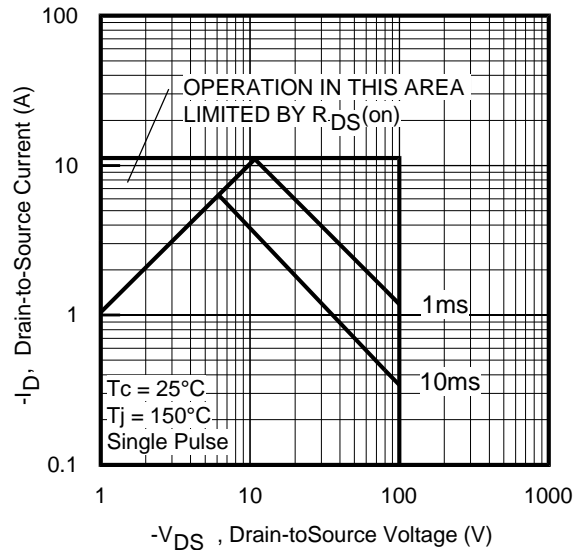


Fig 8. Maximum Safe Operating Area

P-Channel Q2,Q3

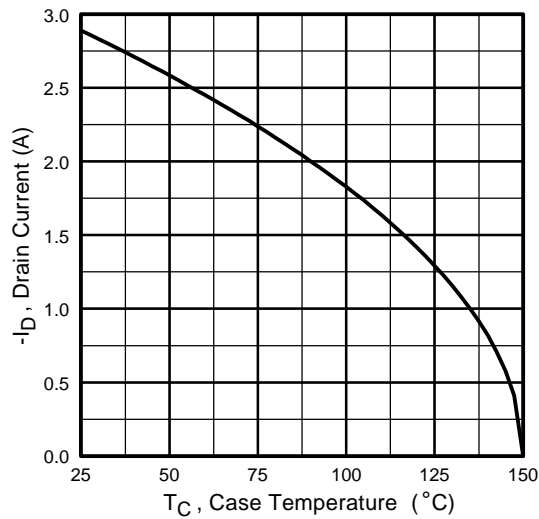


Fig 9. Maximum Drain Current Vs. Case Temperature

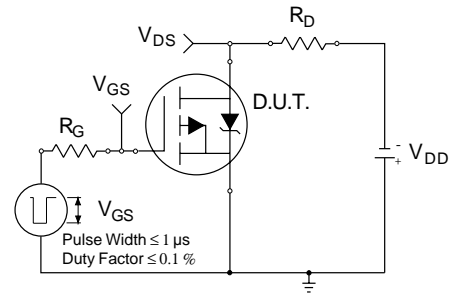


Fig 10a. Switching Time Test Circuit

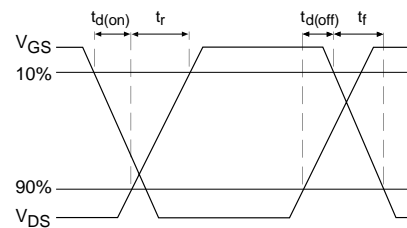


Fig 10b. Switching Time Waveforms

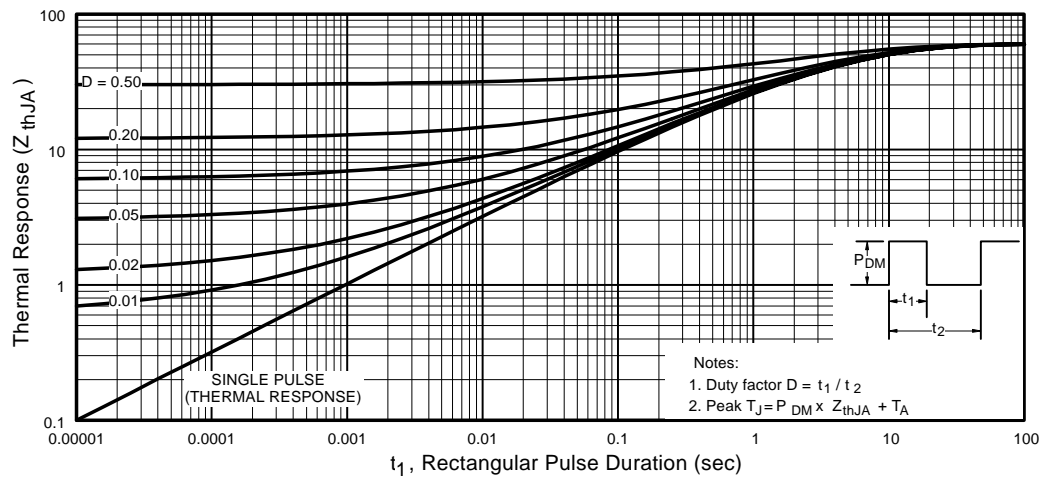


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

P-Channel Q2,Q3

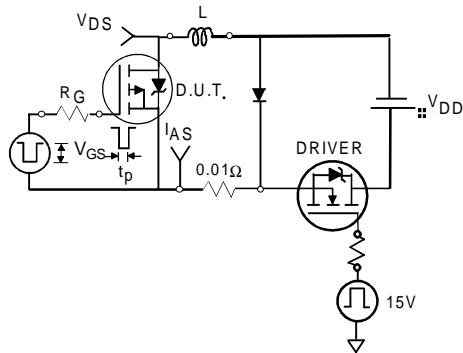


Fig 12a. Unclamped Inductive Test Circuit

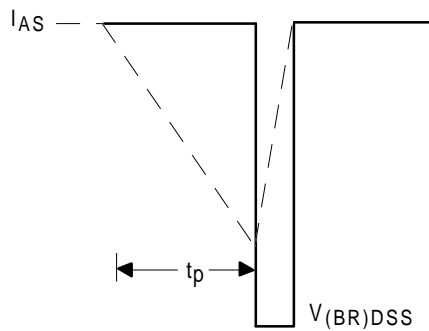


Fig 12b. Unclamped Inductive Waveforms

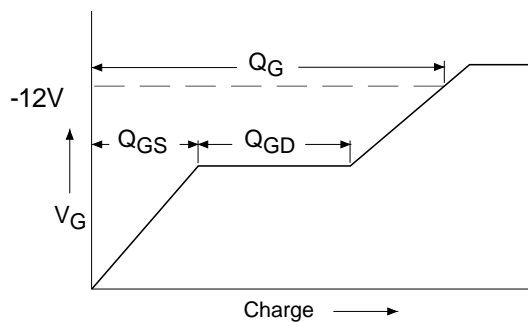


Fig 13a. Basic Gate Charge Waveform

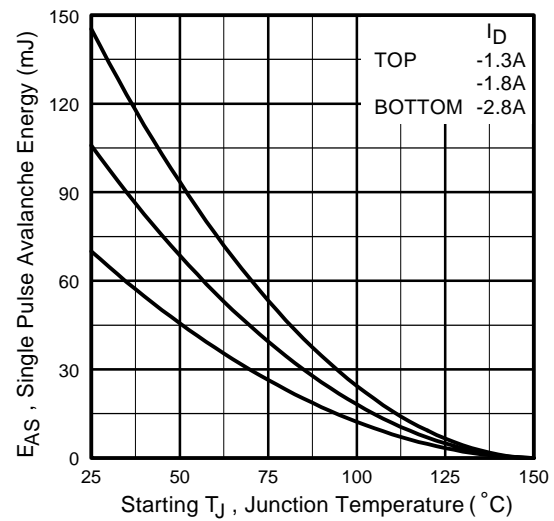


Fig 12c. Maximum Avalanche Energy
Vs. Drain Current

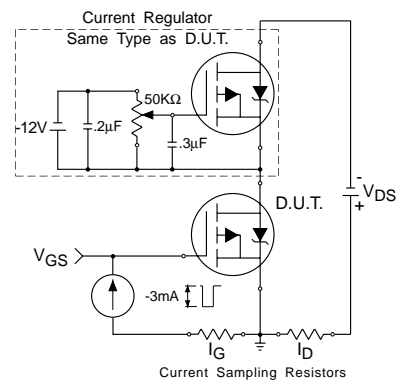
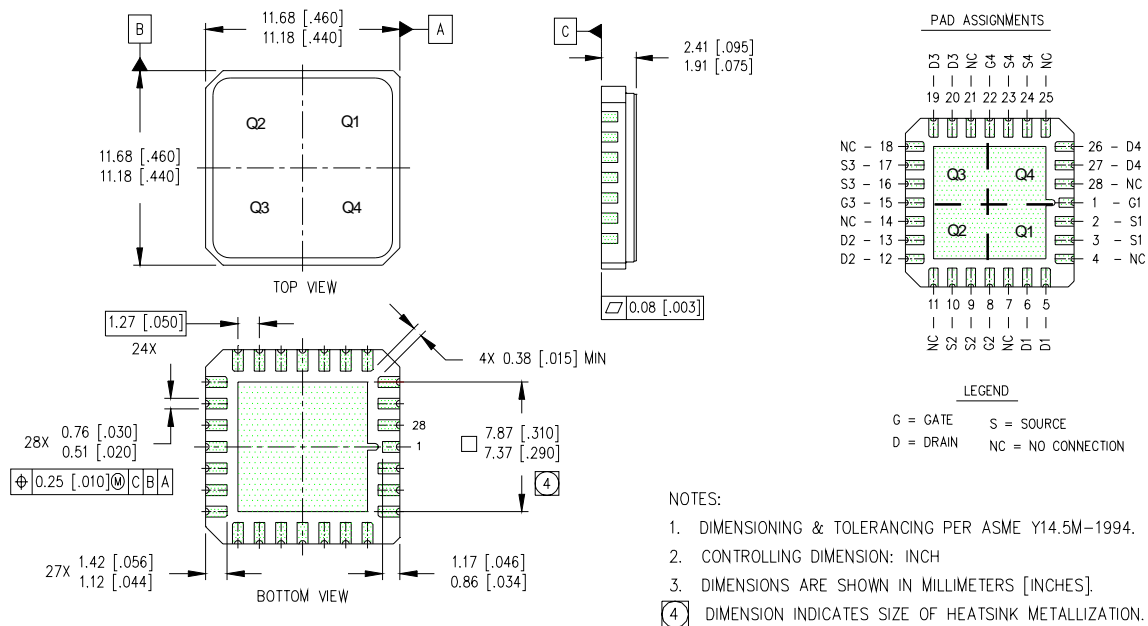


Fig 13b. Gate Charge Test Circuit

Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② $V_{DD} = 25V$, starting $T_J = 25^\circ C$, $L = 4.4mH$, Peak $I_L = 4.6A$, $V_{GS} = 12V$
- ③ $I_{SD} \leq 4.6A$, $di/dt \leq 300A/\mu s$, $V_{DD} \leq 100V$, $T_J \leq 150^\circ C$
- ④ Pulse width $\leq 300 \mu s$; Duty Cycle $\leq 2\%$
- ⑤ **Total Dose Irradiation with VGS Bias.**
12 volt V_{GS} applied and $V_{DS} = 0$ during irradiation per MIL-STD-750, method 1019, condition A
- ⑥ **Total Dose Irradiation with VDS Bias.**
80 volt V_{DS} applied and $V_{GS} = 0$ during irradiation per MIL-STD-750, method 1019, condition A
- ⑦ $V_{DD} = -25V$, starting $T_J = 25^\circ C$, $L = 17.8mH$, Peak $I_L = -2.8A$, $V_{GS} = -12V$
- ⑧ $I_{SD} \leq -2.8A$, $di/dt \leq -263A/\mu s$, $V_{DD} \leq -100V$, $T_J \leq 150^\circ C$

Case Outline and Dimensions — LCC-28

International
IR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903

Visit us at www.irf.com for sales contact information.
Data and specifications subject to change without notice. 07/01