

ST173S SERIES

INVERTER GRADE THYRISTORS

Stud Version

Features

- All diffused design
- Center amplifying gate
- Guaranteed high dv/dt
- Guaranteed high di/dt
- High surge current capability
- Low thermal impedance
- High speed performance

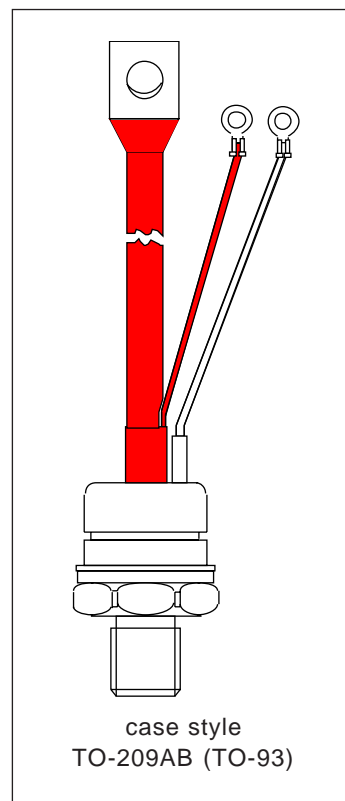
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Typical Applications

- Inverters
- Choppers
- Induction heating
- All types of force-commutated converters

Major Ratings and Characteristics

Parameters	ST173S	Units
$I_{T(AV)}$	175	A
@ T_C	85	°C
$I_{T(RMS)}$	275	A
I_{TSM} @ 50Hz	4680	A
@ 60Hz	4900	A
I^2t @ 50Hz	110	KA ² s
@ 60Hz	100	KA ² s
V_{DRM}/V_{RRM}	1000 to 1200	V
t_q range	15 to 25	μs
T_J	- 40 to 125	°C



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Bulletin I25181 rev. C 12/96

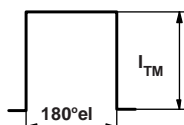
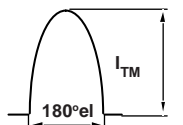
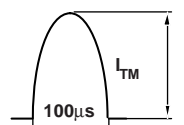
International
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ELECTRICAL SPECIFICATIONS

Voltage Ratings

Type number	Voltage Code	V_{DRM}/V_{RRM} , maximum repetitive peak voltage V	V_{RSM} , maximum non-repetitive peak voltage V	I_{DRM}/I_{RRM} max. @ $T_J = T_J$ max. mA
ST173S	10	1000	1100	40
	12	1200	1300	

Current Carrying Capability

Frequency							Units
50Hz	500	320	790	550	4510	3310	A
400Hz	450	290	810	540	1970	1350	
1000Hz	330	190	760	490	1050	680	
2500Hz	170	80	510	300	480	280	
Recovery voltage Vr	50	50	50	50	50	50	V
Voltage before turn-on Vd	V _{DRM}		V _{DRM}		V _{DRM}		
Rise of on-state current di/dt	50	50	-	-	-	-	A/µs
Case temperature	60	85	60	85	60	85	°C
Equivalent values for RC circuit	47Ω / 0.22µF		47Ω / 0.22µF		47Ω / 0.22µF		

On-state Conduction

Parameter	ST173S	Units	Conditions
$I_{T(AV)}$ Max. average on-state current @ Case temperature	175	A	180° conduction, half sine wave
	85	°C	
$I_{T(RMS)}$ Max. RMS on-state current	275	A	DC @ 75°C case temperature
I_{TSM} Max. peak, one half cycle, non-repetitive surge current	4680		t = 10ms No voltage
	4900		t = 8.3ms reappplied
	3940		t = 10ms 100% V_{RRM}
	4120		t = 8.3ms reappplied
I^2t Maximum I^2t for fusing	110	KA²s	t = 10ms No voltage
	100		t = 8.3ms reappplied
	77		t = 10ms 100% V_{RRM}
	71		t = 8.3ms reappplied
$I^2\sqrt{t}$ Maximum $I^2\sqrt{t}$ for fusing	1100	KA²√s	t = 0.1 to 10ms, no voltage reappplied

On-state Conduction

Parameter	ST173S	Units	Conditions
V_{TM} Max. peak on-state voltage	2.07	V	$I_{TM} = 600A$, $T_J = T_J \text{ max}$, $t_p = 10\text{ms}$ sine wave pulse
$V_{T(TO)1}$ Low level value of threshold voltage	1.55		$(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$, $T_J = T_J \text{ max}$.
$V_{T(TO)2}$ High level value of threshold voltage	1.58		$(I > \pi \times I_{T(AV)})$, $T_J = T_J \text{ max}$.
r_{t1} Low level value of forward slope resistance	0.87	m Ω	$(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$, $T_J = T_J \text{ max}$.
r_{t2} High level value of forward slope resistance	0.82		$(I > \pi \times I_{T(AV)})$, $T_J = T_J \text{ max}$.
I_H Maximum holding current	600	mA	$T_J = 25^\circ\text{C}$, $I_T > 30A$
I_L Typical latching current	1000		$T_J = 25^\circ\text{C}$, $V_A = 12V$, $R_a = 6\Omega$, $I_G = 1A$

Switching

Parameter	ST173S	Units	Conditions
di/dt Max. non-repetitive rate of rise of turned-on current	1000	A/ μs	$T_J = T_J \text{ max}$, $V_{DRM} = \text{rated } V_{DRM}$ $I_{TM} = 2 \times di/dt$
t_d Typical delay time	1.1	μs	$T_J = 25^\circ\text{C}$, $V_{DM} = \text{rated } V_{DRM}$, $I_{TM} = 50A$ DC, $t_p = 1\mu\text{s}$ Resistive load, Gate pulse: 10V, 5 Ω source
t_q Max. turn-off time	Min 15 Max 25		$T_J = T_J \text{ max}$, $I_{TM} = 300A$, commutating $di/dt = 20A/\mu\text{s}$ $V_R = 50V$, $t_p = 500\mu\text{s}$, dv/dt : see table in device code

Blocking

Parameter	ST173S	Units	Conditions
dv/dt Maximum critical rate of rise of off-state voltage	500	V/ μs	$T_J = T_J \text{ max}$., linear to 80% V_{DRM} , higher value available on request
I_{RRM} I_{DRM} Max. peak reverse and off-state leakage current	40	mA	$T_J = T_J \text{ max}$, rated V_{DRM}/V_{RRM} applied

Triggering

Parameter	ST173S	Units	Conditions
P_{GM} Maximum peak gate power	60	W	$T_J = T_J \text{ max}$, $f = 50\text{Hz}$, $d\% = 50$
$P_{G(AV)}$ Maximum average gate power	10		
I_{GM} Max. peak positive gate current	10	A	$T_J = T_J \text{ max}$, $t_p \leq 5\text{ms}$
$+V_{GM}$ Maximum peak positive gate voltage	20	V	$T_J = T_J \text{ max}$, $t_p \leq 5\text{ms}$
$-V_{GM}$ Maximum peak negative gate voltage	5		
I_{GT} Max. DC gate current required to trigger	200	mA	$T_J = 25^\circ\text{C}$, $V_A = 12V$, $R_a = 6\Omega$
V_{GT} Max. DC gate voltage required to trigger	3	V	
I_{GD} Max. DC gate current not to trigger	20	mA	$T_J = T_J \text{ max}$., rated V_{DRM} applied
V_{GD} Max. DC gate voltage not to trigger	0.25	V	

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Thermal and Mechanical Specifications

Parameter	ST173S	Units	Conditions
T _J Max. junction operating temperature range	-40 to 125	°C	
T _{stg} Max. storage temperature range	-40 to 150		
R _{thJC} Max. thermal resistance, junction to case	0.105	K/W	DC operation
R _{thCS} Max. thermal resistance, case to heatsink	0.04		Mounting surface, smooth, flat and greased
T Mounting torque, ± 10%	31 (275)	Nm (lbf-in)	Non lubricated threads
	24.5 (210)	Nm (lbf-in)	Lubricated threads
wt Approximate weight	280	g	
Case style	TO-209AB (TO-93)		See Outline Table

ΔR_{thJC} Conduction

(The following table shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC)

Conduction angle	Sinusoidal conduction	Rectangular conduction	Units	Conditions
180°	0.016	0.012	K/W	T _J = T _J max.
120°	0.019	0.020		
90°	0.025	0.027		
60°	0.036	0.037		
30°	0.060	0.060		

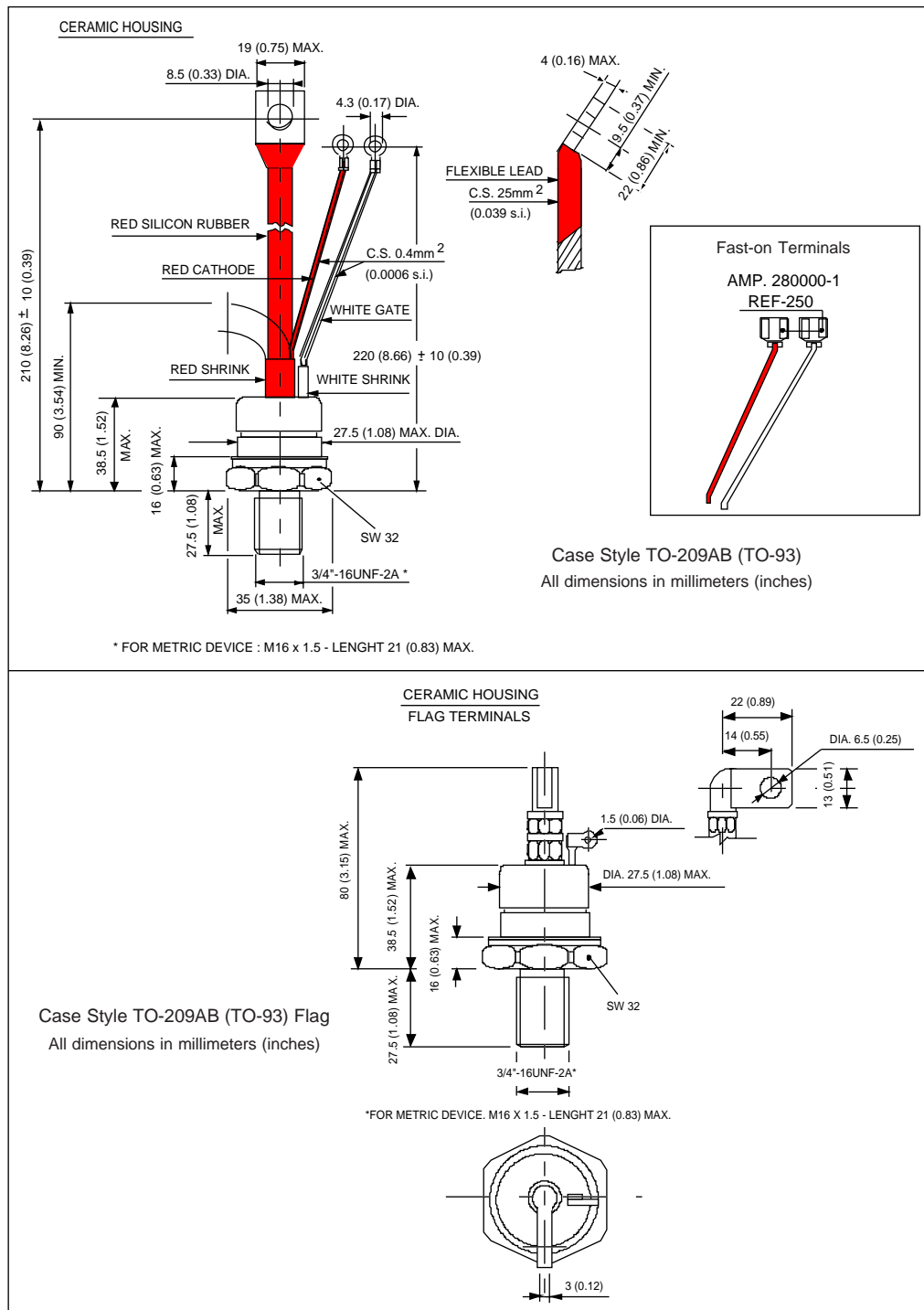
Ordering Information Table

Device Code <div style="display: flex; align-items: center; margin-top: 10px;"> <div style="border: 1px solid black; padding: 2px 5px; margin: 0 2px;">ST</div> <div style="border: 1px solid black; padding: 2px 5px; margin: 0 2px;">17</div> <div style="border: 1px solid black; padding: 2px 5px; margin: 0 2px;">3</div> <div style="border: 1px solid black; padding: 2px 5px; margin: 0 2px;">S</div> <div style="border: 1px solid black; padding: 2px 5px; margin: 0 2px;">12</div> <div style="border: 1px solid black; padding: 2px 5px; margin: 0 2px;">P</div> <div style="border: 1px solid black; padding: 2px 5px; margin: 0 2px;">F</div> <div style="border: 1px solid black; padding: 2px 5px; margin: 0 2px;">K</div> <div style="border: 1px solid black; padding: 2px 5px; margin: 0 2px;">0</div> <div style="border: 1px solid black; padding: 2px 5px; margin: 0 2px;"></div> </div> <div style="display: flex; justify-content: space-around; margin-top: 5px;"> ①②③④⑤⑥⑦⑧⑨⑩ </div>									
1	- Thyristor								
2	- Essential part number								
3	- 3 = Fast turn off								
4	- S = Compression bonding Stud								
5	- Voltage code: Code x 100 = V _{RRM} (See Voltage Ratings table)								
6	- P = Stud base 3/4" 16UNF-2A M = Stud base metric threads M16 x 1.5								
7	- Reapplied dv/dt code (for t _q test condition)								
8	- t _q code								
9	- 0 = Eyelet terminals (Gate and Aux. Cathode Leads) 1 = Fast-on terminals (Gate and Aux. Cathode Leads) 2 = Flag terminals (For Cathode and Gate Terminals)								
10	- Critical dv/dt: None = 500V/μsec (Standard value) L = 1000V/μsec (Special selection)								

dv/dt - t _q combinations available					
dv/dt (V/μs)	20	50	100	200	400
15	CL	--	--	--	--
18	CP	DP	EP	FP *	--
20	CK	DK	EK	FK *	HK
25	CJ	DJ	EJ	FJ	HJ
30	--	DH	EH	FH	HH

*Standard part number.
All other types available only on request.

Outline Table



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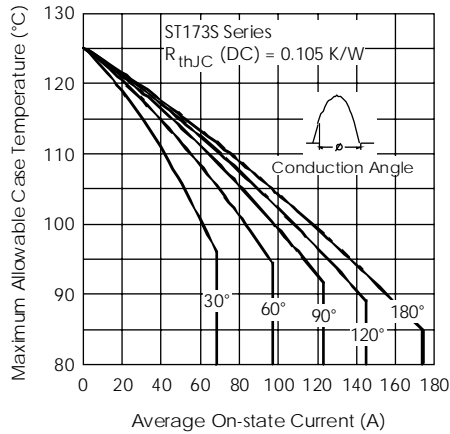


Fig. 1 - Current Ratings Characteristics

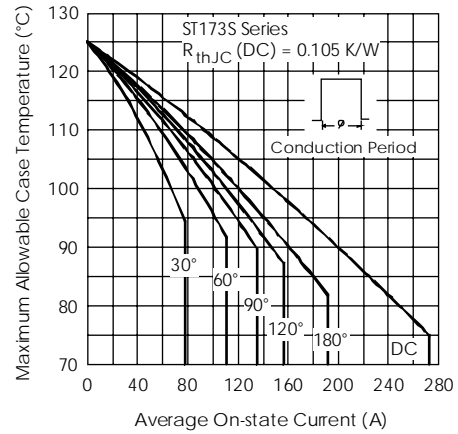


Fig. 2 - Current Ratings Characteristics

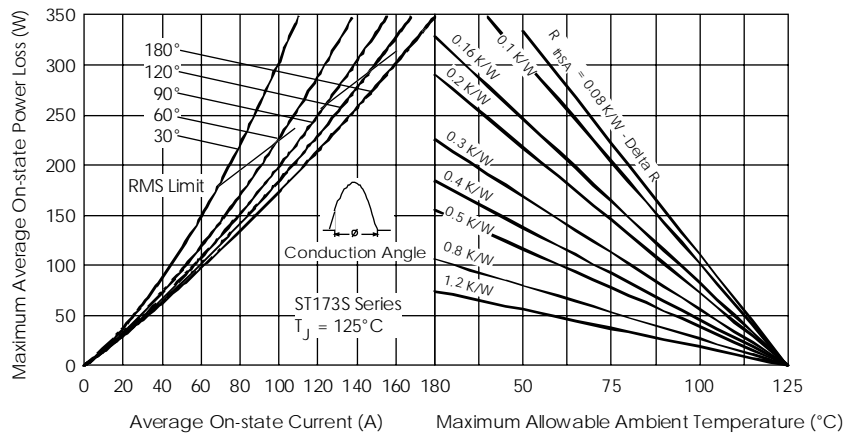


Fig. 3 - On-state Power Loss Characteristics

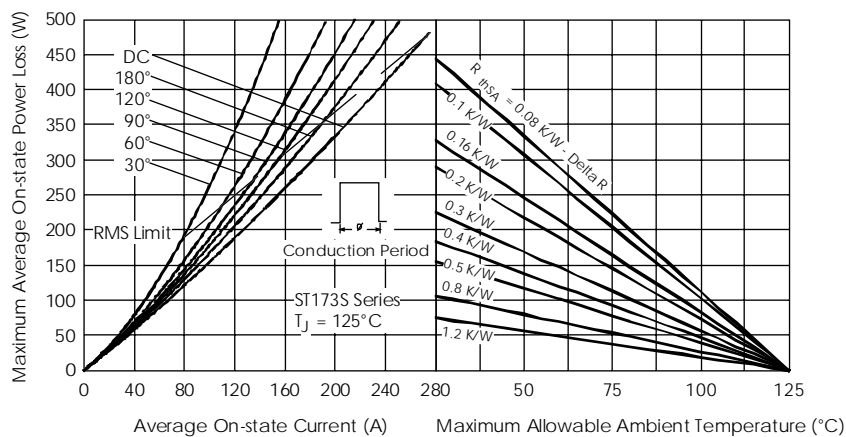


Fig. 4 - On-state Power Loss Characteristics

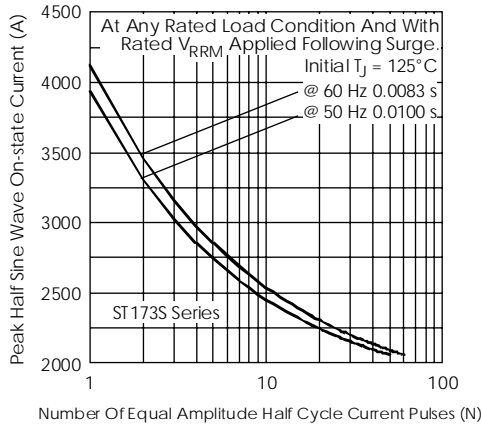


Fig. 5 - Maximum Non-repetitive Surge Current

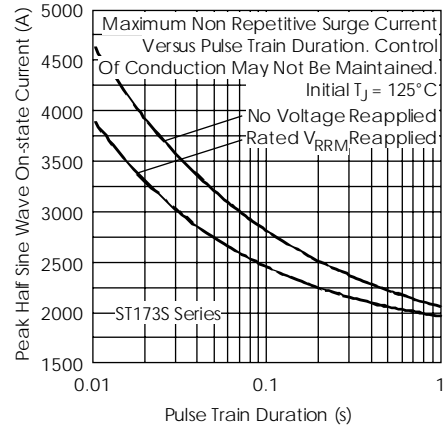


Fig. 6 - Maximum Non-repetitive Surge Current

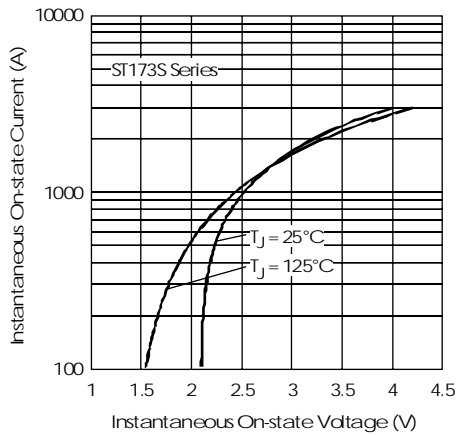


Fig. 7 - On-state Voltage Drop Characteristics

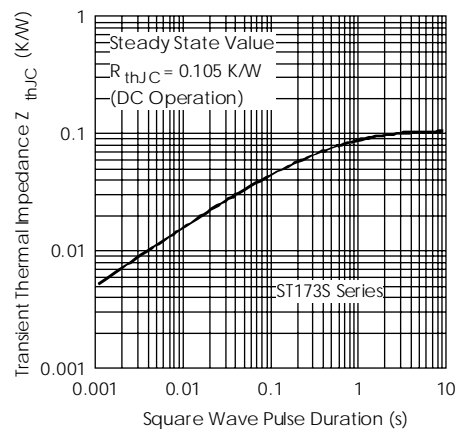


Fig. 8 - Thermal Impedance Z_{thJC} Characteristic

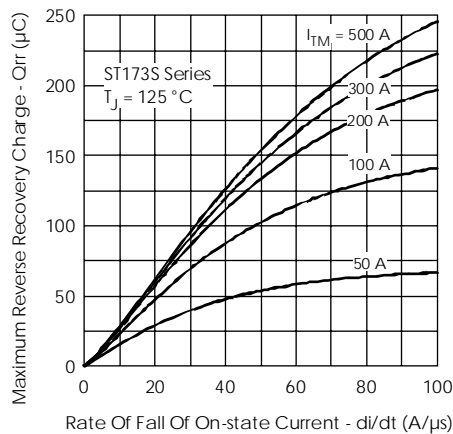


Fig. 9 - Reverse Recovered Charge Characteristics

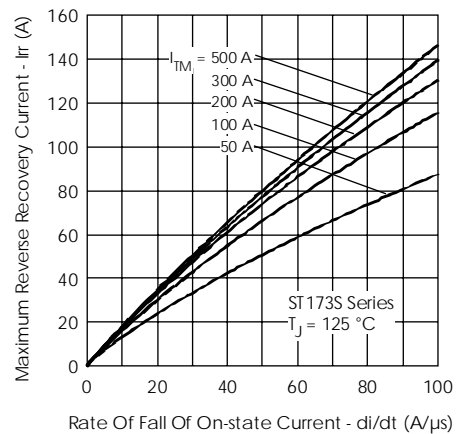


Fig. 10 - Reverse Recovery Current Characteristics

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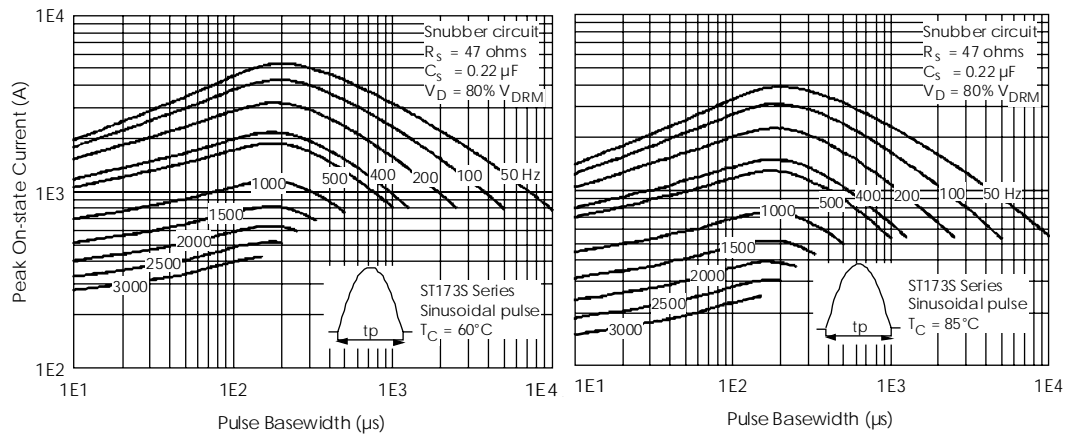


Fig. 11 - Frequency Characteristics

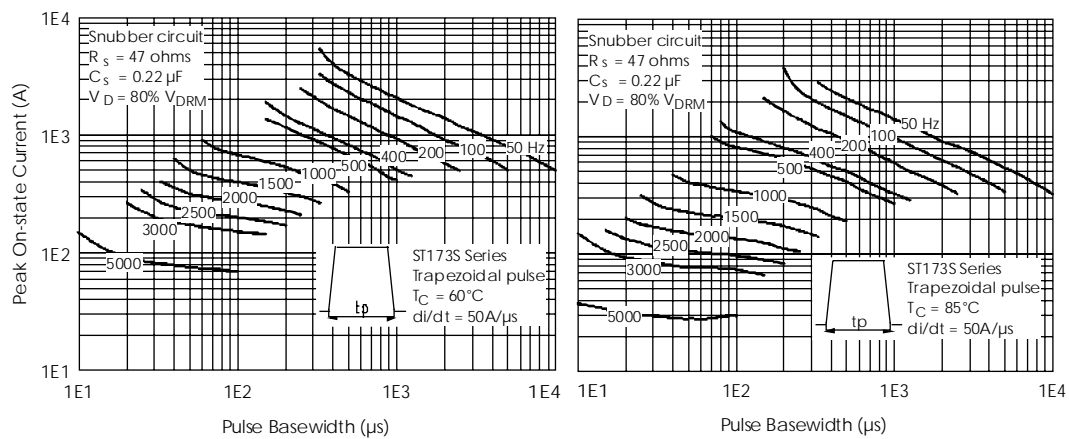


Fig. 12 - Frequency Characteristics

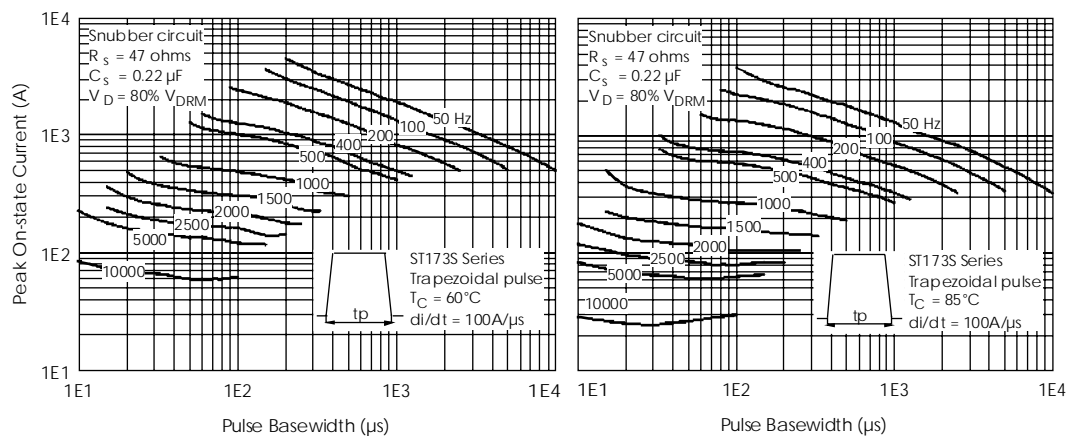


Fig. 13 - Frequency Characteristics

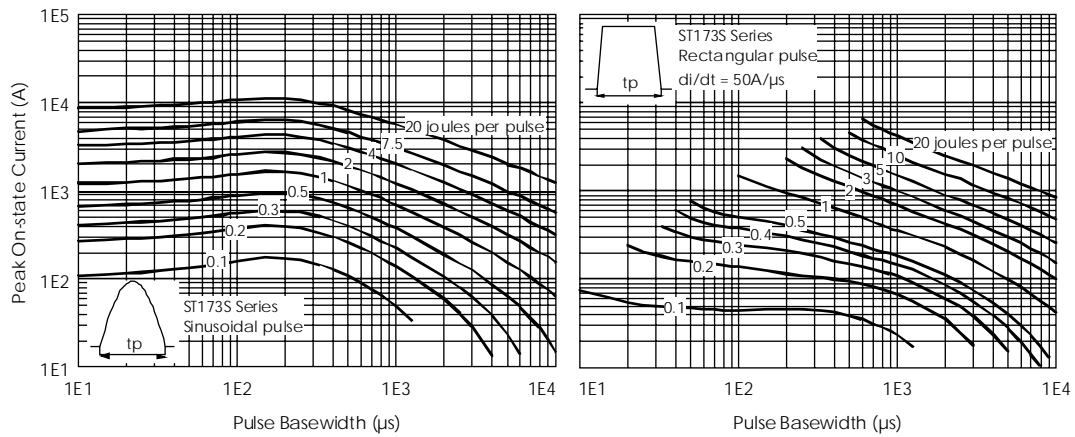


Fig. 14 - Maximum On-state Energy Power Loss Characteristics

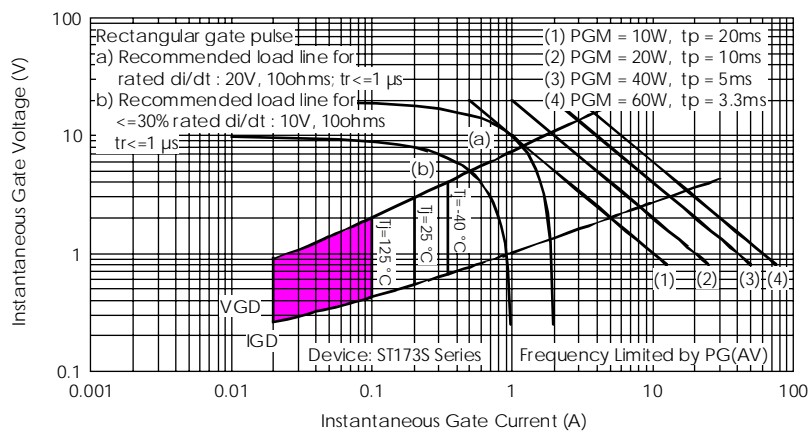


Fig. 15 - Gate Characteristics