2k-bit 2-WIRE SERIAL CMOS EEPROM with Permanent Write-Protection

ADVANCED INFORMATION
JANUARY 2004

FEATURES

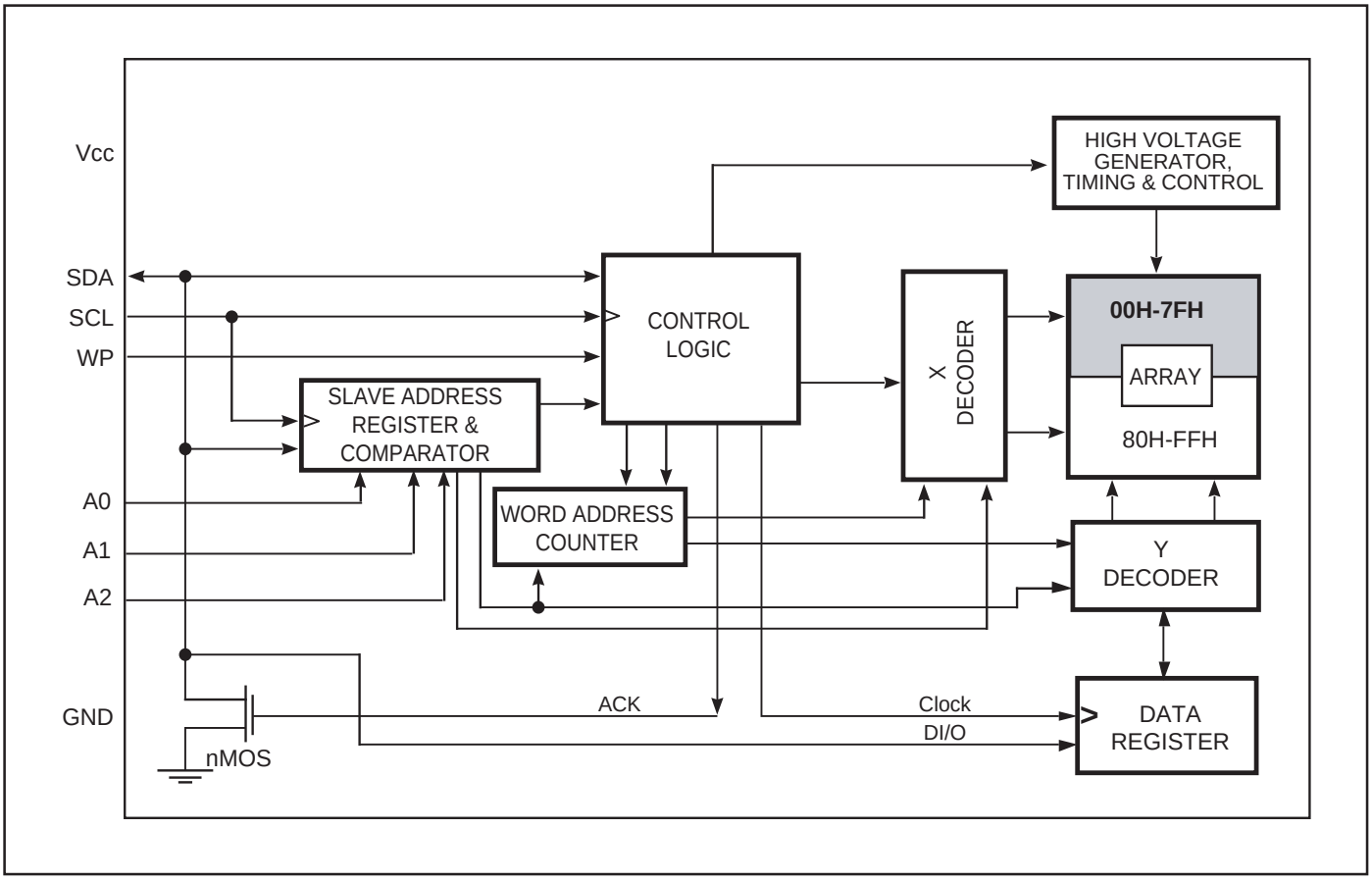
- Two-Wire Serial Interface
  - – Bidirectional data transfer protocol
  - – 400 kHz (I^2C ™ Protocol) Compatibility
- Organization:
  - – 256-bit x 8-bit
- Data Protection Features
  - – Write Protect Pin
  - – Permanent Software Protection
- 16-Byte Page Write Buffer
  - – Partial Page-writes permitted
- Low Power CMOS Technology
  - – Active Current less than 2 mA (5V)
  - – Standby Current less than 6 µA (5V)
  - – Standby Current less than 2 µA (2.5V)
- Low Voltage Operation
  - – IS24C52-2: Vcc = 1.8V to 5.5V
  - – IS24C52-3: Vcc = 2.5V to 5.5V
- Random or Sequential Read Modes
- Filtered Inputs for Noise Suppression
- Self timed Write cycle with auto clear
  - – 5 ms @ 2.5V
- High Reliability
  - – Endurance: 1,000,000 Cycles
  - – Data Retention: 40 Years
- Commercial and Industrial temperature ranges
- 8-pin SOIC, 8-pin TSSOP, and 8-pin MSOP

DESCRIPTION

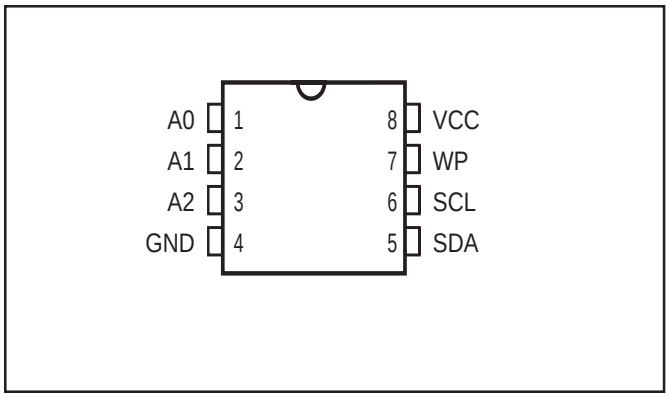
The IS24C52 is an electrically erasable PROM device that uses the standard 2-wire interface for communications. The IS24C52 contains a memory array of 2,048-bits (256K x 8), and is further subdivided into 16 pages of 16 bytes each for page-write mode. The software write-protection feature is initiated with a unique irreversible instruction. After this command is transmitted, the first 128 bytes of the array become permanently read-only. This feature is popular in applications like DRAM DIMMs to retain DRAM related data. This EEPROM is offered in wide operating voltages of 1.8V to 5.5V (IS24C52-2) and 2.5V to 5.5V (IS24C52-3) to be compatible with most application voltages. ISSI designed the IS24C52 as a low-cost and low-power 2-wire EEPROM solution. The devices are packaged in 8-pin SOIC, and 8-pin TSSOP, and 8-pin MSOP.

The IS24C52 maintains compatibility with the popular 2-wire bus protocol, so it is easy to use in applications implementing this bus type. The simple bus consists of the Serial Clock wire (SCL) and the Serial Data wire (SDA). Using the bus, a Master device such as a microcontroller is usually connected to one or more Slave devices such as the IS24C52. The bit stream over the SDA line includes a series of bytes, which identifies a particular Slave device, an instruction, an address within that Slave device, and a series of data, if appropriate. The IS24C52 has a Write Protect pin (WP) to allow blocking of any write instruction transmitted over the bus.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION
8-Pin SOIC, TSSOP, MSOP



PIN DESCRIPTIONS

A0-A2	Address Inputs
SDA	Serial Address/Data I/O
SCL	Serial Clock Input
WP	Write Protect Input
Vcc	Power Supply
GND	Ground

SCL

This input clock pin is used to synchronize the data transfer to and from the device.

SDA

The SDA is a Bi-directional pin used to transfer addresses and data into and out of the device. The SDA pin is an open drain output and can be wire Or'ed with other open drain or open collector outputs. The SDA bus *requires* a pullup resistor to Vcc.

A0, A1, A2

The A0, A1, and A2 are the device address inputs that are hardwired or left unconnected for hardware flexibility. When pins are hardwired, as many as eight devices may be addressed on a single bus system. When the pins are not hardwired, the default A0, A1, and A2 are zero.

WP

WP is the Write Protect pin. If the WP pin is tied to Vcc, the entire array becomes Write Protected, and software write-protection cannot be initiated. When WP is tied to GND or left floating, normal read/write operations are allowed to the device. If the device has already received a write-protection command, the memory in the range of 00h-7Fh is read -only regardless of the setting of the WP pin.

DEVICE OPERATION

The IS24C52 features a serial communication and supports a bi-directional 2-wire bus transmission protocol.

2-WIRE BUS

The two-wire bus is defined as a Serial Data line (SDA), and a Serial Clock line (SCL). The protocol defines any device that sends data onto the SDA bus as a transmitter, and the receiving devices as a receiver. The bus is controlled by Master device which generates the SCL, controls the bus access and generates the Stop and Start conditions. The IS24C52 is the Slave device on the bus.

The Bus Protocol:

– Data transfer may be initiated only when the bus is not busy

– During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a Start or Stop condition.

The state of the data line represents valid data after a Start condition. The data line must be stable for the duration of the High period of the clock signal. The data on the SDA line may be changed during the Low period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a Start condition and terminated with a Stop condition.

Start Condition

The Start condition precedes all commands to the device and is defined as a High to Low transition of SDA when SCL is High. The IS24C52 monitors the SDA and SCL lines and will not respond until the Start condition is met.

Stop Condition

The Stop condition is defined as a Low to High transition of SDA when SCL is High. All operations must end with a Stop condition.

Acknowledge (ACK)

After a successful data transfer, each receiving device is required to generate an ACK. The Acknowledging device pulls down the SDA line.

Reset

The IS24C52 contains a reset function in case the 2-wire bus transmission is accidentally interrupted (eg. a power loss), or needs to be terminated mid-stream. The reset is caused when the Master device creates a Start condition. To do this, it may be necessary for the Master device to monitor the SDA line while cycling the SCL up to nine times. (For each clock signal transition to High, the Master checks for a High level on SDA.)

Standby Mode

Power consumption in reduced in standby mode. The IS24C52 will enter standby mode: a) At Power-up, and remain in it until SCL or SDA toggles; b) Following the Stop signal if no write operation is initiated; or c) Following any internal write operation

DEVICE ADDRESSING

The Master begins a transmission by sending a Start condition. The Master then sends the address of the particular Slave devices it is requesting. The Slave (Fig. 5) address is 8 bits.

The four most significant bits of the device address are fixed as 1010 for normal read/write operations, and 0110 for permanent write-protection operations.

This device has three address bits (A1, A2, and A0) that allow up to eight IS24C52 devices to share the 2-wire bus. Upon receiving the Slave address, the device compares the three address bits with the hardwired A2, A1, and A0 input pins to determine if it is the appropriate Slave. If any of the A2 - A0 pins is neither biased to High nor Low, then internal circuitry defaults the value to Low.

The last bit of the Slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, a Read operation is selected, and when set to 0, a Write operation is selected.

After the Master transmits the Start condition and Slave address byte (Fig. 5), the appropriate 2-wire Slave (eg. IS24C52) will respond with ACK on the SDA line. The Slave will pull down the SDA on the ninth clock cycle, signaling that it received the eight bits of data. The selected IS24C52 then prepares for a Read or Write operation by monitoring the bus.

WRITE OPERATION

Byte Write

In the Byte Write mode, the Master device sends the Start condition and the Slave address information (with the R/$\overline{W}$ set to Zero) to the Slave device. After the Slave generates an ACK, the Master sends a byte address that is written into the address pointer of the IS24C52. After receiving another ACK from the Slave, the Master device transmits the data byte to be written into the address memory location. The IS24C52 acknowledges once more and the Master generates the Stop condition, at which time the device begins its internal programming cycle. While this internal cycle is in progress, the device will not respond to any request from the Master device.

Page Write

The IS24C52 is capable of 16-byte Page-Write operation. A Page-Write is initiated in the same manner as a Byte Write, but instead of terminating the internal Write cycle after the first data byte is transferred, the Master device can transmit up to 15 more bytes. After the receipt of each data byte, the IS24C52 responds immediately with an ACK on SDA line, and the four lower order data byte address bits are internally incremented by one, while the higher order bits of the data byte address remain constant. If a byte address is incremented from the last byte of a page, it returns to the first byte of that page. If the Master device should transmit more than 16 bytes prior to issuing the Stop condition, the address counter will "roll over," and the previously written data will be overwritten. Once all 16 bytes are received and the Stop condition has been sent by the Master, the internal programming cycle begins. At this point, all received data is written to the IS24C52 in a single Write cycle. All inputs are disabled until completion of the internal Write cycle.

Permanent Write Protection

The IS24C52 contains a permanent write protection feature that is initiated by means of a software command. After the command is transmitted, the protected area becomes irreversibly read-only despite power removal and re-application on the device. The address range of the 128 bytes of the array that is affected by this feature is 00h-7Fh. Once enabled, the permanent protection is independent of the status of the WP pin. (If WP is raised to High, the entire array is read-only. If WP is low, the region 00h-7Fh can still be read-only.)

The software command is initiated similarly to a normal byte write operation; however, the slave address begins with the bits 0110 (see Figure 5). The following three bits are A2 - A0. The last bit of the slave address (R/$\overline{W}$) is 0. If the IS24C52 responds with ACK, then the device has not yet had its write-protection permanently enabled. To complete the command, the Master must transmit a dummy address byte, dummy data byte, and a Stop signal (see Figure 11). The WP pin must be Low during this command. Before resuming any other command, the internal write cycle should be observed.

The status of the permanent write protection can be safely determined without any changes by transmitting the same Slave address as above, but with the last bit (R/$\overline{W}$) set to 1(see Figure 12). If the permanent write protection has been enabled, then the IS24C52 will not acknowledge any slave address starting with bits 0110 (see Figure 5).

Acknowledge (ACK) Polling

The disabling of the inputs can be used to take advantage of the typical Write cycle time. Once the Stop condition is issued to indicate the end of the host's Write operation, the IS24C52 initiates the internal Write cycle. ACK polling can be initiated immediately. This involves issuing the Start condition followed by the Slave address for a Write operation. If the IS24C52 is still busy with the Write operation, no ACK will be returned. If the IS24C52 has completed the Write operation, an ACK will be returned and the host can then proceed with the next Read or Write operation.

READ OPERATION

Read operations are initiated in the same manner as Write operations, except that the (R/$\overline{W}$) bit of the Slave address is set to "1". There are three Read operation options: current address read, random address read and sequential read.

Current Address Read

The IS24C52 contains an internal address counter which maintains the address of the last byte accessed, incremented by one. For example, if the previous operation is either a Read or Write operation addressed to the address location n, the internal address counter would increment to address location n+1. When the IS24C52 receives the Device Addressing Byte with a Read operation (R/$\overline{W}$ bit set to "1"), it will respond an ACK and transmit the 8-bit data byte stored at address location n+1. The Master should not acknowledge the transfer but should generate a Stop condition so the IS24C52 discontinues transmission. If 'n' is the last byte of the memory, then the data from location '0' will be transmitted. (Refer to Figure 8. Current Address Read Diagram.)

Random Address Read

Selective Read operations allow the Master device to select at random any memory location for a Read operation. The Master device first performs a 'dummy' Write operation by sending the Start condition, Slave address and word address of the location it wishes to read. After the IS24C52 acknowledges the word address, the Master device resends the Start condition and the Slave address, this time with the R/$\overline{W}$ bit set to one. The IS24C52 then responds with its ACK and sends the data requested. The Master device does not send an ACK but will generate a Stop condition. (Refer to Figure 9. Random Address Read Diagram.)

Sequential Read

Sequential Reads can be initiated as either a Current Address Read or Random Address Read. After the IS24C52 sends the initial byte sequence, the Master device responds with an ACK indicating it requires additional data from the IS24C52. The IS24C52 continues to output data for each ACK received. The Master device terminates the sequential Read operation by pulling SDA High (no ACK) indicating the last data byte to be read, followed by a Stop condition.

The data output is sequential, with the data from address n followed by the data from address n+1, ... etc. The address counter increments by one automatically, allowing the entire memory contents to be serially read during sequential Read operations. When the memory address boundary 255 is reached, the address counter "rolls over" to address 0, and the IS24C52 continues to output data for each ACK received. (Refer to Figure 10. Sequential Read Operation Starting with a Random Address Read Diagram.)

Figure 1. Typical System Bus Configuration

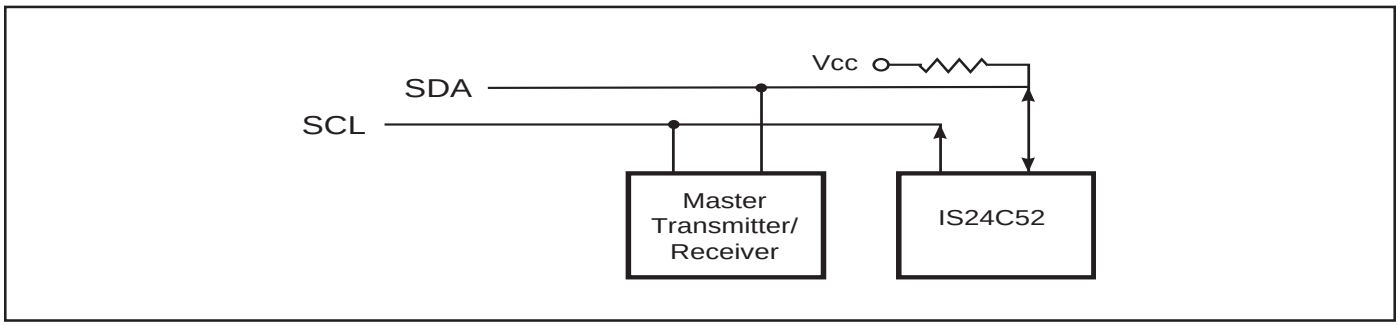


Figure 2. Output Acknowledge

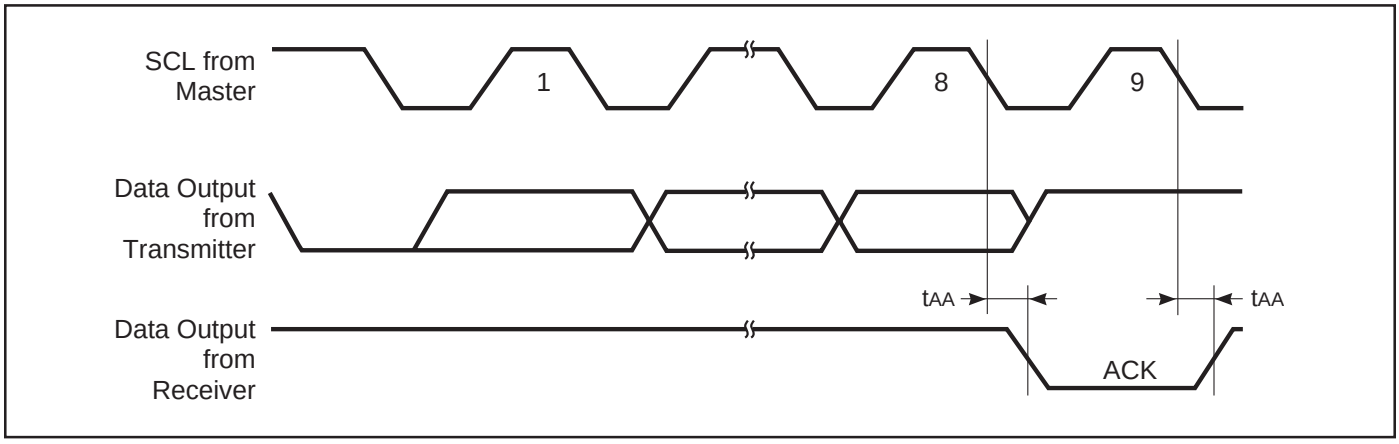


Figure 3. Start and Stop Conditions

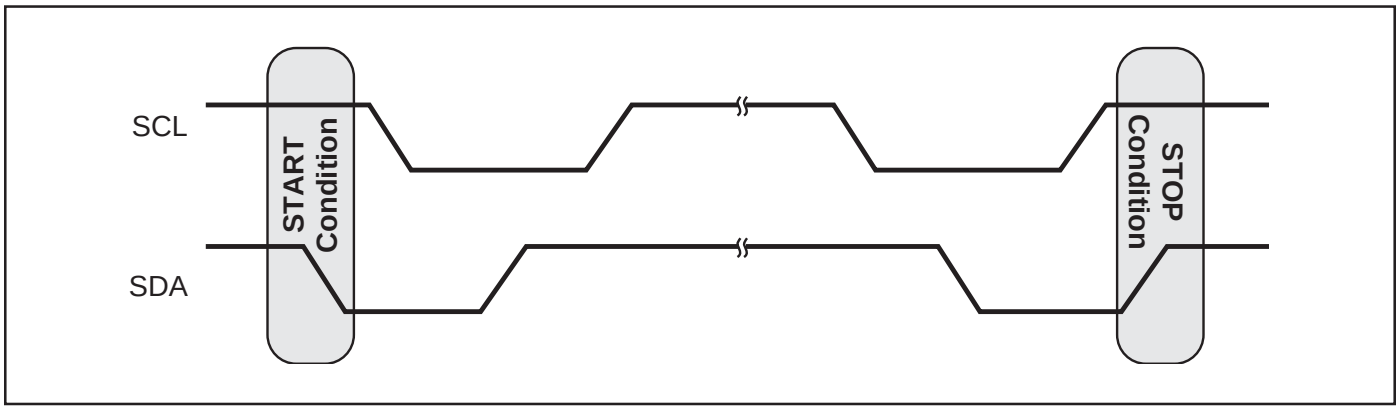


Figure 4. Data Validity Protocol

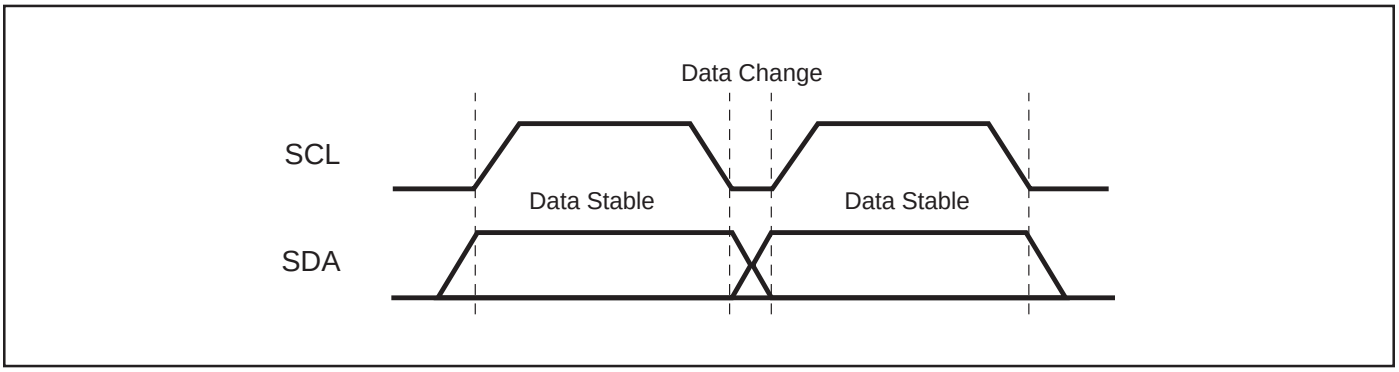


Figure 5. Slave Address

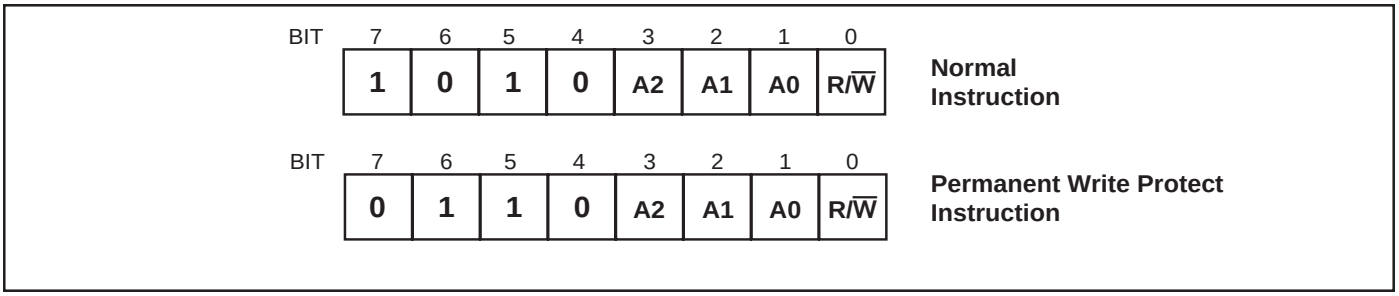


Figure 6. Byte Write

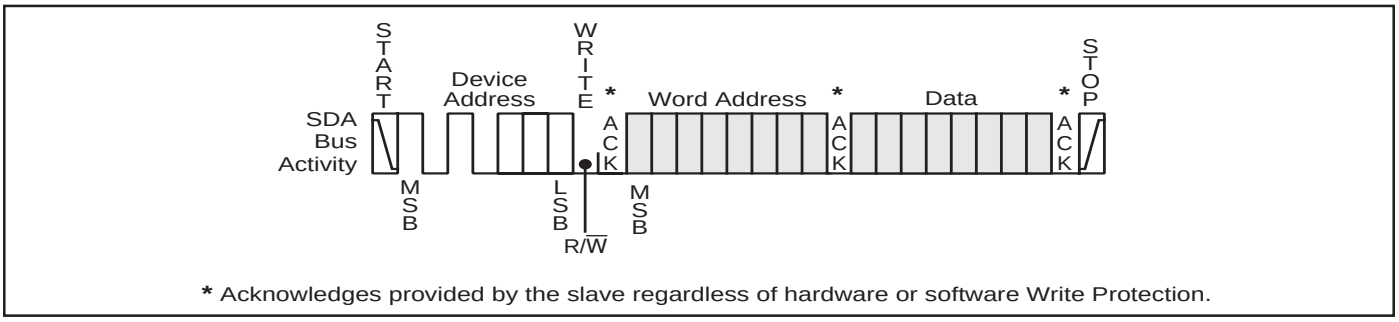


Figure 7. Page Write

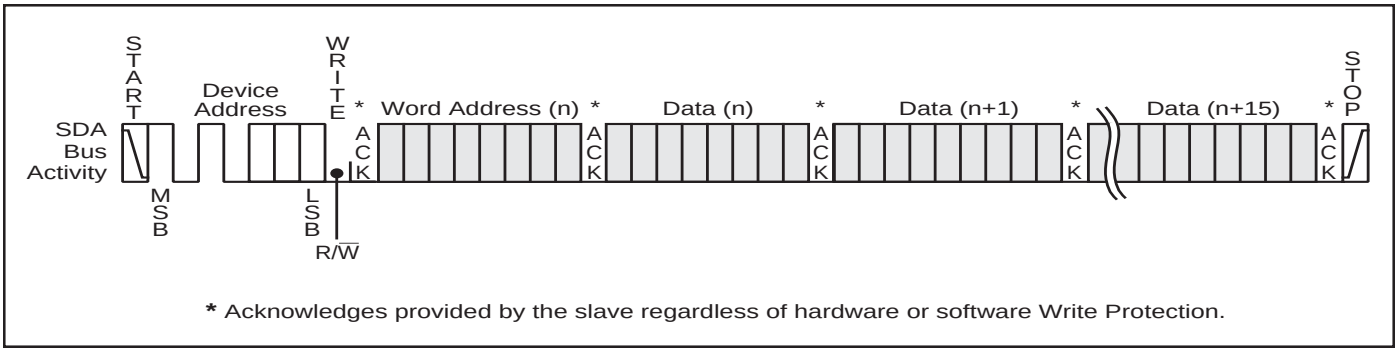


Figure 8. Current Address Read

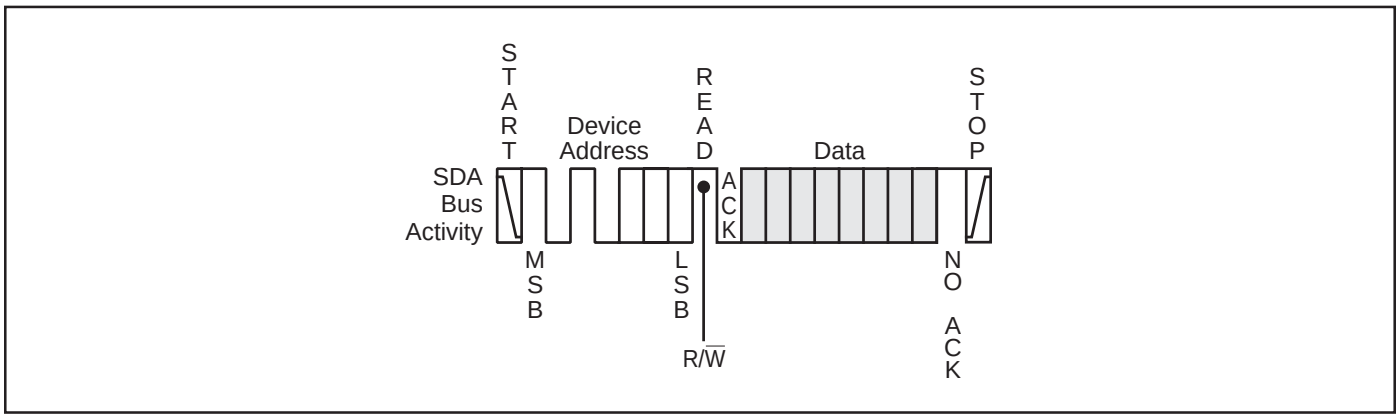


Figure 9. Random Address Read

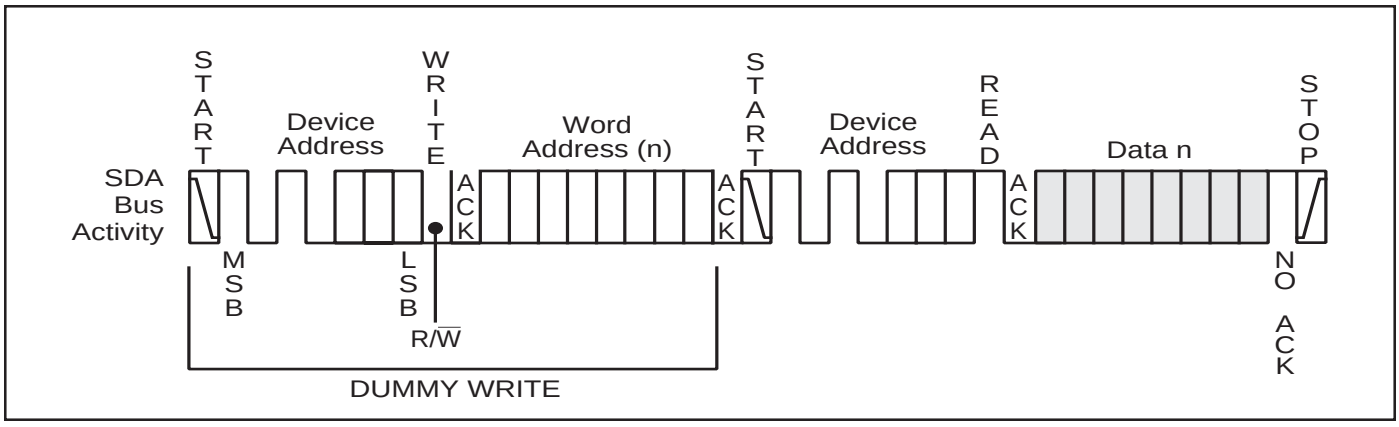


Figure 10. Sequential Read

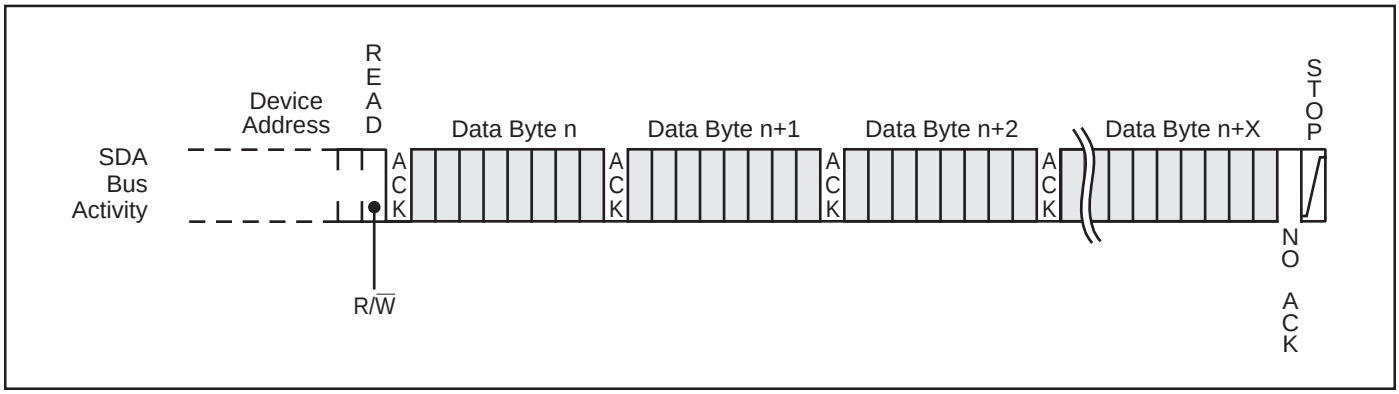
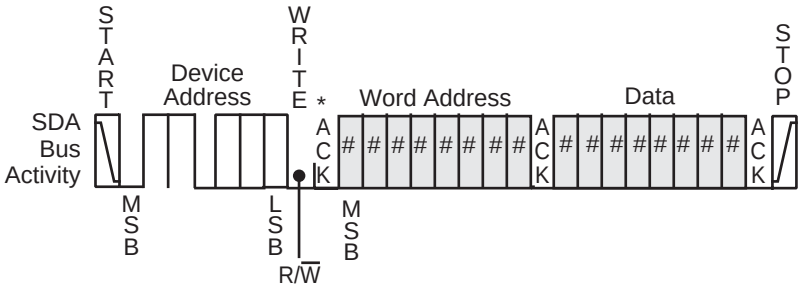


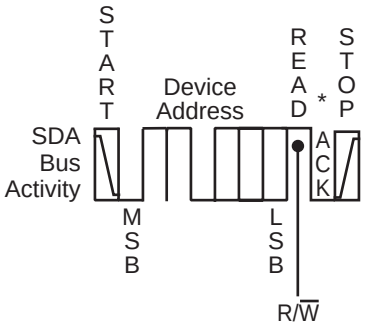
FIGURE 11. PERMANENT WRITE PROTECTION INITIATION



* The slave does not provide an acknowledgement if the permanent write protection is already enabled.

Don't care bits are required.

FIGURE 12. PERMANENT WRITE PROTECTION VERIFICATION



* The slave does not provide an acknowledgement if the permanent write protection is already enabled.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	0.5 to +6.25	V
V_P	Voltage on Any Pin	–0.5 to Vcc + 0.5	V
T_{BIAS}	Temperature Under Bias	–40 to +85	°C
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	Output Current	5	mA

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

(IS24C52-2)

Range	Ambient Temperature	Vcc
Commercial	0°C to +70°C	1.8V to 5.5V
Industrial	–40°C to +85°C	1.8V to 5.5V

OPERATING RANGE

(IS24C52-3)

Range	Ambient Temperature	Vcc
Commercial	0°C to +70°C	2.5V to 5.5V
Industrial	–40°C to +85°C	2.5V to 5.5V
Automotive	–40°C to +125°C	2.5V to 5.5V

Note: Automotive data is preliminary.

CAPACITANCE(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, Vcc = 5.0V.

DC ELECTRICAL CHARACTERISTICS

Commercial (T_A = 0°C to +70°C) Industrial (T_A = -40°C to +85°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$V_{OL}1$	Output Low Voltage	V_{CC} = 1.8V, I_{OL} = 0.15 mA	—	0.2	V
$V_{OL}2$	Output Low Voltage	V_{CC} = 2.5V, I_{OL} = 3 mA	—	0.4	V
V_{IH}	Input High Voltage		V_{CC} x 0.7	V_{CC} + 0.5	V
V_{IL}	Input Low Voltage		–1.0	V_{CC} x 0.3	V
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} max.	—	3	µA
I_{LO}	Output Leakage Current		—	3	µA

Notes: V_{IL} min and V_{IH} max are reference only and are not tested.

POWER SUPPLY CHARACTERISTICS

Commercial (T_A = 0°C to +70°C) Industrial (T_A = -40°C to +85°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$I_{CC}1$	Vcc Operating Current	Read at 400 KHz (Vcc = 5V)	—	2.0	mA
$I_{CC}2$	Vcc Operating Current	Write at 400 KHz (Vcc = 5V)	—	3.0	mA
$I_{SB}1$	Standby Current	Vcc = 1.8V	—	1	µA
$I_{SB}2$	Standby Current	Vcc = 2.5V	—	2	µA
$I_{SB}3$	Standby Current	Vcc = 5.0 V	—	6	µA

AC ELECTRICAL CHARACTERISTICS

Commercial (T_A = 0°C to +70°C) Industrial (T_A = -40°C to +85°C)

		1.8V-5.5V		2.5V-5.5V		4.5V-5.5V		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
f_{SCL}	SCL Clock Frequency	0	100	0	400	0	1000	KHz
T	Noise Suppression Time(1)	—	100	—	50	—	50	ns
t_{Low}	Clock Low Period	4.7	—	1.2	—	0.6	—	µs
t_{High}	Clock High Period	4	—	0.6	—	0.4	—	µs
t_{BUF}	Bus Free Time Before New Transmission(1)	4.7	—	1.2	—	0.5	—	µs
$t_{SU:STA}$	Start Condition Setup Time	4	—	0.6	—	0.25	—	µs
$t_{SU:STO}$	Stop Condition Setup Time	4	—	0.6	—	0.25	—	µs
$t_{HD:STA}$	Start Condition Hold Time	4	—	0.6	—	0.25	—	µs
$t_{HD:STO}$	Stop Condition Hold Time	4	—	0.6	—	0.25	—	µs
$t_{SU:DAT}$	Data In Setup Time	100	—	100	—	100	—	ns
$t_{HD:DAT}$	Data In Hold Time	0	—	0	—	0	—	ns
$t_{SU:WP}$	WP pin Setup Time	4	—	0.6	—	0.6	—	µs
$t_{HD:WP}$	WP pin Hold Time	4.7	—	1.2	—	1.2	—	µs
t_{DH}	Data Out Hold Time (SCL Low to SDA Data Out Change)	100	—	50	—	50	—	ns
t_{AA}	Clock to Output (SCL Low to SDA Data Out Valid)	100	3500	50	900	50	400	ns
t_R	SCL and SDA Rise Time(1)	—	1000	—	300	—	300	ns
t_F	SCL and SDA Fall Time(1)	—	300	—	300	—	100	ns
t_{WR}	Write Cycle Time	—	10	—	10	—	5	ms

FIGURE 13. AC WAVEFORMS

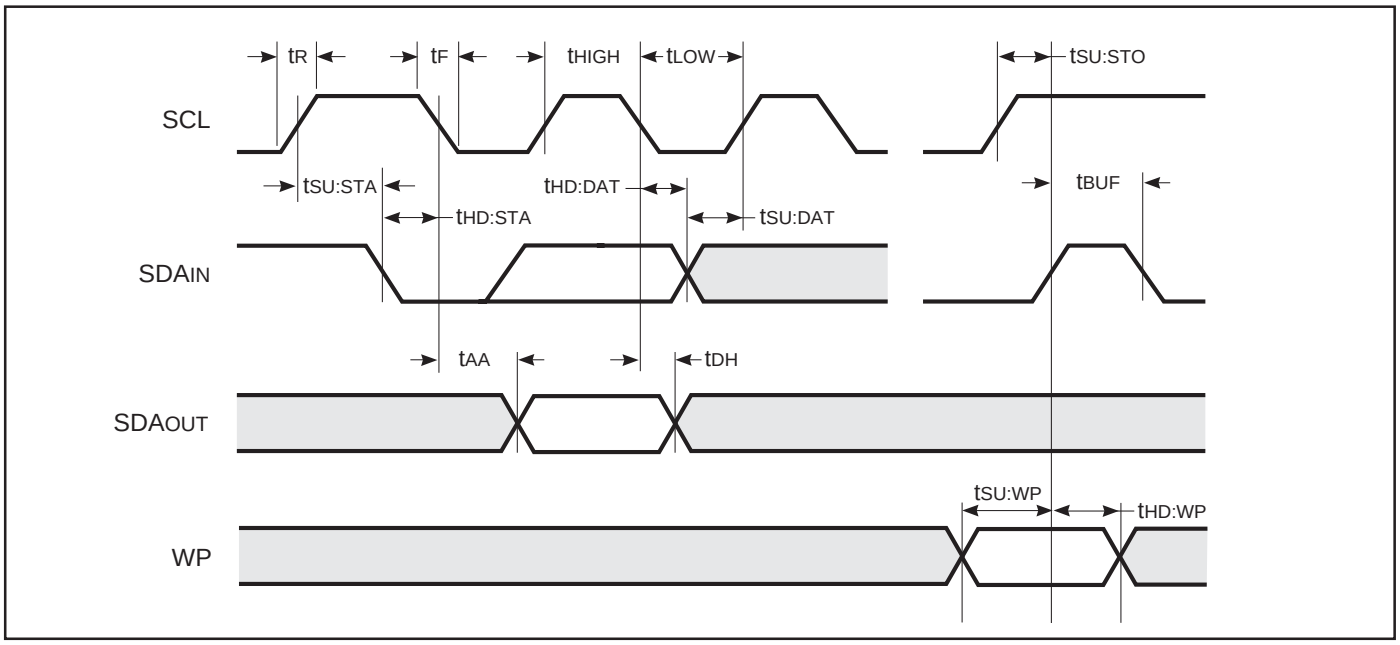
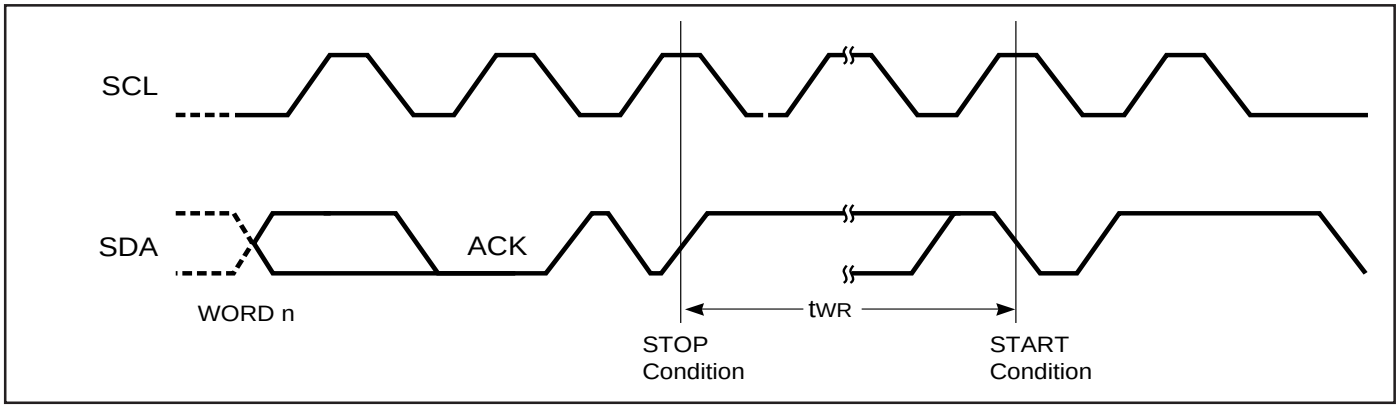


FIGURE 14. WRITE CYCLE TIMING



ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Frequency	Voltage Range	Part Number	Package
100 KHz	1.8V to 5.5V	IS24C52-2G IS24C52-2S IS24C52-2Z	Small Outline (JEDEC STD) (8-pin) MSOP TSSOP
400 KHz	2.5V to 5.5V	IS24C52-3G IS24C52-3S IS24C52-3Z	Small Outline (JEDEC STD) (8-pin) MSOP TSSOP

Industrial Range: –40°C to +85°C

Frequency	Voltage Range	Part Number	Package
100 KHz	1.8V to 5.5V	IS24C52-2GI IS24C52-2SI IS24C52-2ZI	Small Outline (JEDEC STD) (8-pin) MSOP TSSOP
400 KHz	2.5V to 5.5V	IS24C52-3GI IS24C52-3SI IS24C52-3ZI	Small Outline (JEDEC STD) (8-pin) MSOP TSSOP

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