128K x 8 HIGH-SPEED CMOS STATIC RAM

PRELIMINARY INFORMATION
APRIL 2003

FEATURES

- High-speed access time: 20ns
- High-performance, low-power CMOS process
- Multiple center power and ground pins for greater noise immunity
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- $\overline{CE}$ power-down
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
- Single 2.5V-3.6V V_{DD} power supply
- Packages available:
  - 32-pin TSOP (Type II)
  - 32-pin sTSOP (Type I)
  - 36-Ball miniBGA (6mm x 8mm)
  - 44-pin TSOP (Type II)

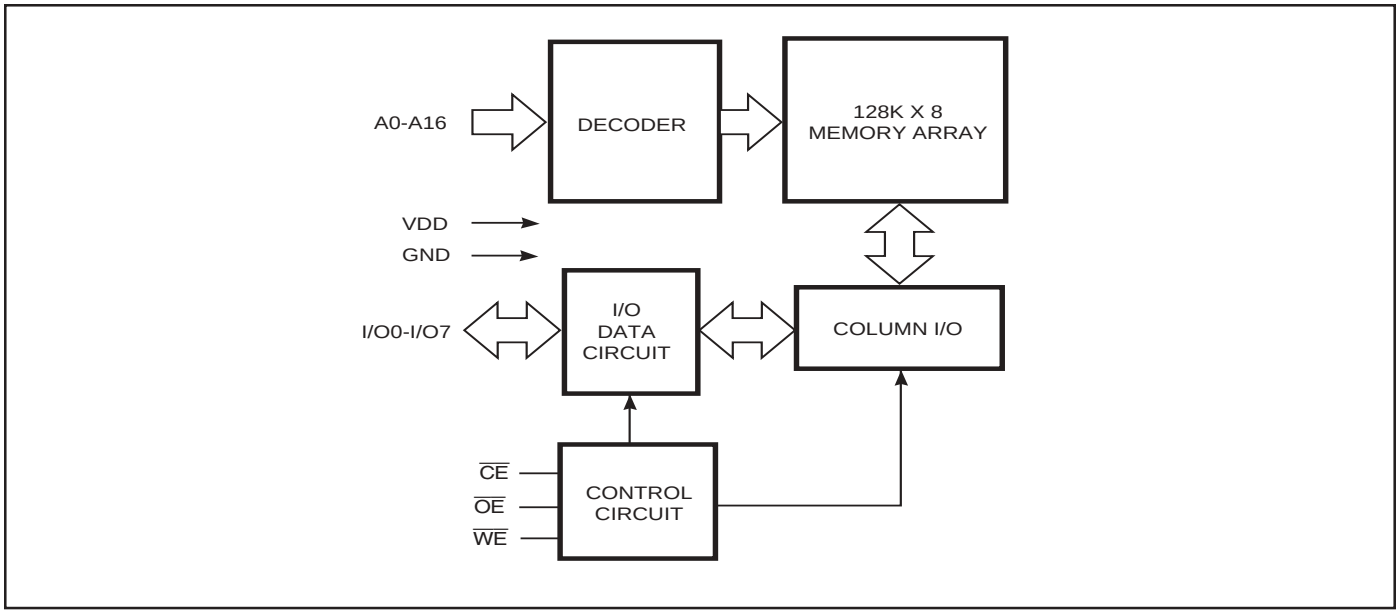
DESCRIPTION

The *ISSI* IS63WV1024LL is a very high-speed, low power, 131,072-word by 8-bit CMOS static RAM. The IS63WV1024LL is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

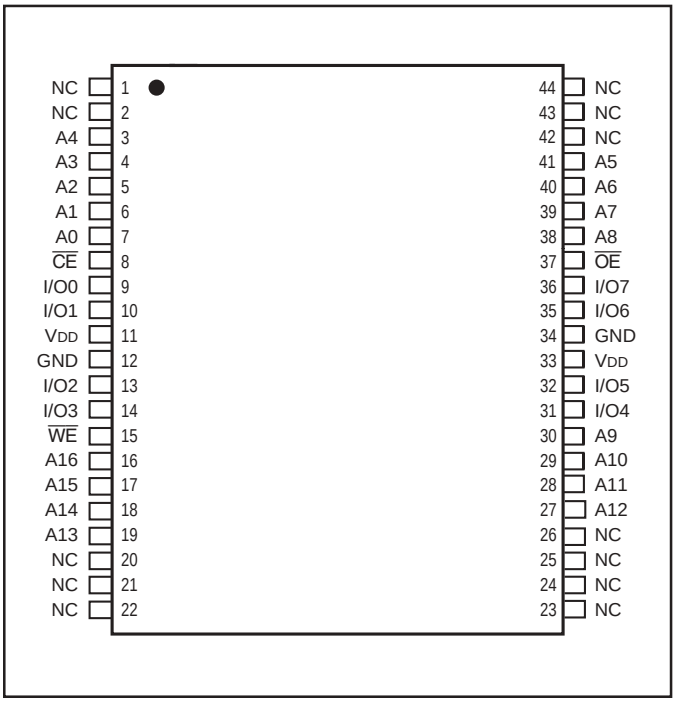
When $\overline{CE}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down to 250 µW (typical) with CMOS input levels.

The IS63WV1024LL operates from a single V_{DD} power supply. The IS63WV1024LL is available in 32-pin TSOP (Type II), 32-pin sTSOP (Type I), 36-Ball miniBGA (6mm x 8mm), and 44-pin TSOP (Type II) packages.

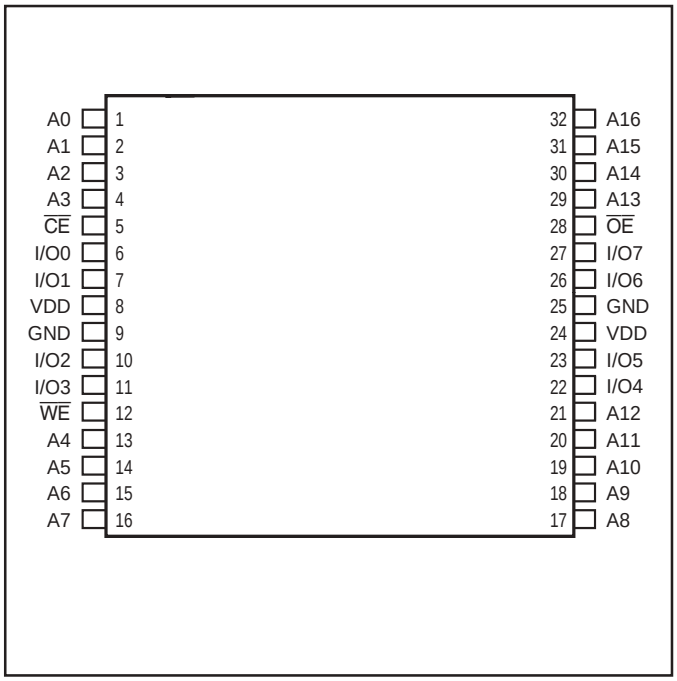
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION
44-Pin TSOP (Type II) (T2)



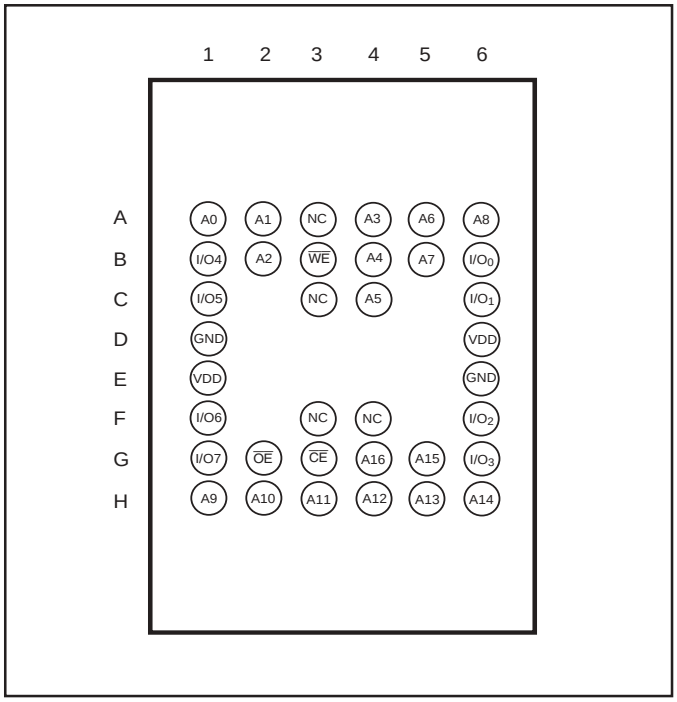
PIN CONFIGURATION
32-Pin TSOP (Type II) (T)
32-Pin sTSOP (Type I) (H)



PIN DESCRIPTIONS

A0-A16	Address Inputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Bidirectional Ports
V_{DD}	Power
GND	Ground

PIN CONFIGURATION
36-mini BGA (B) (6 mm x 8 mm)



TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O Operation	V_{DD} Current
Not Selected (Power-down)	X	H	X	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	High-Z	I_{CC1}, I_{CC2}
Read	H	L	L	D_{OUT}	I_{CC1}, I_{CC2}
Write	L	L	X	D_{IN}	I_{CC1}, I_{CC2}

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to V_{DD}+0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.5	W
V_{DD}	V_{DD} Related to GND	-0.2 to +3.9	V

Note:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE (V_{DD})

Range	Ambient Temperature	IS63WV1024LL
Commercial	0°C to +70°C	2.5V-3.6V
Industrial	–40°C to +85°C	2.5V-3.6V

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –1.0 mA	2.2	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 1.0 mA	—	0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage[1]		–0.3	0.6	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}	–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled	–1	1	µA

Notes:
1. V_{IL} (min.) = –2.0V for pulse width less than 10 ns.

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

				-20 ns		
Symbol	Parameter	Test Conditions	Options	Min.	Max.	Unit
I_{CC}	V_{DD} Dynamic Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX}	COM.	—	25	mA
			IND.	—	30	
			typ.[2]	—	15	
I_{CC1}	Operating Supply Current	V_{DD} = Max., Iout = 0mA, f = 0	COM.	—	5	mA
			IND.	—	5	
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{DD} = Max., V_{IN} = V_{IH} or V_{IL}, $\overline{CE}$ ≥ V_{IH}, f = 0	COM.	—	2	mA
			IND.	—	3	
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max., $\overline{CE}$ ≥ V_{DD} – 0.2V, V_{IN} ≥ V_{DD} – 0.2V, or V_{IN} ≤ 0.2V, f = 0	COM.	—	20	uA
			IND.	—	20	
			typ.[2]	—	4	

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at V_{DD}=2.5V, T_A=25°C. Not 100% tested.

CAPACITANCE[1]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	8	pF

Note:
1. Tested initially and after any design or process changes that may affect these parameters.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0.4V to V_{DD}-0.3V
Input Rise and Fall Times	1.5ns
Input and Output Timing and Reference Level (V_{Ref})	1.25V
Output Load	See Figures 1a and 1b

AC TEST LOADS

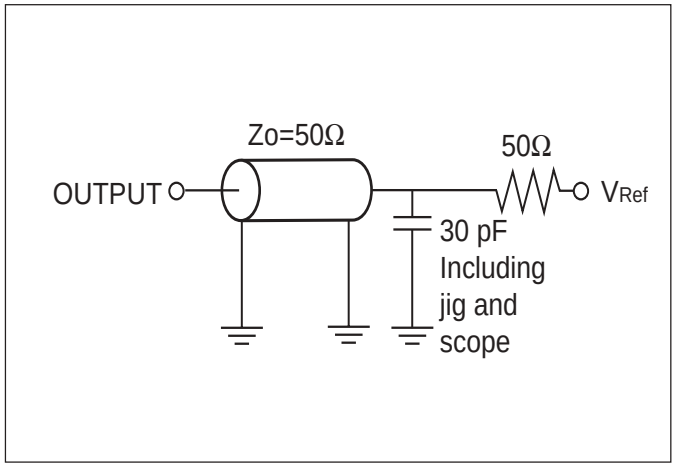


Figure 1a.

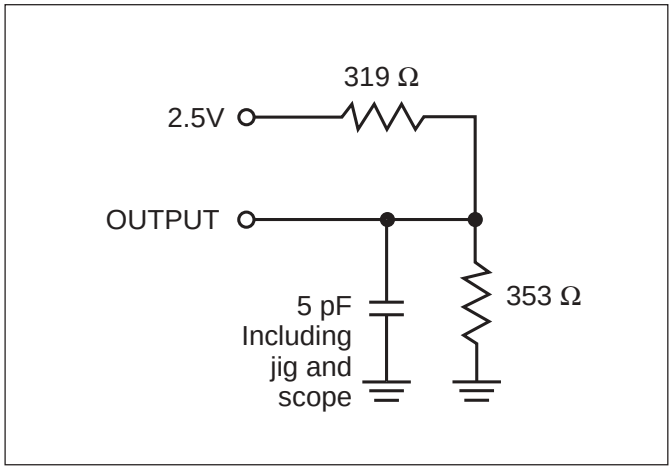


Figure 1b.

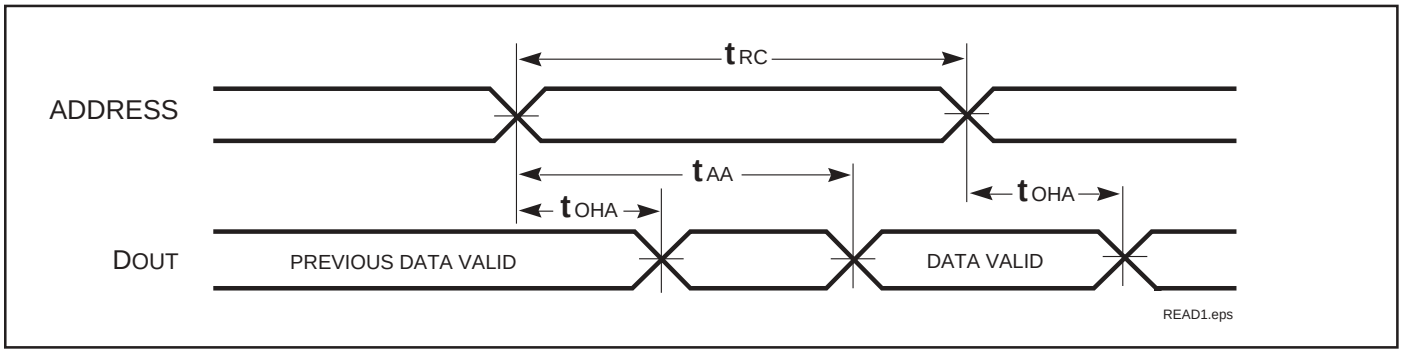
READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	-20 ns Min.	-20 ns Max.	Unit
t_{RC}	Read Cycle Time	20	—	ns
t_{AA}	Address Access Time	—	20	ns
t_{OHA}	Output Hold Time	3	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	20	ns
t_{DOE}	$\overline{OE}$ Access Time	—	8	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	0	8	ns
t_{LZCE}[2]	$\overline{CE}$ to Low-Z Output	3	—	ns
t_{HZCE}[2]	$\overline{CE}$ to High-Z Output	0	8	ns
t_{PU}	$\overline{CE}$ to Power Up Time	0	—	ns
t_{PD}	$\overline{CE}$ to Power Down Time	—	20	ns

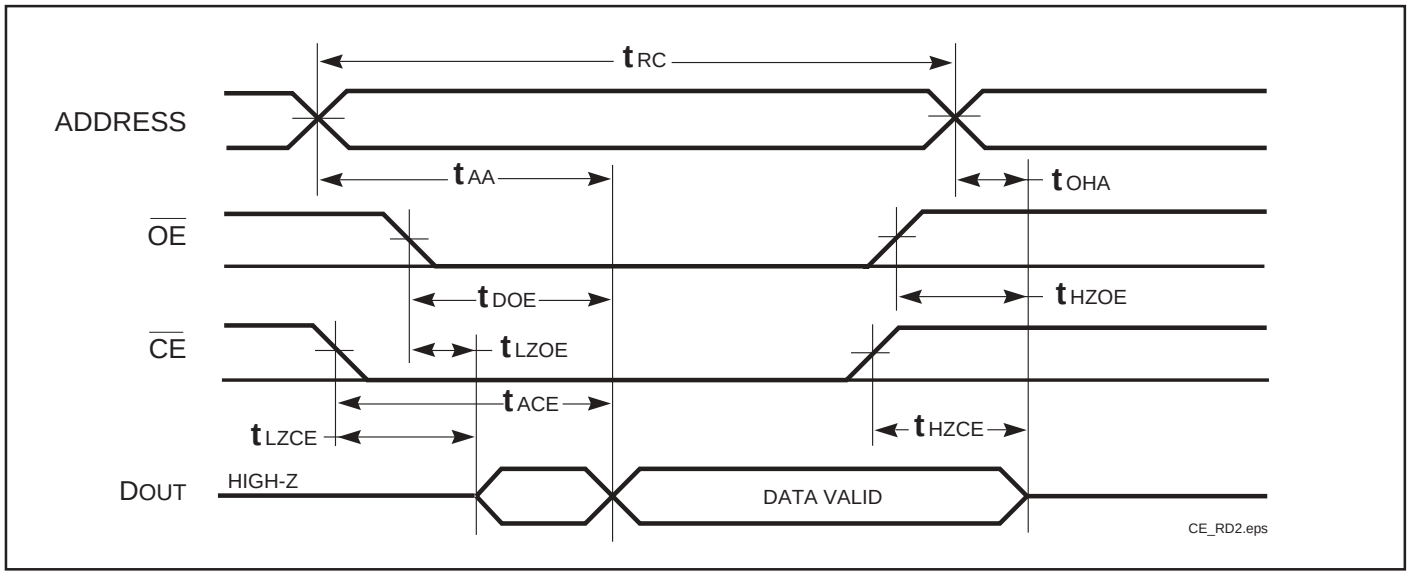
Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.25V, input pulse levels of 0.4V to V_{DD}-0.3V and output loading specified in Figure 1.
2. Tested with the loading specified in Figure 1. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

AC WAVEFORMS

READ CYCLE NO. 1[1,2]



READ CYCLE NO. 2[1,3]



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.

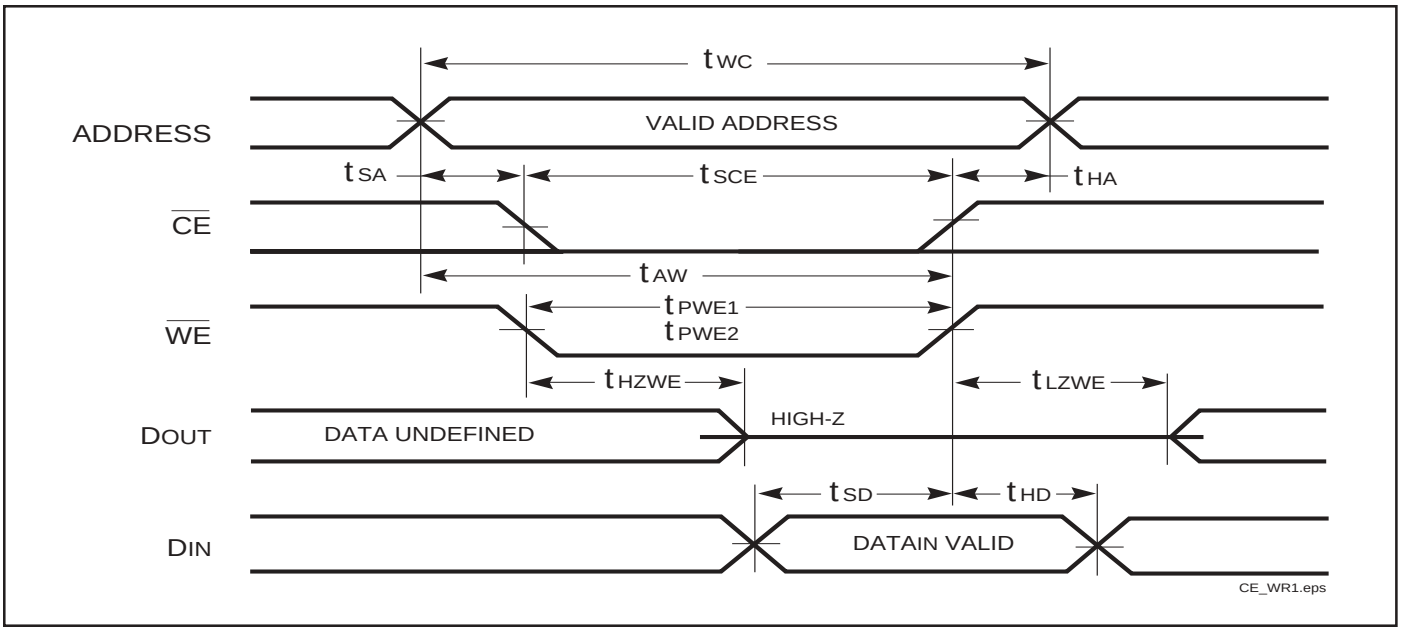
WRITE CYCLE SWITCHING CHARACTERISTICS[1,3] (Over Operating Range)

Symbol	Parameter	-20 ns Min.	Max.	Unit
t_{WC}	Write Cycle Time	20	—	ns
t_{SCE}	$\overline{CE}$ to Write End	12	—	ns
t_{AW}	Address Setup Time to Write End	12	—	ns
t_{HA}	Address Hold from Write End	0	—	ns
t_{SA}	Address Setup Time	0	—	ns
t_{PWE_1}[1]	$\overline{WE}$ Pulse Width ($\overline{OE}$ High)	12	—	ns
t_{PWE_2}[2]	$\overline{WE}$ Pulse Width ($\overline{OE}$ Low)	17	—	ns
t_{SD}	Data Setup to Write End	9	—	ns
t_{HD}	Data Hold from Write End	0	—	ns
t_{HZWE}[2]	$\overline{WE}$ LOW to High-Z Output	—	9	ns
t_{LZWE}[2]	$\overline{WE}$ HIGH to Low-Z Output	3	—	ns

Notes:
1. Test conditions assume signal transition times of 3ns or less, timing reference levels of 1.25V, input pulse levels of 0.4V to V_{DD}-0.3V and output loading specified in Figure 1a.
2. Tested with the loading specified in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.

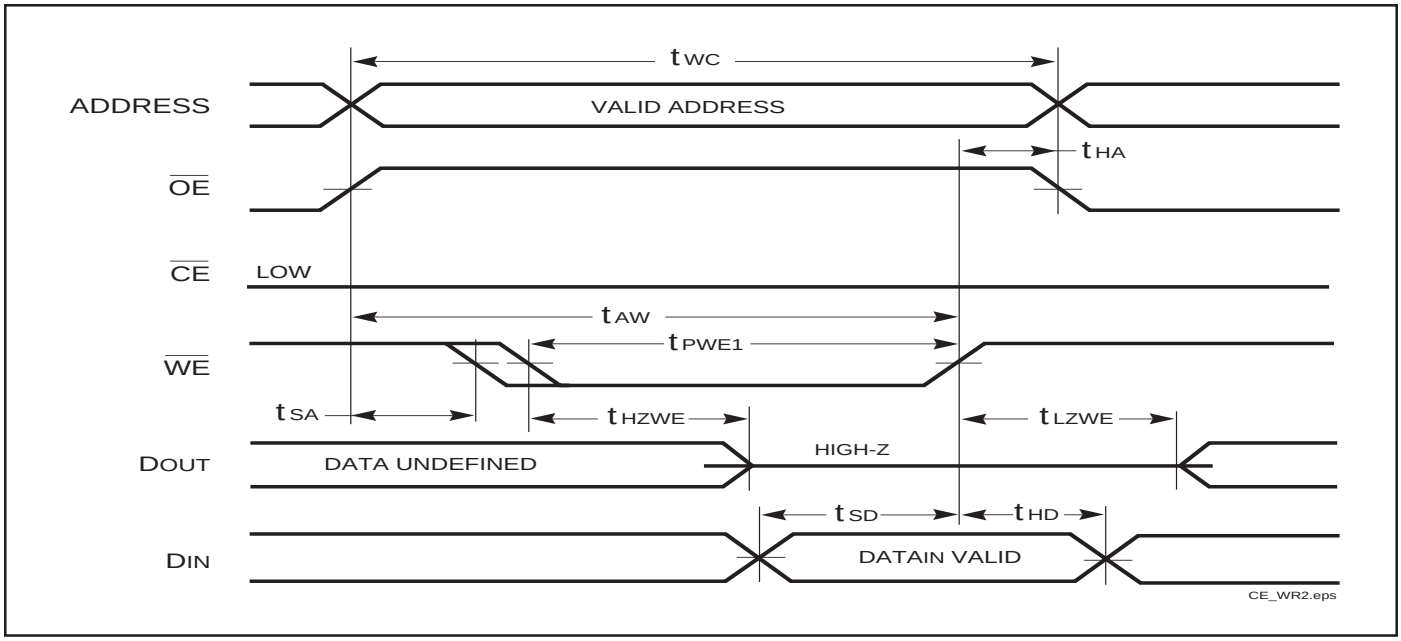
AC WAVEFORMS

WRITE CYCLE NO. 1[1,2] ($\overline{CE}$ Controlled, $\overline{OE}$ = HIGH or LOW)

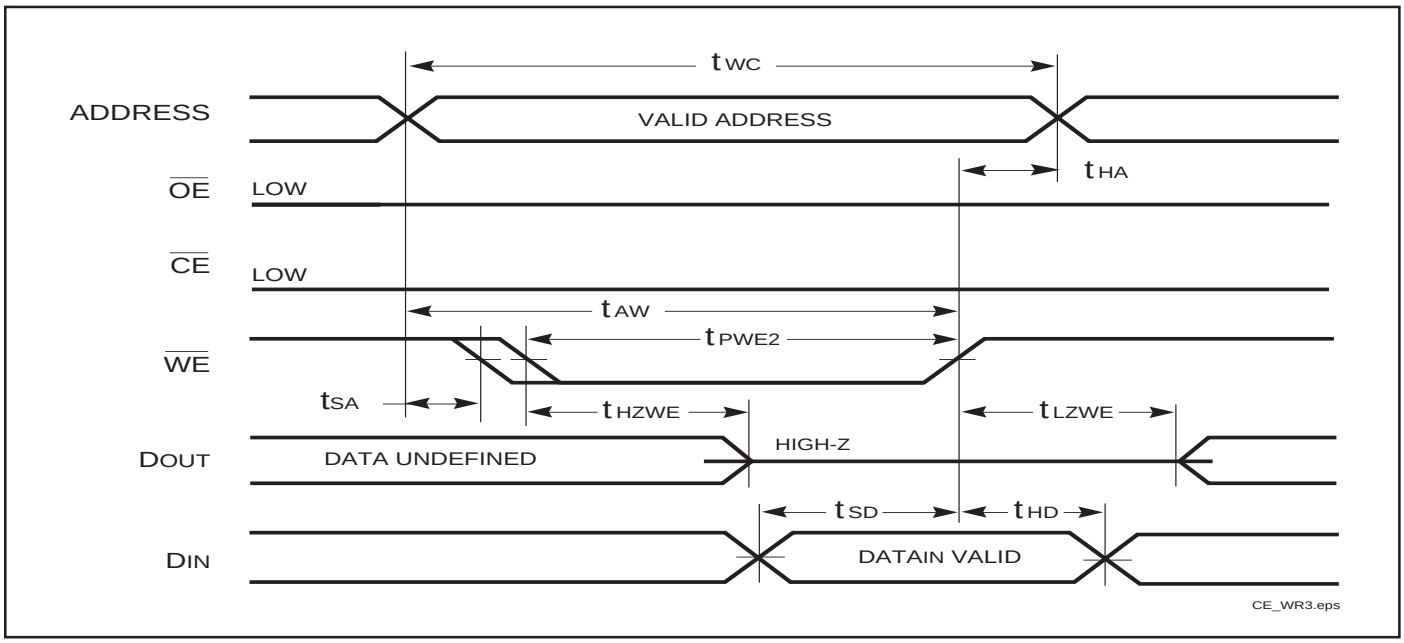


AC WAVEFORMS

WRITE CYCLE NO. 2[1] ($\overline{WE}$ Controlled, $\overline{OE}$ = HIGH during Write Cycle)



WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled: $\overline{OE}$ is LOW During Write Cycle)



Notes:

1. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE}$ > V_{IH}.

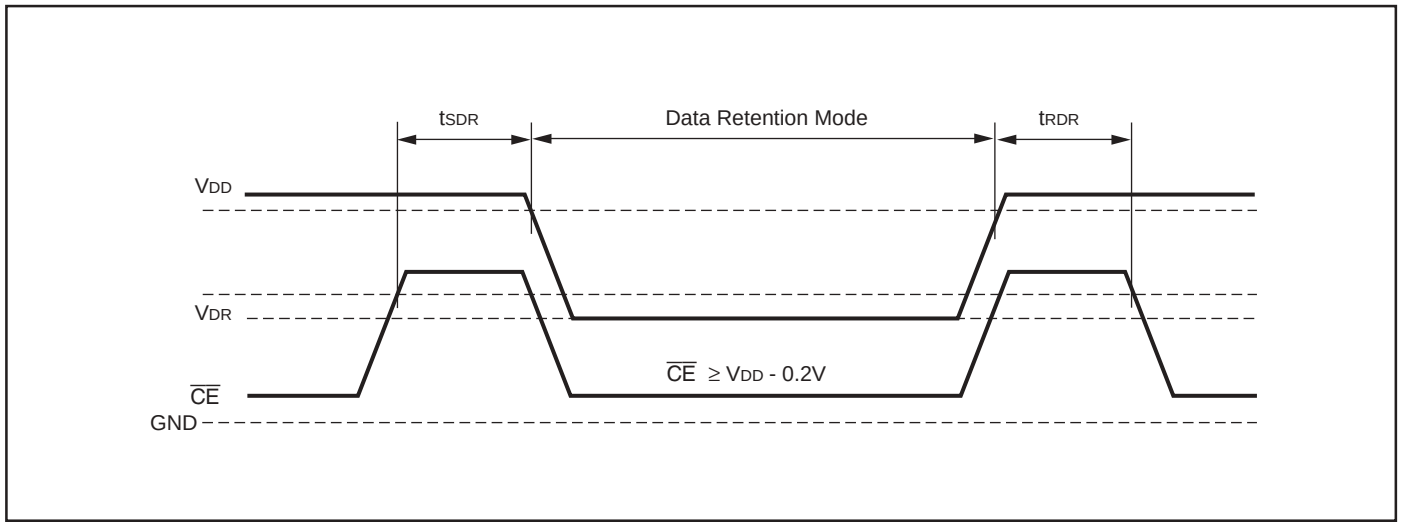
DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition	Operations	Min.	Typ.(1)	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		1.2	—	3.6	V
I_{DR}	Data Retention Current	V_{DD} = 1.2V, $\overline{CE} \geq V_{DD} - 0.2V$	COM.	—	4	20	µA
			IND.	—	4	20	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	—	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		t_{RC}	—	—	ns

Note:

1. Typical values are measured at V_{DD} = 2.5V, T_A = 25°C. Not 100% tested.

DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)



ORDERING INFORMATION

Commercial Range: 0°C to +70°C

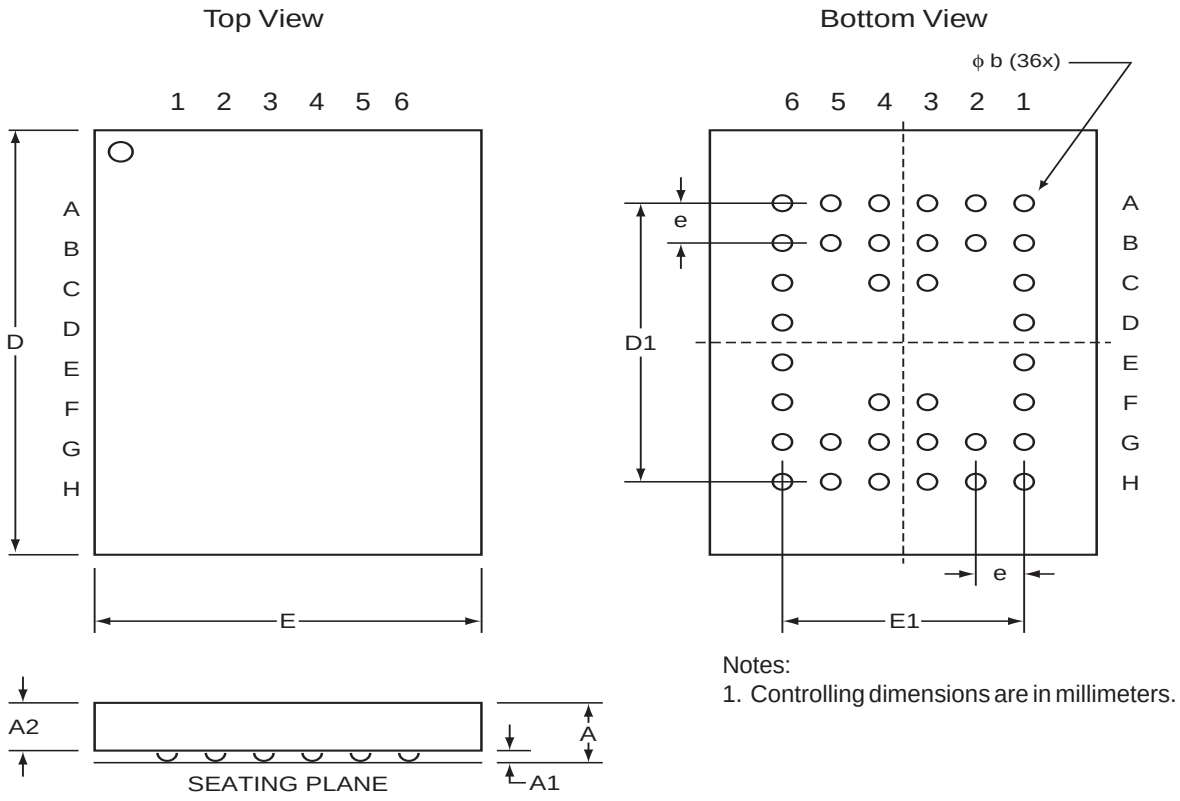
Speed (ns)	Order Part No.	Package
20	IS63WV1024LL-20T	32-pin TSOP (Type II)
	IS63WV1024LL-20H	sTSOP (Type I) (8mm x13.4mm)
	IS63WV1024LL-20T2	44-pin TSOP (Type II)
	IS63WV1024LL-20B	mBGA(6mmx8mm)

Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
20	IS63WV1024LL-20TI	32-pin TSOP (Type II)
	IS63WV1024LL-20HI	sTSOP (Type I) (8mm x13.4mm)
	IS63WV1024LL-20T2I	44-pin TSOP (Type II)
	IS63WV1024LL-20BI	mBGA(6mmx8mm)

PACKAGING INFORMATION

Mini Ball Grid Array
Package Code: B (36-pin)



Notes:
1. Controlling dimensions are in millimeters.

mBGA - 6mm x 8mm

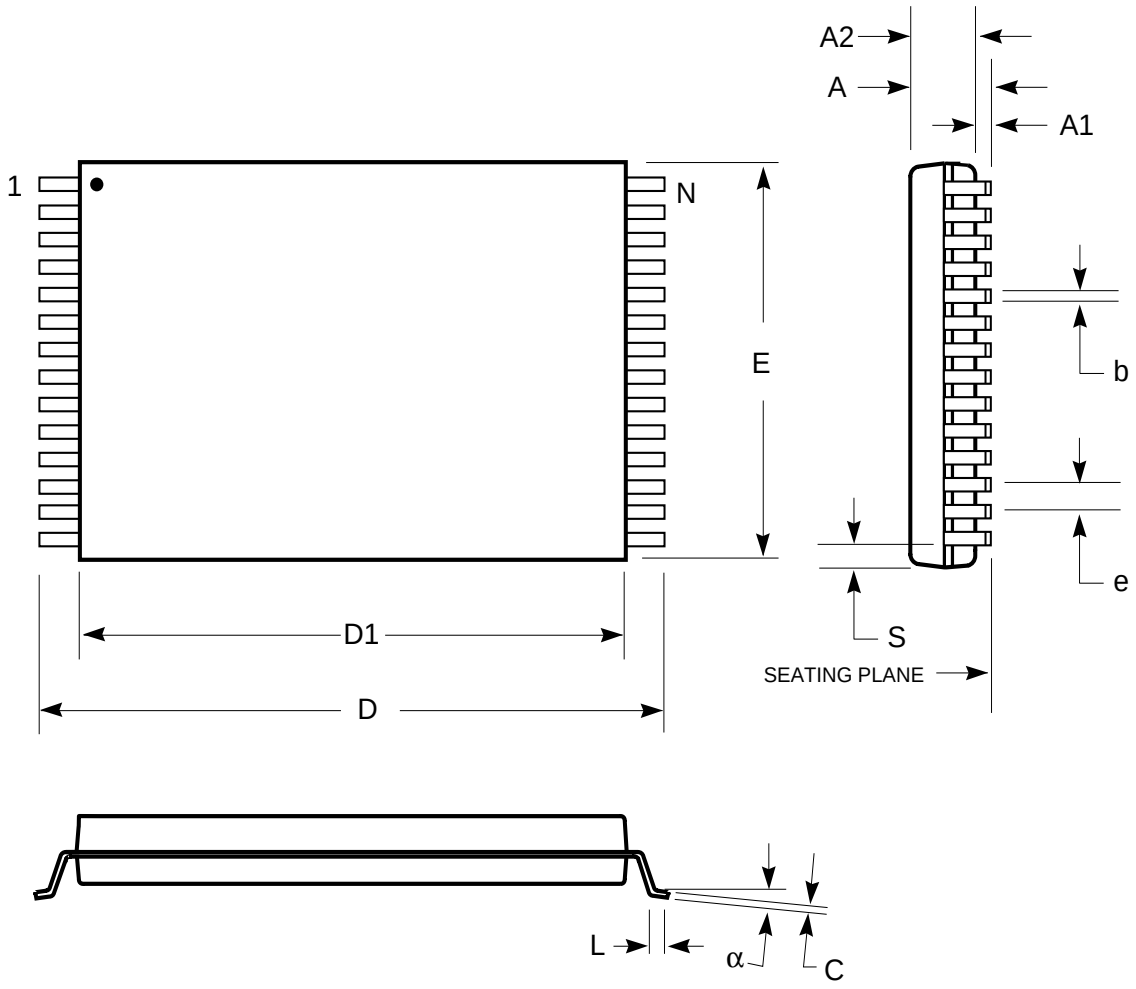
	MILLIMETERS			INCHES		
Sym.	Min.	Typ.	Max.	Min.	Typ.	Max.
N0. Leads		36			36	
A	—	—	1.20	—	—	0.047
A1	0.24	—	0.30	0.009	—	0.012
A2	0.60	—	—	0.024	—	—
D	7.90	8.00	8.10	0.311	0.315	0.319
D1		5.25BSC			0.207BSC	
E	5.90	6.00	6.10	0.232	0.236	0.240
E1		3.75BSC			0.148BSC	
e		0.75BSC			0.030BSC	
b	0.30	0.35	0.40	0.012	0.014	0.016

mBGA - 8mm x 10mm

	MILLIMETER			INCHES		
Sym.	Min.	Typ.	Max.	Min.	Typ.	Max.
N0. Leads		36			36	
A	—	—	1.20	—	—	0.047
A1	0.24	—	0.30	0.009	—	0.012
A2	0.60	—	—	0.024	—	—
D	9.90	10.00	10.10	0.390	0.394	0.398
D1		5.25BSC			.207BSC	
E	7.90	8.00	8.10	0.311	0.315	0.319
E1		3.75BSC			0.148BSC	
e		0.75BSC			0.030BSC	
b	0.30	0.35	0.40	0.012	0.014	0.016

PACKAGING INFORMATION

Plastic STSOP - 32 pins
Package Code: H (Type I)

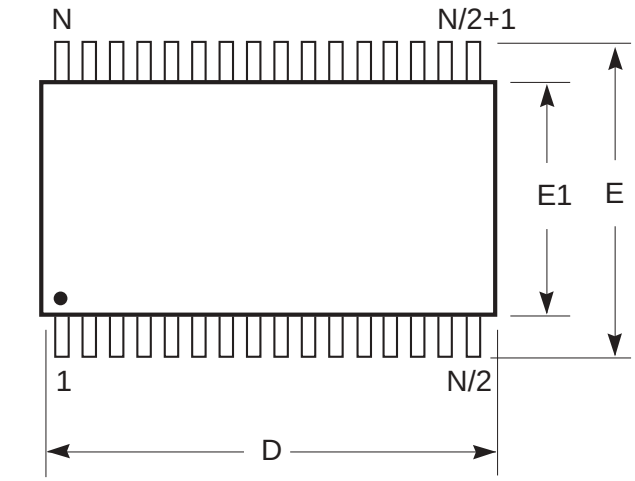


Plastic STSOP (H - Type I)				
	Millimeters		Inches	
Symbol	Min	Max	Min	Max
Ref. Std.				
N		32		
A	—	1.25	—	0.049
A1	0.05	—	0.002	—
A2	0.95	1.05	0.037	0.041
b	0.17	0.23	0.007	0.009
C	0.14	0.16	0.0055	0.0063
D	13.20	13.60	0.520	0.535
D1	11.70	11.90	0.461	0.469
E	7.90	8.10	0.311	0.319
e	0.50 BSC		0.020 BSC	
L	0.30	0.70	0.012	0.028
S	0.28 Typ.		0.011 Typ.	
α	0°	5°	0°	5°

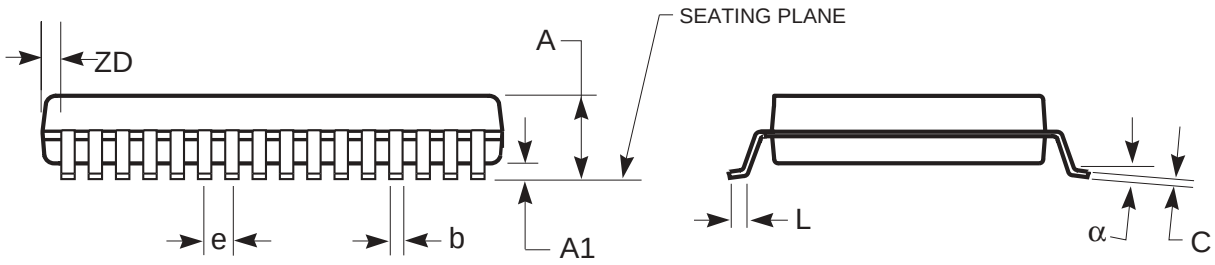
Notes:
1. Controlling dimension: millimeters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D1 and E do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

PACKAGING INFORMATION

Plastic TSOP
Package Code: T (Type II)



Notes:
1. Controlling dimension: millimieters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.



Plastic TSOP (T - Type II)												
	Millimeters		Inches		Millimeters		Inches		Millimeters		Inches	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Ref. Std.												
No. Leads (N)	32				44				50			
A	—	1.20	—	0.047	—	1.20	—	0.047	—	1.20	—	0.047
A1	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006
b	0.30	0.52	0.012	0.020	0.30	0.45	0.012	0.018	0.30	0.45	0.012	0.018
C	0.12	0.21	0.005	0.008	0.12	0.21	0.005	0.008	0.12	0.21	0.005	0.008
D	20.82	21.08	0.820	0.830	18.31	18.52	0.721	0.729	20.82	21.08	0.820	0.830
E1	10.03	10.29	0.391	0.400	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405
E	11.56	11.96	0.451	0.466	11.56	11.96	0.455	0.471	11.56	11.96	0.455	0.471
e	1.27 BSC		0.050 BSC		0.80 BSC		0.032 BSC		0.80 BSC		0.031 BSC	
L	0.40	0.60	0.016	0.024	0.41	0.60	0.016	0.024	0.40	0.60	0.016	0.024
ZD	0.95 REF.		0.037 REF.		0.81 REF.		0.032 REF.		0.88 REF.		0.035 REF	
α	0°	5°	0°	5°	0°	5°	0°	5°	0°	5°	0°	5°