IS71V16F32GST04
IS71V16F32GSB04

ISSI®

3.0 Volt-Only Flash & SRAM COMBO with Stacked Multi-Chip Package (MCP) — 32 Mbit Simultaneous Operation Flash Memory (x16) and 4 Mbit Static RAM (x16)

MAY 2003

MCP FEATURES

- Power supply voltage 2.7V to 3.3V
- High performance:
  Flash: 70ns maximum access time
  SRAM: 70ns maximum access time
- Packages: 59-ball BGA or 56-ball BGA
- Operating Temperature: -30C to +85C

FLASH FEATURES

- Power Dissipation:
  Read Current at 1 Mhz: 4 mA maximum
  Read Current at 5 Mhz:18 mA maximum
  Sleep Mode: 5 µA maximum
- User Configurable Banks
  - Bank A : 4 Mbit (8KB x 8 and 64KB x 7)
  - Bank B : 12 Mbit (64KB x 24)
  - Bank C : 12 Mbit (64KB x 24)
  - Bank D : 4 Mbit (64KB x 8)

  User chooses two virtual banks from a combination of four physical banks
- Simultaneous R/W Operations (dual virtual bank):
  Zero latency between read and write operations; Data can be programmed or erased in one bank while data is simultaneously being read from the other bank
- Low-Power Mode:
  A period of no activity causes flash to enter a low-power state
- Erase Suspend/Resume:
  Suspends of erase activity to allow a read in the same bank
- Sector Erase Architecture:
  8 sectors of 4K words each and 63 sectors of 32K words each in Word mode. Any combination of sectors, or the entire flash can be simultaneously erased
- Erase Algorithms:
  Automatically preprograms/erases the flash memory entirely, or by sector
- Program Algorithms:
  Automatically writes and verifies data at specified address
- Top or Bottom Boot
- Hidden ROM Region:
  256 byte with a Factory-serialized secure electronic serial number (ESN), which is accessible through a command sequence
- Data Polling and Toggle Bit:
  Allow for detection of program or erase cycle completion
- Ready-Busy output (RY/$\overline{BY}$)
  Detection of program or erase cycle completion
- Over 100,000 write/erase cycles
- Low supply voltage (Vccf ≤ 2.5V) inhibits writes
- $\overline{WP}$/ACC input pin:
  If V_{IL}, allows partial protection of boot sectors
  If V_{IH}, allows removal of boot sector protection
  If Vacc, program time is improved

SRAM FEATURES (4 Mb density)

- Power Dissipation:
  Operating: 40 mA maximum
  Standby: 10 µA maximum
- Chip Selects: $\overline{CE1}$s, CE2s
- Power down feature using $\overline{CE1}$s, or CE2s
- Data retention supply voltage: 1.5 to 3.3 volt
- Byte data control: $\overline{LB}$s (DQ0–DQ7), $\overline{UB}$s (DQ8–DQ15)

GENERAL DESCRIPTION

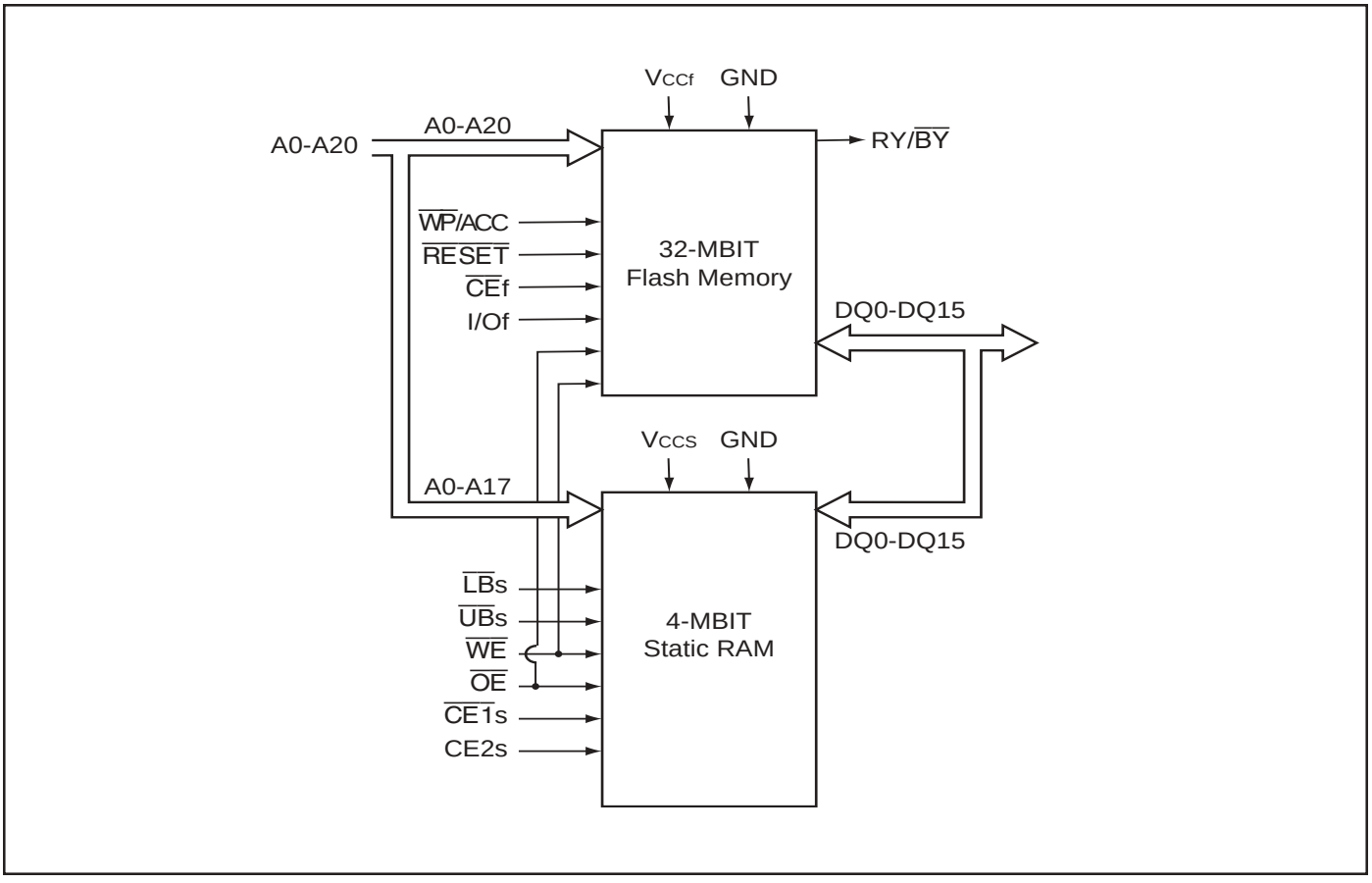
The flash and SRAM MCP is a 32 Mbit Flash/4 Mbit SRAM with shared data, address, and control pins. The 32 Mbit flash is composed of 2,097,152 words of 16 bits. The 4Mb SRAM has 262,144 words of 16 bits. Data lines DQ0-DQ15 handle the 16-bit word access for both the SRAM and Flash memories. Optionally, $\overline{UB}$s or $\overline{LB}$s control pins allow single byte accesses with the SRAM.

The package uses a 3.0V power supply for all operations. No other source is required for program and erase operations. The flash can be programmed in system using this 3.0V supply, or can be programmed in a standard EPROM programmer.

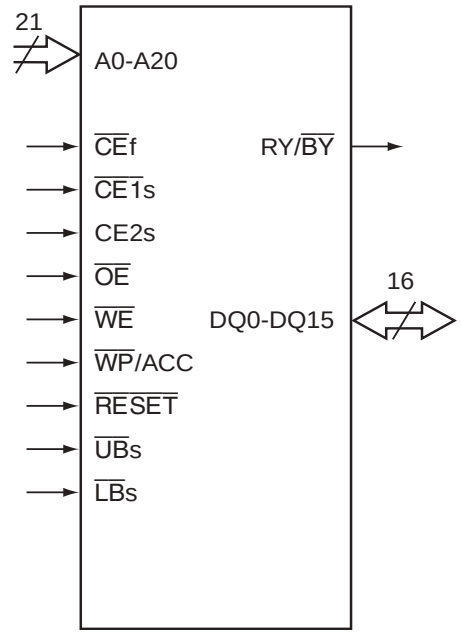
The 32 Mbit flash/4 Mbit SRAM is offered in 56-ball or 59-ball package. The flash is compatible with the JEDEC Flash command set standard. The flash access time is 70ns, and the SRAM access time is 70ns.

The Flash architecture is composed of two virtual banks which allows simultaneous operation on each. Optimized performance can be achieved by first initializing a program or erase function in one bank, then immediately starting a read from the other bank. Both operations would then be operating simultaneously, with zero latency.

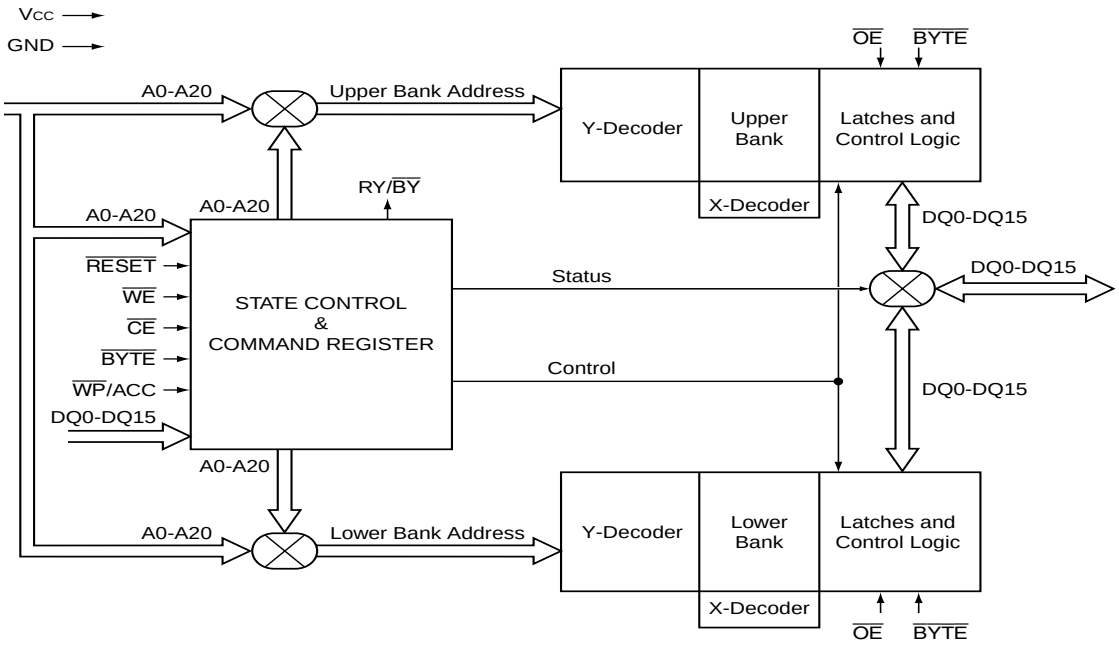
MCP BLOCK DIAGRAM



LOGIC SYMBOL

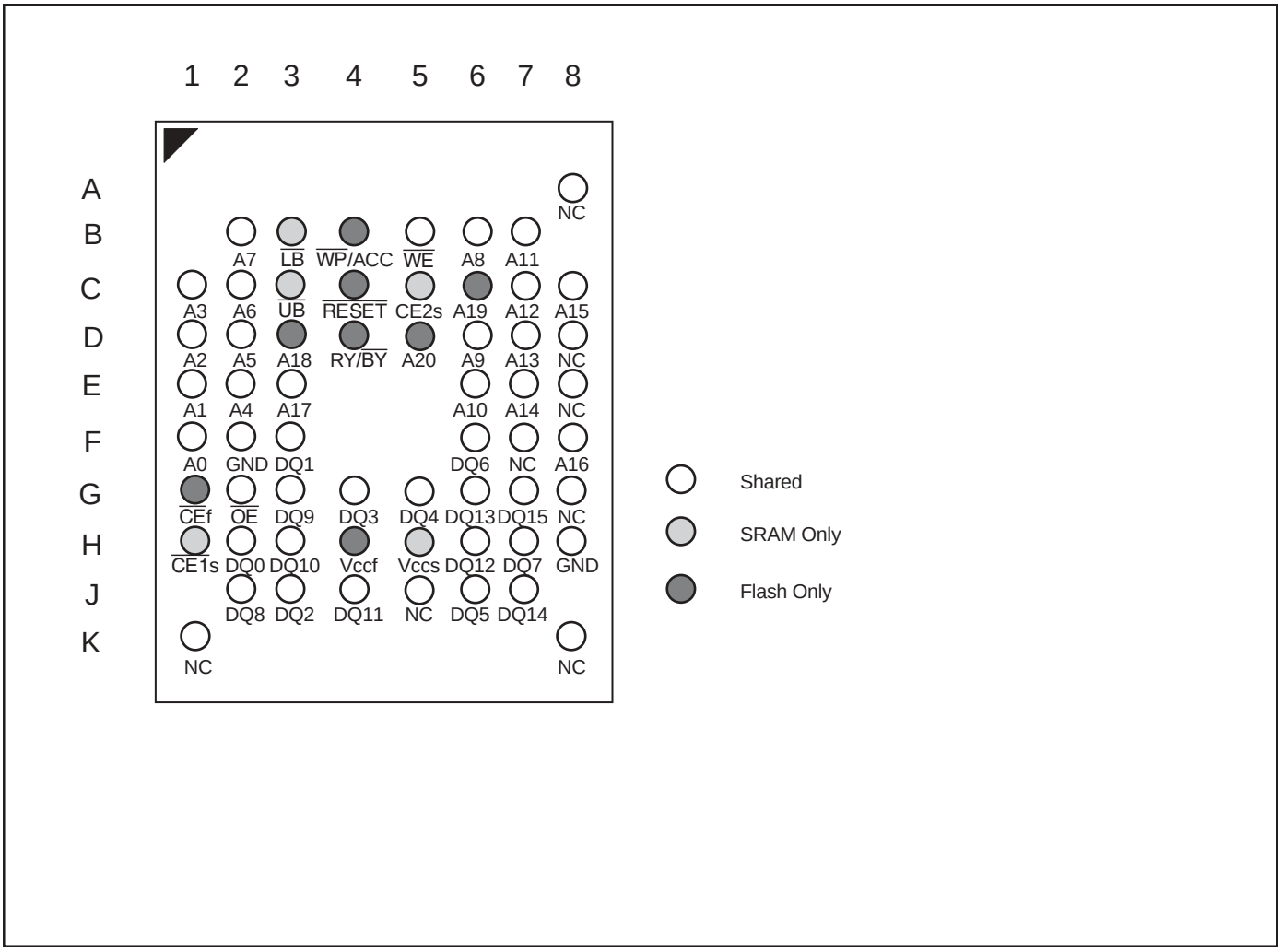


FLASH MEMORY BLOCK DIAGRAM



PIN CONFIGURATION (32 Mb Flash and 4 Mb SRAM)

PACKAGE CODE: B 59 BALL FBGA (Top View) (7.00 mm x 9.00 mm Body, 0.8 mm Ball Pitch)



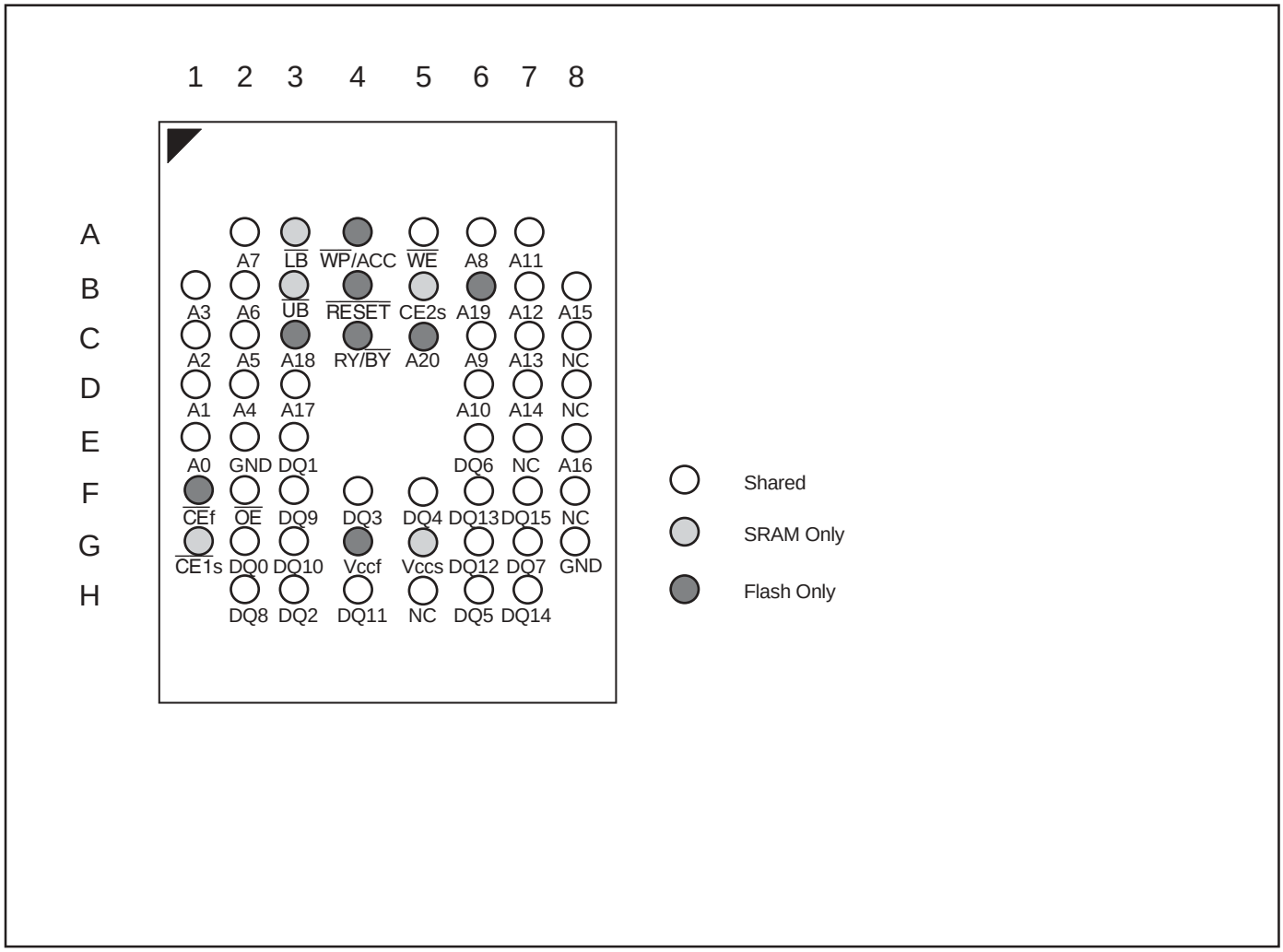
PIN DESCRIPTIONS

A17-A0	Address Inputs, Common
A20-A18	Address Inputs, Flash
DQ15-DQ0	Data Inputs/Outputs, Common
$\overline{RESET}$	Reset
$\overline{CE1}$s, CE2s	Chip Enable, SRAM
$\overline{CE}$f	Chip Enable, Flash
$\overline{OE}$	Output Enable, Common
$\overline{WE}$	Write Enable, Common

$\overline{LB}$s	Lower-byte Control, SRAM
$\overline{UB}$s	Upper-byte Control, SRAM
$\overline{WP}$/ACC	Write Protect/Acceleration Pin, Flash
RY/$\overline{BY}$	Ready/Busy Output (Flash) Open Drain Output
Vccf	Power, Flash
Vccs	Power, SRAM
GND	Ground, Common

PIN CONFIGURATION (32 Mb Flash and 4 Mb SRAM)

PACKAGE CODE: M 56 BALL FBGA (Top View) (7.00 mm x 9.00 mm Body, 0.8 mm Ball Pitch)



PIN DESCRIPTIONS

A17-A0	Address Inputs, Common
A20-A18	Address Inputs, Flash
DQ15-DQ0	Data Inputs/Outputs, Common
$\overline{RESET}$	Reset
$\overline{CE1}$s, CE2s	Chip Enable, SRAM
$\overline{CE}$f	Chip Enable, Flash
$\overline{OE}$	Output Enable, Common
$\overline{WE}$	Write Enable, Common

$\overline{LB}$s	Lower-byte Control, SRAM
$\overline{UB}$s	Upper-byte Control, SRAM
$\overline{WP}$/ACC	Write Protect/Acceleration Pin, Flash
RY/$\overline{BY}$	Ready/Busy Output (Flash) Open Drain Output
Vccf	Power, Flash
Vccs	Power, SRAM
GND	Ground, Common

DEVICE BUS OPERATIONS

User Bus Operations (Flash and SRAM Operating with x16 Data Accesses)

OPERATION[1,3]	$\overline{CE}$f	$\overline{CE1}$s	CE2s	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$s	$\overline{UB}$s	DQ_0-DQ_7	DQ_8-DQ_{15}	$\overline{RESET}$	WP/ACC[5]
Full Standby	H	H	X	X	X	X	X	High-Z	High-Z	H	X
	H	X	L	X	X	X	X	High-Z	High-Z	H	X
Output Disable	H	L	H	H	H	X	X	High-Z	High-Z	H	X
	H	L	H	X	X	H	H	High-Z	High-Z	H	X
	L	H	X	H	H	X	X	High-Z	High-Z	H	X
	L	X	L	H	H	X	X	High-Z	High-Z	H	X
Read from Flash[2]	L	H	X	L	H	X	X	DOUT	DOUT	H	X
	L	X	L	L	H	X	X	DOUT	DOUT	H	X
Write to Flash	L	H	X	H	L	X	X	DIN	DIN	H	X
	L	X	L	H	L	X	X	DIN	DIN	H	X
Read from SRAM	H	L	H	L	H	L	L	DOUT	DOUT	H	X
	H	L	H	L	H	H	L	High-Z	DOUT	H	X
	H	L	H	L	H	L	H	DOUT	High-Z	H	X
Write to SRAM	H	L	H	X	L	L	L	DIN	DIN	H	X
	H	L	H	X	L	H	L	High-Z	DIN	H	X
	H	L	H	X	L	L	H	DIN	High-Z	H	X
Temporary Sector Group Unprotection[4]	X	X	X	X	X	X	X	X	X	V_{ID}[7]	X
Flash Hardware	X	H	X	X	X	X	X	High-Z	High-Z	L	X
Reset	X	X	L	X	X	X	X	High-Z	High-Z	L	X
Boot Block Sector Write Protection	X	X	X	X	X	X	X	X	X	X	L

Notes:

1. Any operations not indicated this column are inhibited..
2. $\overline{WE}$ can be VIL if $\overline{OE}$ is VIL, $\overline{OE}$ at VIH initiates the write operations.
3. Do not apply $\overline{CE}$f = VIL, $\overline{CE}$1s = VIL and CE2s = VIH all at once.
4. It is used for the extended sector group protections.
5. $\overline{WP}$/ACC = VIL: protection of boot sectors.
   $\overline{WP}$/ACC = VIH: removal of boot sectors protection.
   $\overline{WP}$/ACC = VACC (9V): Program time will reduce by 40%.
6. L = VIL, H = VIH, X = VIL or VIH.
7. See DC CHARACTERISTICS.

FLEXIBLE SECTOR-ERASE ARCHITECTURE ON FLASH MEMORY - Top Boot Block

Bank	Sector Address	K-Word	Address	Bank	Sector Address	K-Word	Address
BankA	SA70	4	1FF000h	BankB	SA34	32	110000h
BankA	SA69	4	1FE000h	BankB	SA33	32	108000h
BankA	SA68	4	1FD000h	BankB	SA32	32	100000h
BankA	SA67	4	1FC000h	BankC	SA31	32	0F8000h
BankA	SA66	4	1FB000h	BankC	SA30	32	0F0000h
BankA	SA65	4	1FA000h	BankC	SA29	32	0E8000h
BankA	SA64	4	1F9000h	BankC	SA28	32	0E0000h
BankA	SA63	4	1F8000h	BankC	SA27	32	0D8000h
BankA	SA62	32	1F0000h	BankC	SA26	32	0D0000h
BankA	SA61	32	1E8000h	BankC	SA25	32	0C8000h
BankA	SA60	32	1E0000h	BankC	SA24	32	0C0000h
BankA	SA59	32	1D8000h	BankC	SA23	32	0B8000h
BankA	SA58	32	1D0000h	BankC	SA22	32	0B0000h
BankA	SA57	32	1C8000h	BankC	SA21	32	0A8000h
BankA	SA56	32	1C0000h	BankC	SA20	32	0A0000h
BankB	SA55	32	1B8000h	BankC	SA19	32	098000h
BankB	SA54	32	1B0000h	BankC	SA18	32	090000h
BankB	SA53	32	1A8000h	BankC	SA17	32	088000h
BankB	SA52	32	1A0000h	BankC	SA16	32	080000h
BankB	SA51	32	198000h	BankC	SA15	32	078000h
BankB	SA50	32	190000h	BankC	SA14	32	070000h
BankB	SA49	32	188000h	BankC	SA13	32	068000h
BankB	SA48	32	180000h	BankC	SA12	32	060000h
BankB	SA47	32	178000h	BankC	SA11	32	058000h
BankB	SA46	32	170000h	BankC	SA10	32	050000h
BankB	SA45	32	168000h	BankC	SA9	32	048000h
BankB	SA44	32	160000h	BankC	SA8	32	040000h
BankB	SA43	32	158000h	BankD	SA7	32	038000h
BankB	SA42	32	150000h	BankD	SA6	32	030000h
BankB	SA41	32	148000h	BankD	SA5	32	028000h
BankB	SA40	32	140000h	BankD	SA4	32	020000h
BankB	SA39	32	138000h	BankD	SA3	32	018000h
BankB	SA38	32	130000h	BankD	SA2	32	010000h
BankB	SA37	32	128000h	BankD	SA1	32	008000h
BankB	SA36	32	120000h	BankD	SA0	32	000000h
BankB	SA35	32	118000h				

FLEXIBLE SECTOR-ERASE ARCHITECTURE ON FLASH MEMORY - Bottom Boot Block

Bank	Sector Address	K-Word	Address	Bank	Sector Address	K-Word	Address
BankD	SA70	32	1F8000h	BankB	SA35	32	0E0000h
BankD	SA69	32	1F0000h	BankB	SA34	32	0D8000h
BankD	SA68	32	1E8000h	BankB	SA33	32	0D0000h
BankD	SA67	32	1E0000h	BankB	SA32	32	0C8000h
BankD	SA66	32	1D8000h	BankB	SA31	32	0C0000h
BankD	SA65	32	1D0000h	BankB	SA30	32	0B8000h
BankD	SA64	32	1C8000h	BankB	SA29	32	0B0000h
BankD	SA63	32	1C0000h	BankB	SA28	32	0A8000h
BankC	SA62	32	1B8000h	BankB	SA27	32	0A0000h
BankC	SA61	32	1B0000h	BankB	SA26	32	098000h
BankC	SA60	32	1A8000h	BankB	SA25	32	090000h
BankC	SA59	32	1A0000h	BankB	SA24	32	088000h
BankC	SA58	32	198000h	BankB	SA23	32	080000h
BankC	SA57	32	190000h	BankB	SA22	32	078000h
BankC	SA56	32	188000h	BankB	SA21	32	070000h
BankC	SA55	32	180000h	BankB	SA20	32	068000h
BankC	SA54	32	178000h	BankB	SA19	32	060000h
BankC	SA53	32	170000h	BankB	SA18	32	058000h
BankC	SA52	32	168000h	BankB	SA17	32	050000h
BankC	SA51	32	160000h	BankB	SA16	32	048000h
BankC	SA50	32	158000h	BankB	SA15	32	040000h
BankC	SA49	32	150000h	BankA	SA14	32	038000h
BankC	SA48	32	148000h	BankA	SA13	32	030000h
BankC	SA47	32	140000h	BankA	SA12	32	028000h
BankC	SA46	32	138000h	BankA	SA11	32	020000h
BankC	SA45	32	130000h	BankA	SA10	32	018000h
BankC	SA44	32	128000h	BankA	SA9	32	010000h
BankC	SA43	32	120000h	BankA	SA8	32	008000h
BankC	SA42	32	118000h	BankA	SA7	4	007000h
BankC	SA41	32	110000h	BankA	SA6	4	006000h
BankC	SA40	32	108000h	BankA	SA5	4	005000h
BankC	SA39	32	100000h	BankA	SA4	4	004000h
BankB	SA38	32	0F8000h	BankA	SA3	4	003000h
BankB	SA37	32	0F0000h	BankA	SA2	4	002000h
BankB	SA36	32	0E8000h	BankA	SA1	4	001000h
				BankA	SA0	4	000000h

USER CONFIGURABLE BANK ARCHITECTURE TABLE

	Bank 1		Bank 2	
Bank Split	**Volume**	**Combination**	**Volume**	**Combination**
1	4 Mbit	Bank A	28 Mbit	Bank B, C, D
2	12 Mbit	Bank B	20 Mbit	Bank A, C, D
3	12 Mbit	Bank C	20 Mbit	Bank A, B, D
4	4 Mbit	Bank D	28 Mbit	Bank A, B, C

EXAMPLE OF VIRTUAL BANKS COMBINATION TABLE

	Bank 1			Bank 2		
Bank Split	**Volume**	**Combination**	**Sector Size**	**Volume**	**Combination**	**Sector Size**
1	4 Mbit	Bank A	8x8 Kbyte/4 Kword 7x64 Kbyte/32 Kword	28 Mbit	Bank B, C, D	56x64 Kbyte/32 Kword
2	8 Mbit	Bank A,D	8x8 Kbyte/4 Kword 15x64 Kbyte/32 Kword	24 Mbit	Bank B,C	48x64 Kbyte/32 Kword
3	16 Mbit	Bank A,B	8x8 Kbyte/4 Kword 31x64 Kbyte/32 Kword	16 Mbit	Bank C, D	32x64 Kbyte/32 Kword

Notes:

1) When multiple sector erase over several banks is operated, the system cannot read out of the bank to which a sector being erased belongs. For example, if erasing is taking place at both Bank A and Bank B, neither Bank A nor Bank B is read out. They would output the sequence flag once they were selected. Meanwhile the system would get to read from either Bank C or Bank D.

2) Each word is made of 2 Bytes: one upper Byte and one lower Byte. A Kword is 2^{10} words.

SECTOR ADDRESS TABLE - TOP BOOT TYPE

		Bank Address			Sector Address							Address Range
Bank	**Sector**	**A20**	**A19**	**A18**	**A17**	**A16**	**A15**	**A14**	**A13**	**A12**	**A11**	**Word Mode**
Bank D	SA0	0	0	0	0	0	0	X	X	X	X	000000h to 007FFFh
Bank D	SA1	0	0	0	0	0	1	X	X	X	X	008000h to 00FFFFh
Bank D	SA2	0	0	0	0	1	0	X	X	X	X	010000h to 017FFFh
Bank D	SA3	0	0	0	0	1	1	X	X	X	X	018000h to 01FFFFh
Bank D	SA4	0	0	0	1	0	0	X	X	X	X	020000h to 027FFFh
Bank D	SA5	0	0	0	1	0	1	X	X	X	X	028000h to 02FFFFh
Bank D	SA6	0	0	0	1	1	0	X	X	X	X	030000h to 037FFFh
Bank D	SA7	0	0	0	1	1	1	X	X	X	X	038000h to 03FFFFh
Bank C	SA8	0	0	1	0	0	0	X	X	X	X	040000h to 047FFFh
Bank C	SA9	0	0	1	0	0	1	X	X	X	X	048000h to 04FFFFh
Bank C	SA10	0	0	1	0	1	0	X	X	X	X	050000h to 057FFFh
Bank C	SA11	0	0	1	0	1	1	X	X	X	X	058000h to 05FFFFh
Bank C	SA12	0	0	1	1	0	0	X	X	X	X	060000h to 067FFFh
Bank C	SA13	0	0	1	1	0	1	X	X	X	X	068000h to 06FFFFh
Bank C	SA14	0	0	1	1	1	0	X	X	X	X	070000h to 077FFFh
Bank C	SA15	0	0	1	1	1	1	X	X	X	X	078000h to 077FFFh
Bank C	SA16	0	1	0	0	0	0	X	X	X	X	080000h to 087FFFh
Bank C	SA17	0	1	0	0	0	1	X	X	X	X	088000h to 08FFFFh
Bank C	SA18	0	1	0	0	1	0	X	X	X	X	090000h to 097FFFh
Bank C	SA19	0	1	0	0	1	1	X	X	X	X	098000h to 09FFFFh
Bank C	SA20	0	1	0	1	0	0	X	X	X	X	0A0000h to 0A7FFFh
Bank C	SA21	0	1	0	1	0	1	X	X	X	X	0A8000h to 0AFFFFh
Bank C	SA22	0	1	0	1	1	0	X	X	X	X	0B0000h to 0B7FFFh
Bank C	SA23	0	1	0	1	1	1	X	X	X	X	0B8000h to 0BFFFFh
Bank C	SA24	0	1	1	0	0	0	X	X	X	X	0C0000h to 0C7FFFh
Bank C	SA25	0	1	1	0	0	1	X	X	X	X	0C8000h to 0CFFFFh
Bank C	SA26	0	1	1	0	1	0	X	X	X	X	0D0000h to 0D7FFFh
Bank C	SA27	0	1	1	0	1	1	X	X	X	X	0D8000h to 0DFFFFh
Bank C	SA28	0	1	1	1	0	0	X	X	X	X	0E0000h to 0E7FFFh
Bank C	SA29	0	1	1	1	0	1	X	X	X	X	0E8000h to 0EFFFFh
Bank C	SA30	0	1	1	1	1	0	X	X	X	X	0F0000h to 0F7FFFh
Bank C	SA31	0	1	1	1	1	1	X	X	X	X	0F8000h to 0FFFFFh

SECTOR ADDRESS TABLE - TOP BOOT TYPE (Continued)

		Bank Address			Sector Address							Address Range
Bank	**Sector**	**A20**	**A19**	**A18**	**A17**	**A16**	**A15**	**A14**	**A13**	**A12**	**A11**	**Word Mode**
Bank B	SA32	1	0	0	0	0	0	X	X	X	X	100000h to 107FFFh
Bank B	SA33	1	0	0	0	0	1	X	X	X	X	108000h to 10FFFFh
Bank B	SA34	1	0	0	0	1	0	X	X	X	X	110000h to 117FFFh
Bank B	SA35	1	0	0	0	1	1	X	X	X	X	118000h to 11FFFFh
Bank B	SA36	1	0	0	1	0	0	X	X	X	X	120000h to 127FFFh
Bank B	SA37	1	0	0	1	0	1	X	X	X	X	128000h to 12FFFFh
Bank B	SA38	1	0	0	1	1	0	X	X	X	X	130000h to 137FFFh
Bank B	SA39	1	0	0	1	1	1	X	X	X	X	138000h to 13FFFFh
Bank B	SA40	1	0	1	0	0	0	X	X	X	X	140000h to 147FFFh
Bank B	SA41	1	0	1	0	0	1	X	X	X	X	148000h to 14FFFFh
Bank B	SA42	1	0	1	0	1	0	X	X	X	X	150000h to 157FFFh
Bank B	SA43	1	0	1	0	1	1	X	X	X	X	158000h to 15FFFFh
Bank B	SA44	1	0	1	1	0	0	X	X	X	X	160000h to 167FFFh
Bank B	SA45	1	0	1	1	0	1	X	X	X	X	168000h to 16FFFFh
Bank B	SA46	1	0	1	1	1	0	X	X	X	X	170000h to 177FFFh
Bank B	SA47	1	0	1	1	1	1	X	X	X	X	178000h to 17FFFFh
Bank B	SA48	1	1	0	0	0	0	X	X	X	X	180000h to 187FFFh
Bank B	SA49	1	1	0	0	0	1	X	X	X	X	188000h to 18FFFFh
Bank B	SA50	1	1	0	0	1	0	X	X	X	X	190000h to 197FFFh
Bank B	SA51	1	1	0	0	1	1	X	X	X	X	198000h to 19FFFFh
Bank B	SA52	1	1	0	1	0	0	X	X	X	X	1A0000h to 1A7FFFh
Bank B	SA53	1	1	0	1	0	1	X	X	X	X	1A8000h to 1AFFFFh
Bank B	SA54	1	1	0	1	1	0	X	X	X	X	1B0000h to 1B7FFFh
Bank B	SA55	1	1	0	1	1	1	X	X	X	X	1B8000h to 1BFFFFh
Bank A	SA56	1	1	1	0	0	0	X	X	X	X	1C0000h to 1C7FFFh
Bank A	SA57	1	1	1	0	0	1	X	X	X	X	1C8000h to 1CFFFFh
Bank A	SA58	1	1	1	0	1	0	X	X	X	X	1D0000h to 1D7FFFh
Bank A	SA59	1	1	1	0	1	1	X	X	X	X	1D8000h to 1DFFFFh
Bank A	SA60	1	1	1	1	0	0	X	X	X	X	1E0000h to 1E7FFFh
Bank A	SA61	1	1	1	1	0	1	X	X	X	X	1E8000h to 1EFFFFh
Bank A	SA62	1	1	1	1	1	0	X	X	X	X	1F0000h to 1F7FFFh
Bank A	SA63	1	1	1	1	1	1	0	0	0	X	1F8000h to 1F8FFFh
Bank A	SA64	1	1	1	1	1	1	0	0	1	X	1F9000h to 1F9FFFh
Bank A	SA65	1	1	1	1	1	1	0	1	0	X	1FA000h to 1FAFFFh
Bank A	SA66	1	1	1	1	1	1	0	1	1	X	1FB000h to 1FBFFFh
Bank A	SA67	1	1	1	1	1	1	1	0	0	X	1FC000h to 1FCFFFh
Bank A	SA68	1	1	1	1	1	1	1	0	1	X	1FD000h to 1FDFFFh
Bank A	SA69	1	1	1	1	1	1	1	1	0	X	1FE000h to 1FEFFFh
Bank A	SA70	1	1	1	1	1	1	1	1	1	X	1FF000h to 1FFFFFh

SECTOR ADDRESS TABLE - BOTTOM BOOT TYPE

		Bank Address			Sector Address							Address Range
Bank	**Sector**	**A20**	**A19**	**A18**	**A17**	**A16**	**A15**	**A14**	**A13**	**A12**	**A11**	**Word Mode**
Bank D	SA70	1	1	1	1	1	1	X	X	X	X	1F8000h to 1FFFFFh
Bank D	SA69	1	1	1	1	1	0	X	X	X	X	1F0000h to 1F7FFFh
Bank D	SA68	1	1	1	1	0	1	X	X	X	X	1E8000h to 1EFFFFh
Bank D	SA67	1	1	1	1	0	0	X	X	X	X	1E0000h to 1E7FFFh
Bank D	SA66	1	1	1	0	1	1	X	X	X	X	1D8000h to 1DFFFFh
Bank D	SA65	1	1	1	0	1	0	X	X	X	X	1D0000h to 1D7FFFh
Bank D	SA64	1	1	1	0	0	1	X	X	X	X	1C8000h to 1CFFFFh
Bank D	SA63	1	1	1	0	0	0	X	X	X	X	1C0000h to 1C7FFFh
Bank C	SA62	1	1	0	1	1	1	X	X	X	X	1B8000h to 1BFFFFh
Bank C	SA61	1	1	0	1	1	0	X	X	X	X	1B0000h to 1B7FFFh
Bank C	SA60	1	1	0	1	0	1	X	X	X	X	1A8000h to 1AFFFFh
Bank C	SA59	1	1	0	1	0	0	X	X	X	X	1A0000h to 1A7FFFh
Bank C	SA58	1	1	0	0	1	1	X	X	X	X	198000h to 19FFFFh
Bank C	SA57	1	1	0	0	1	0	X	X	X	X	190000h to 197FFFh
Bank C	SA56	1	1	0	0	0	1	X	X	X	X	188000h to 18FFFFh
Bank C	SA55	1	1	0	0	0	0	X	X	X	X	180000h to 187FFFh
Bank C	SA54	1	0	1	1	1	1	X	X	X	X	178000h to 17FFFFh
Bank C	SA53	1	0	1	1	1	0	X	X	X	X	170000h to 177FFFh
Bank C	SA52	1	0	1	1	0	1	X	X	X	X	168000h to 16FFFFh
Bank C	SA51	1	0	1	1	0	0	X	X	X	X	160000h to 167FFFh
Bank C	SA50	1	0	1	0	1	1	X	X	X	X	158000h to 15FFFFh
Bank C	SA49	1	0	1	0	1	0	X	X	X	X	150000h to 157FFFh
Bank C	SA48	1	0	1	0	0	1	X	X	X	X	148000h to 14FFFFh
Bank C	SA47	1	0	1	0	0	0	X	X	X	X	140000h to 147FFFh
Bank C	SA46	1	0	0	1	1	1	X	X	X	X	138000h to 13FFFFh
Bank C	SA45	1	0	0	1	1	0	X	X	X	X	130000h to 137FFFh
Bank C	SA44	1	0	0	1	0	1	X	X	X	X	128000h to 12FFFFh
Bank C	SA43	1	0	0	1	0	0	X	X	X	X	120000h to 127FFFh
Bank C	SA42	1	0	0	0	1	1	X	X	X	X	118000h to 11FFFFh
Bank C	SA41	1	0	0	0	1	0	X	X	X	X	110000h to 117FFFh
Bank C	SA40	1	0	0	0	0	1	X	X	X	X	108000h to 10FFFFh
Bank C	SA39	1	0	0	0	0	0	X	X	X	X	100000h to 107FFFh

SECTOR ADDRESS TABLE - BOTTOM BOOT TYPE (Continued)

		Bank Address			Sector Address							Address Range
Bank	**Sector**	**A20**	**A19**	**A18**	**A17**	**A16**	**A15**	**A14**	**A13**	**A12**	**A11**	**Word Mode**
Bank B	SA38	0	1	1	1	1	1	X	X	X	X	0F8000h to 0FFFFFh
Bank B	SA37	0	1	1	1	1	0	X	X	X	X	0F0000h to 0F7FFFh
Bank B	SA36	0	1	1	1	0	1	X	X	X	X	0E8000h to 0EFFFFh
Bank B	SA35	0	1	1	1	0	0	X	X	X	X	0E0000h to 0E7FFFh
Bank B	SA34	0	1	1	0	1	1	X	X	X	X	0D8000h to 0DFFFFh
Bank B	SA33	0	1	1	0	1	0	X	X	X	X	0D0000h to 0D7FFFh
Bank B	SA32	0	1	1	0	0	1	X	X	X	X	0C8000h to 0CFFFFh
Bank B	SA31	0	1	1	0	0	0	X	X	X	X	0C0000h to 0C7FFFh
Bank B	SA30	0	1	0	1	1	1	X	X	X	X	0B8000h to 0BFFFFh
Bank B	SA29	0	1	0	1	1	0	X	X	X	X	0B0000h to 0B7FFFh
Bank B	SA28	0	1	0	1	0	1	X	X	X	X	0A8000h to 0AFFFFh
Bank B	SA27	0	1	0	1	0	0	X	X	X	X	0A0000h to 0A7FFFh
Bank B	SA26	0	1	0	0	1	1	X	X	X	X	098000h to 09FFFFh
Bank B	SA25	0	1	0	0	1	0	X	X	X	X	090000h to 097FFFh
Bank B	SA24	0	1	0	0	0	1	X	X	X	X	088000h to 08FFFFh
Bank B	SA23	0	1	0	0	0	0	X	X	X	X	080000h to 087FFFh
Bank B	SA22	0	0	1	1	1	1	X	X	X	X	078000h to 07FFFFh
Bank B	SA21	0	0	1	1	1	0	X	X	X	X	070000h to 077FFFh
Bank B	SA20	0	0	1	1	0	1	X	X	X	X	068000h to 06FFFFh
Bank B	SA19	0	0	1	1	0	0	X	X	X	X	060000h to 067FFFh
Bank B	SA18	0	0	1	0	1	1	X	X	X	X	058000h to 05FFFFh
Bank B	SA17	0	0	1	0	1	0	X	X	X	X	050000h to 057FFFh
Bank B	SA16	0	0	1	0	0	1	X	X	X	X	048000h to 04FFFFh
Bank B	SA15	0	0	1	0	0	0	X	X	X	X	040000h to 047FFFh
Bank A	SA14	0	0	0	1	1	1	X	X	X	X	038000h to 03FFFFh
Bank A	SA13	0	0	0	1	1	0	X	X	X	X	030000h to 037FFFh
Bank A	SA12	0	0	0	1	0	1	X	X	X	X	028000h to 02FFFFh
Bank A	SA11	0	0	0	1	0	0	X	X	X	X	020000h to 027FFFh
Bank A	SA10	0	0	0	0	1	1	X	X	X	X	018000h to 01FFFFh
Bank A	SA9	0	0	0	0	1	0	X	X	X	X	010000h to 017FFFh
Bank A	SA8	0	0	0	0	0	1	X	X	X	X	008000h to 00FFFFh
Bank A	SA7	0	0	0	0	0	0	1	1	1	X	007000h to 007FFFh
Bank A	SA6	0	0	0	0	0	0	1	1	0	X	006000h to 006FFFh
Bank A	SA5	0	0	0	0	0	0	1	0	1	X	005000h to 005FFFh
Bank A	SA4	0	0	0	0	0	0	1	0	0	X	004000h to 004FFFh
Bank A	SA3	0	0	0	0	0	0	0	1	1	X	003000h to 003FFFh
Bank A	SA2	0	0	0	0	0	0	0	1	0	X	002000h to 002FFFh
Bank A	SA1	0	0	0	0	0	0	0	0	1	X	001000h to 001FFFh
Bank A	SA0	0	0	0	0	0	0	0	0	0	X	000000h to 000FFFh

SECTOR ADDRESS GROUP TABLE - TOP BOOT TYPE

Sector	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	Sectors
SGA0	0	0	0	0	0	0	X	X	X	SA0
SGA1	0	0	0	0	0 1 1	1 0 1	X	X	X	SA1 to SA3
SGA2	0	0	0	1	X	X	X	X	X	SA4 to SA7
SGA3	0	0	1	0	X	X	X	X	X	SA8 to SA11
SGA4	0	0	1	1	X	X	X	X	X	SA12 to SA15
SGA5	0	1	0	0	X	X	X	X	X	SA16 to SA19
SGA6	0	1	0	1	X	X	X	X	X	SA20 to SA23
SGA7	0	1	1	0	X	X	X	X	X	SA24 to SA27
SGA8	0	1	1	1	X	X	X	X	X	SA28 to SA31
SGA9	1	0	0	0	X	X	X	X	X	SA32 to SA35
SGA10	1	0	0	1	X	X	X	X	X	SA36 to SA39
SGA11	1	0	1	0	X	X	X	X	X	SA40 to SA43
SGA12	1	0	1	1	X	X	X	X	X	SA44 to SA47
SGA13	1	1	0	0	X	X	X	X	X	SA48 to SA51
SGA14	1	1	0	1	X	X	X	X	X	SA52 to SA55
SGA15	1	1	1	0	X	X	X	X	X	SA56 to SA59
SGA16	1	1	1	1	0 0 1	0 1 0	X	X	X	S60 to SA62
SGA17	1	1	1	1	1	1	0	0	0	SA63
SGA18	1	1	1	1	1	1	0	0	1	SA64
SGA19	1	1	1	1	1	1	0	1	0	SA65
SGA20	1	1	1	1	1	1	0	1	1	SA66
SGA21	1	1	1	1	1	1	1	0	0	SA67
SGA22	1	1	1	1	1	1	1	0	1	SA68
SGA23	1	1	1	1	1	1	1	1	0	SA69
SGA24	1	1	1	1	1	1	1	1	1	SA70

SECTOR ADDRESS GROUP TABLE - BOTTOM BOOT TYPE

Sector	A20	A19	A18	A17	A16	A15	A14	A13	A12	Sectors
SGA0	0	0	0	0	0	0	0	0	0	SA0
SGA1	0	0	0	0	0	0	0	0	1	SA1
SGA2	0	0	0	0	0	0	0	1	0	SA2
SGA3	0	0	0	0	0	0	0	1	1	SA3
SGA4	0	0	0	0	0	0	1	0	0	SA4
SGA5	0	0	0	0	0	0	1	0	1	SA5
SGA6	0	0	0	0	0	0	1	1	0	SA6
SGA7	0	0	0	0	0	0	1	1	1	SA7
SGA8	0	0	0	0	0 1 1	1 0 1	X	X	X	SA8 to SA10
SGA9	0	0	0	1	X	X	X	X	X	SA11 to SA14
SGA10	0	0	1	0	X	X	X	X	X	SA15 to SA18
SGA11	0	0	1	1	X	X	X	X	X	SA19 to SA22
SGA12	0	1	0	0	X	X	X	X	X	SA23 to SA26
SGA13	0	1	0	1	X	X	X	X	X	SA27 to SA30
SGA14	0	1	1	0	X	X	X	X	X	SA31 to SA34
SGA15	0	1	1	1	X	X	X	X	X	SA35 to SA38
SGA16	1	0	0	0	X	X	X	X	X	SA39 to SA42
SGA17	1	0	0	1	X	X	X	X	X	SA43 to SA46
SGA18	1	0	1	0	X	X	X	X	X	SA47 to SA50
SGA19	1	0	1	1	X	X	X	X	X	SA51 to SA54
SGA20	1	1	0	0	X	X	X	X	X	SA55 to SA58
SGA21	1	1	0	1	X	X	X	X	X	SA59 to SA62
SGA22	1	1	1	0	X	X	X	X	X	SA63 to SA66
SGA23	1	1	1	1	0 0 1	0 1 0	X	X	X	SA67 to SA69
SGA24	1	1	1	1	1	1	X	X	X	SA70

Sector Group Protection Verify Autoselect Codes Table (Top Boot Type)

Type	A20 to A12	A6	A3	A2	A1	A0	Code (HEX)
Manufacture's Code	BA	L	L	L	L	L	04h
Device Code	BA	L	L	L	L	H	227Eh
Extended Device	BA	L	H	H	H	L	220Ah
Code	BA	L	H	H	H	H	2201h
Sector Group Protection	SA	L	L	L	H	L	01h(1)

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Sector Group Protection Verify Autoselect Codes Table (Bottom Boot Type)

Type	A20 to A12	A6	A3	A2	A1	A0	Code (HEX)
Manufacture's Code	BA	L	L	L	L	L	04h
Device Code	BA	L	L	L	L	H	227Eh
Extended Device	BA	L	H	H	H	L	220Ah
Code	BA	L	H	H	H	H	2200h
Sector Group Protection	SA	L	L	L	H	L	01h(1)

Legend: L = VIL, H = VIH. See “n DC CHARACTERISTICS” for voltage levels.

Notes:

1. Outputs 01h at protected sector group addresses and outputs 00h at unprotected sector group addresses.
2. A read cycle at address (BA) 01h outputs device code. When 227Eh was output, this indicates that there will require two additional codes, called Extended Device Codes. Therefore the system may continue reading out these Extended Device Codes at the address of (BA) 0Eh, as well as at (BA) 0Fh.

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FLASH MEMORY COMMAND DEFINITIONS

Command Sequence	Bus Write Cycle Req'd	First Bus Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write		Fifth Bus Cycle		Sixth Bus Cycle	
		Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read / Reset (1)	1	XXXh	F0h	—	—	—	—	—	—	—	—	—	—
Read / Reset (1)	3	555h	AAh	2AAh	55h	555h	F0h	RA	RD	—	—	—	—
Autoselect	3	555h	AAh	2AAh	55h	(BA) 555h	90h	—	—	—	—	—	—
Program	4	555h	AAh	2AAh	55h	555h	A0h	PA	PD	—	—	—	—
Program Suspend	1	BA	B0h	—	—	—	—	—	—	—	—	—	—
Program Resume	1	BA	30h	—	—	—	—	—	—	—	—	—	—
Chip Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	555h	10h
Sector Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	SA	30h
Erase Suspend	1	BA	B0h	—	—	—	—	—	—	—	—	—	—
Erase Resume	1	BA	30h	—	—	—	—	—	—	—	—	—	—
Extended Sector Group Protection (3)	4	XXXh	60h	SGA	60h	SGA	40h	SGA	SD	—	—	—	—
Set to Fast Mode (2)	3	555h	AAh	2AAh	55h	555h	20h	—	—	—	—	—	—
Fast Program (2)	2	XXXh	A0h	PA	PD	—	—	—	—	—	—	—	—
Reset from Fast Mode (2)	2	BA	90h	XXXh	(6) F0H	—	—	—	—	—	—	—	—
Query (4)	1	(BA) 55h	98h	—	—	—	—	—	—	—	—	—	—
Hi-ROM Entry	3	555h	AAh	2AAh	55h	555h	88h	—	—	—	—	—	—
Hi-ROM Program (5)	4	555h	AAh	2AAh	55h	555h	A0h	(HRA) PA	PD	—	—	—	—
Hi-ROM Exit (5)	4	555h	AAh	2AAh	55h	(HRBA) 555h	90h	XXXh	00h	—	—	—	—

Notes:
1. Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.
2. This command is valid during Fast Mode.
3. This command is valid while $\overline{\text{RESET}}$ = V_{ID}
4. The valid address is A6 to A0.
5. This command is valid during Hi-ROM mode.
6. The data “00h” is also acceptable.

Address bits A11 to A20 = X = “H” or “L” for all address commands except for Program Address (PA), Sector Address (SA),and Bank Address (BA).

Bus operations are defined in “Device Bus Operations”.
RA = Address of the memory location to be read
PA = Address of the memory location to be programmed

Addresses are latched on the falling edge of the write pulse.

SA = Address of the sector to be erased.

The combination of A20, A19, A18, A17, A16, A15, A14, A13, and A12 will uniquely select any sector.

BA = Bank address (A18 to A20)
SGA = Sector group address to be protected.

Set sector group address (SGA) and (A6 , A3 , A2 , A1 ,A0) = (0, 0, 0, 1, 0) to protect

HRA= Address of the Hidden-ROM area
Top Boot Type
Word mode: 1FFF80h to 1FFFFFh

Bottom Boot Type
Word mode: 000000h to 00007Fh

HRBA = Bank address of the Hidden-ROM area
Top Boot Type:
A18 = A19 = A20 = 1

Bottom Boot Type:
A18 = A19 = A20 = 0

RD = Data read from location RA during read operation.
PD = Data to be programmed at location PA.
SD = Sector protection verify data.
Output 01h at protected sector addresses and output 00h at unprotected sector addresses.

The system should generate the following address patterns;
Word mode : 555h or 2AAh to addresses A0 to A10

MCP ABSOLUTE MAXIMUM RATINGS(1,2,3)

Symbol	Parameter	Value	Unit
T_{BIAS}	Temperature Under Bias	–30 to +85	°C
I_{OUT}	Output Current (per I/O)	100	mA
V_{IN}, V_{OUT}	Voltage Relative to GND for Data, Address and Control Pins	–0.3 to V_{CCf} + 0.3 –0.3 to V_{CCS} + 0.4	V V
V_{IN}	$\overline{RESET}$(5)	-0.5 TO +13.0	V
V_{IN}	$\overline{WP}$/ACC(6)	-0.5 TO +10.5	V
V_{CCf}/V_{CCS}	Voltage on Vcc Supply Relative to GND(4)	–0.3 to 3.5	V

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.
4. Minimum DC voltage on input or I/O pins is –0.3 V. During voltage transitions, input or I/O pins may undershoot GND to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{CCf}+0.3 V or V_{CCS}+0.4 V. During voltage transitions, input or I/O pins may overshoot to V_{CCf}+2.0 V or V_{CCS}+2.0 V for periods of up to 20 ns.
5. Minimum DC input voltage on RESET pin is –0.5 V. During voltage transitions, RESET pin may undershoot VSS to –2.0 V for periods of up to 20 ns. Voltage difference between input and supply voltage (V_{IN}-V_{CCf} or V_{CCS}) does not exceed 9.0 V. Maximum DC input voltage on RESET pin is +13.0 V which may overshoot to +14.0 V for periods of up to 20 ns.
6. Minimum DC input voltage on $\overline{WP}$/ACC pin is –0.5 V. During voltage transitions, $\overline{WP}$/ACC pin may undershoot GND to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on $\overline{WP}$/ACC pin is +10.5 V which may overshoot to +12.0V for periods of up to 20 ns, when V_{CCf} is applied.

MCP OPERATING RANGE

Range	Ambient Temperature	V_{CCF},V_{CCS}
Industrial	–30°C to +85°C	2.7–3.3V

STANDARD VOLTAGE RANGE: V_{CC} = 2.7-3.3 V

	Flash Memory	SRAM	Units
Max Access Time	70	70	ns
$\overline{CE}$ Access	70	70	ns
$\overline{OE}$ Access	30	35	ns

CAPACITANCE[1]

Symbol	Parameter	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	11	14	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	16	pF
$C_{IN}2$	Control Pin Capacitance	V_{IN} = 0V	14	16	pF
$C_{IN}3$	$\overline{WP}$/ACC Pin Capacitance	V_{IN} = 0V	21.5	26	pF

Notes:
1. Test conditions: T_A = 25°C, f = 1 MHz

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage	V_{IN}=V_{SS} to V_{CCf}, V_{CCS}	-1.0	1.0	µA
I_{LO}	Output Leakage	V_{OUT}=V_{SS} to V_{CCf}, V_{CCS}	-1.0	1.0	µA
V_{IL}	Input Low Level		-0.3	0.5	V
V_{IH}	Input High Level		2.0	V_{CC} ± 0.3[2]	V
V_{ID}	Voltage for Sector Protection, and Temporary Sector Unprotection ($\overline{RESET}$)[1]		11.5	12.5	V
V_{ACC}	Voltage for Program Acceleration ($\overline{WP}$/A_{CC})[1]		8.5	9.5	V
V_{OL}	Output Low (Flash) Output Low (SRAM)	V_{CCf} = V_{CCf} min., I_{OL} = 4.0 mA V_{CCS}=V_{CCS} min, I_{OL} = 0.1mA	— —	0.45 0.1	V V
V_{OH}	Output High (Flash) Output High (SRAM)	V_{CCf} = V_{CCf} min.,I_{OH} = -0.1mA V_{CCf} =V_{CCS} min, I_{OH} = -0.1mA	V_{CCf}-0.4 V_{CCS}-0.1	— —	V V
V_{LKO}	Flash Low V_{CCf}		2.3	2.5	V

Notes:
1. Only applicable with V_{CCf} applied.
2. Use indicates the lower voltage of V_{CCS} or V_{CCf}.

FLASH DC CHARACTERISTICS

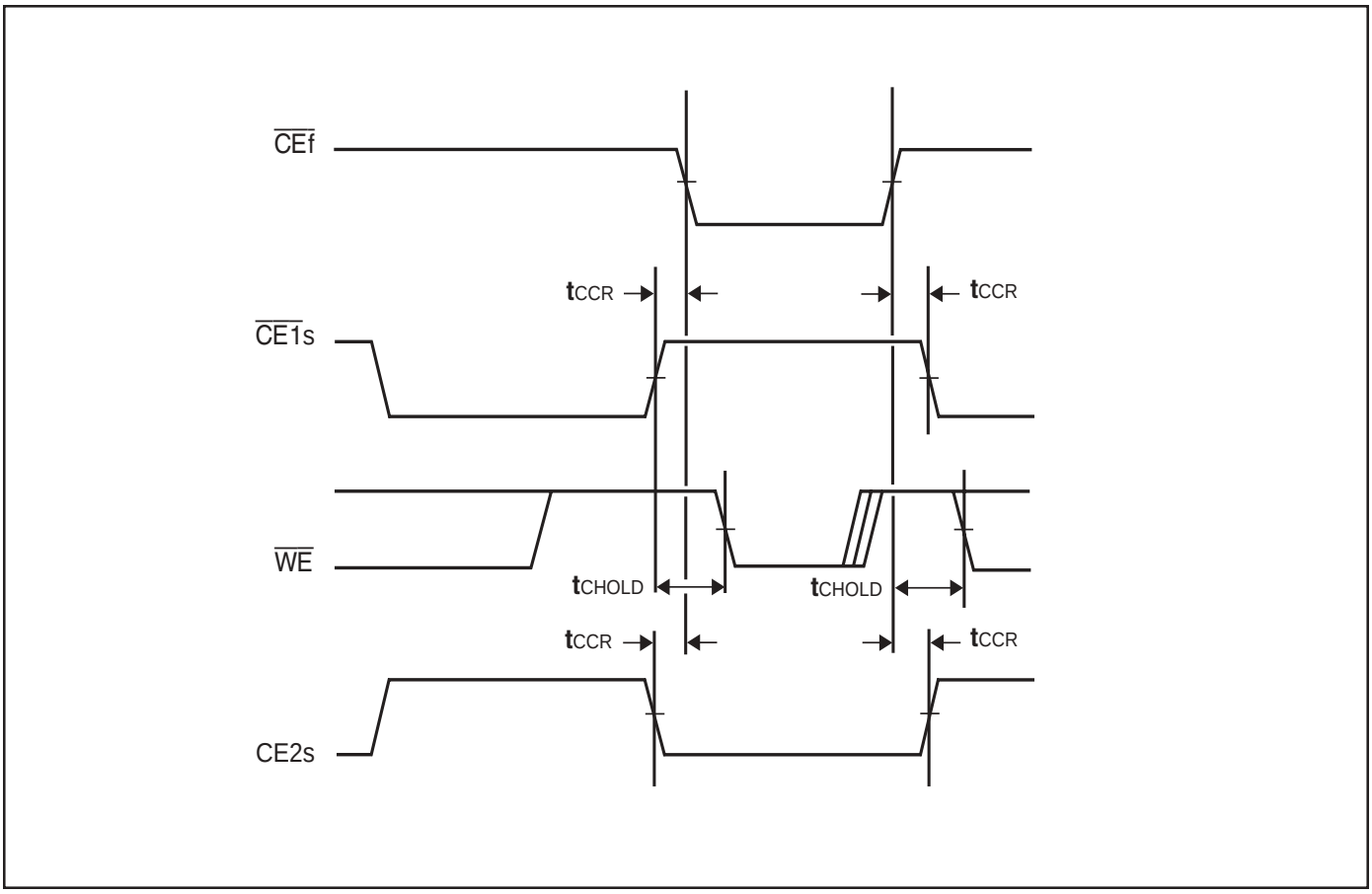
Symbol	Parameter	Test Conditions		Min.	Max.	Unit
I_{LIT}	$\overline{RESET}$ Inputs Leakage Current	V_{CCf}=V_{CCf} max., V_{CCs}=V_{CCs} max. $\overline{RESET}$ = 12.5V		—	35	µA
I_{ACC}	ACC Accelerated Program Current	V_{CCf}=V_{CCf} max., V_{CCs}=V_{CCs} max. $\overline{WP}$/ACC = Vacc max.		—	20	mA
I_{CC}1f	FLASH Vcc [1] Active Current (Read)	$\overline{CE}$f=V_{IL}	tCycle = 5Mhz Word	—	18	mA
		$\overline{OE}$=V_{IH}	tCycle = 1Mhz Word	—	4	
I_{CC}2f	FLASH Vcc Active[2] Current(Program/Erase)	$\overline{CE}$f=V_{IL} $\overline{OE}$=V_{IH}		—	25	mA
I_{CC}3f	FLASH Vcc Active[4] Current (Read-While-Program)	$\overline{CE}$f=V_{IL} $\overline{OE}$=V_{IH}	Word	—	43	mA
I_{CC}4f	FLASH Vcc Active[4] Current (Read-While-Erase)	$\overline{CE}$f=V_{IL} $\overline{OE}$=V_{IH}	Word	—	43	mA
I_{CC}5f	FLASH Vcc Active Current (Erase-Suspend-Program)	$\overline{CE}$f=V_{IL} $\overline{OE}$=V_{IH}		—	25	mA
I_{SB}1f	FLASH Vcc Standby Current	V_{CCf} = Vcc max, $\overline{CE}$f V_{CCf} ± 0.3V $\overline{RESET}$, $\overline{CE}$f, $\overline{WP}$/ACC = V_{CCf} ± 0.3V		—	5	µA
I_{SB}2f	FLASH Vcc Standby Current ($\overline{RESET}$)	V_{CCf} = Vcc max, $\overline{RESET}$= V_{SS} ± 0.3V $\overline{WP}$/ACC = V_{CCf} ± 0.3V		—	5	µA
I_{SB}3f (Auto Sleep Mode)	FLASH Vcc[3] Standby Current	V_{CCf} = Vcc max. $\overline{CE}$f, = V_{SS} ± 0.3V $\overline{RESET}$, $\overline{WP}$/ACC = V_{CCf} ± 0.3V V_{IN} = V_{CCf} ± 0.3V OR V_{SS} ± 0.3V		—	5	µA

Notes:
1. The ICC current listed includes both the DC operating current and the frequency dependent component.
2. ICC active while Embedded Algorithm (program or erase) is in progress.
3. Automatic sleep mode enables the low power mode when address remain stable for 150 ns..
4. Embedded Algorithm (program or erase) is in progress. (@5 MHz)

AC CHARACTERISTICS - $\overline{CE}$ TIMING

Parameter		Symbol	Condition	Min	Unit
$\overline{CE}$ Recover Time	_	t_{CCR}	_	0	ns
$\overline{CE}$ Hold Time	_	t_{CHOLD}	_	3	ns

Timing Diagram for Alternating SRAM to Flash



FLASH READ ONLY SWITCHING CHARACTERISTICS

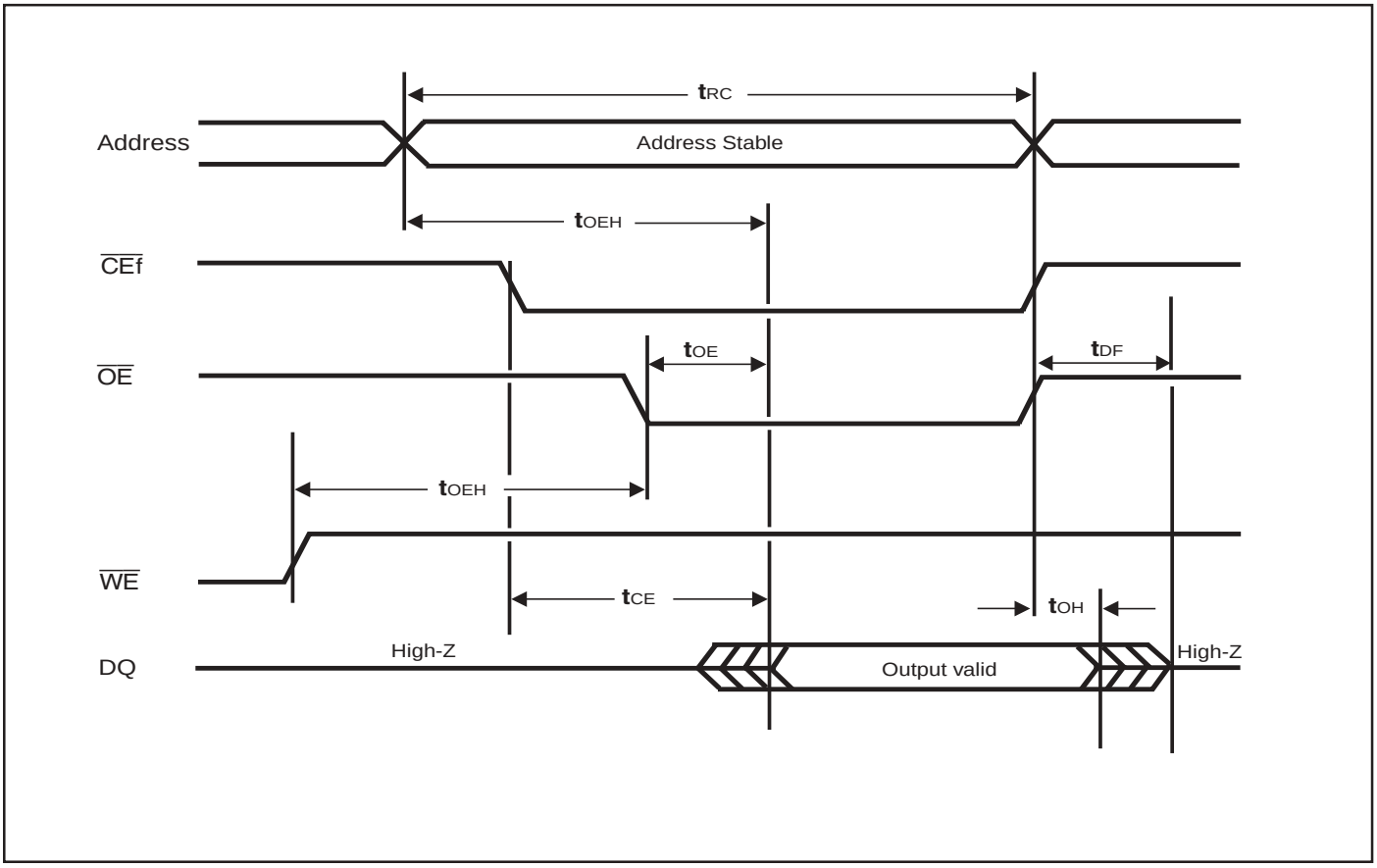
(Over Operating Range)

Symbol	Parameter	Min.	Max.	Unit
t_{RC}	Cycle Time	70	—	ns
t_{ACC}	Address to Output Delay	—	70	ns
t_{CE}	Chip Enable to Output Delay	—	70	ns
t_{OE}	Output Enable to Output Delay	—	30	ns
t_{DF}	Chip Enable to Output High-Z	—	25	ns
t_{DF}	Output Enable to Output High-Z	—	25	ns
t_{OH}	Output Hold Time from Addresses, $\overline{CE}$f or $\overline{OE}$, Whichever Occurs First	0	—	ns
t_{READY}	$\overline{RESET}$ Pin Low to Read Mode	—	20	µs

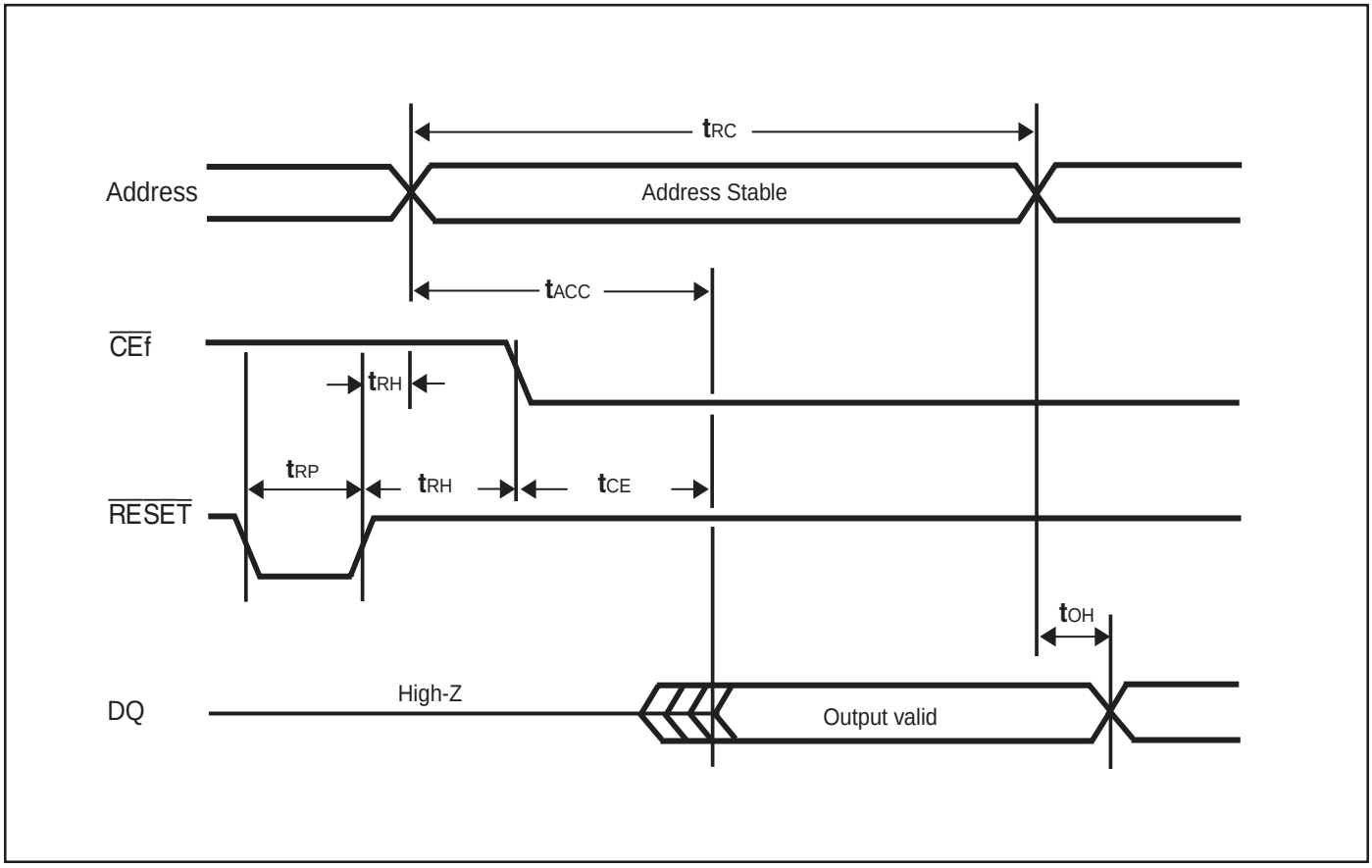
FLASH AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	5 ns
Input and Output Timing and Reference Level	0.5 x Vccf
Output Load	1 TTL gate and 30pF

FLASH READ CYCLE



FLASH HARDWARE $\overline{\text{RESET}}$ / READ OPERATION TIMING DIAGRAM



FLASH ERASE/PROGRAM OPERATION CHARACTERISTICS

(Over Operating Range)

Symbol	Parameter	-70 ns Min.	Typ.	Max.	Unit
t_{WC}	Write Cycle Time	70	-	-	ns
t_{AS}	Address Setup Time ($\overline{WE}$ to Addr.)	0	-	-	ns
t_{ASO}	Address Setup Time to $\overline{CE}$f Low During Toggle Bit Polling	12	-	-	ns
t_{AH}	Address Hold Time ($\overline{WE}$ to Addr.)	45	-	-	ns
t_{AHT}	Address Hold Time from $\overline{CE}$f or $\overline{OE}$ High During Toggle Bit Polling	0	-	-	ns
t_{DS}	Data Setup Time	30	-	-	ns
t_{DH}	Data Hold Time	0	-	-	ns
t_{OES}	Output Enable Setup Time	0	-	-	ns
t_{OEH}	Output Enable Hold Time Read	0	-	-	ns
t_{OEH}	Output Enable Hold Time Toggle and $\overline{Data}$ Polling	10	-	-	ns
t_{CEPH}	$\overline{CE}$f High During Toggle Bit Polling	20	-	-	ns
t_{OEPH}	$\overline{OE}$ High During Toggle Bit Polling	20	-	-	ns
t_{GHEL}	Read Recover Time Before Write ($\overline{OE}$ to $\overline{CE}$f)	0	-	-	ns
t_{GHWL}	Read Recover Time Before Write ($\overline{OE}$ to $\overline{WE}$)	0	-	-	ns
t_{WS}	WE Setup Time (CEf to WE)	0	-	-	ns
t_{CS}	$\overline{CE}$f Setup Time (WE to CEf)	0	-	-	ns
t_{WH}	$\overline{WE}$ Hold Time (CEf to WE)	0	-	-	ns
t_{CH}	$\overline{CE}$f Hold Time (WE to CEf)	0	-	-	ns
t_{WP}	Write Pulse Width	35	-	-	ns
t_{CP}	$\overline{CE}$f Pulse Width	35	-	-	ns
t_{WPH}	Write Pulse Width High	25	-	-	ns
t_{CPH}	$\overline{CE}$f Pulse Width High	25	-	-	ns
t_{WHWH1}	Word Programming Operation (1)	-	6.0	100	µs
t_{WHWH2}	Sector Erase Operation (1)	-	0.5	2.0	s
t_{WHWH3}	Chip Programming Operation (1)	-	25.2	95	s
t_{VCS}	V_{CC}f Setup Time	50	-	-	µs

Note:

1. Does not include the preprogramming time.
2. This timing is for Sector Protection Operation.
3. The time between writes must be less than “tTOW ” otherwise that command will not be accepted and erasure will start. The Sector Erase command(s) would begin at time-out (tTOW) after the last rising edge of either $\overline{CE}$f or $\overline{WE}$ signals.
4. When the Erase Suspend command is written during the Sector Erase operation, the device will take a maximum of “tSPD ” to suspend the erase operation.

FLASH ERASE/PROGRAM OPERATION CHARACTERISTICS (Continued)

(Over Operating Range)

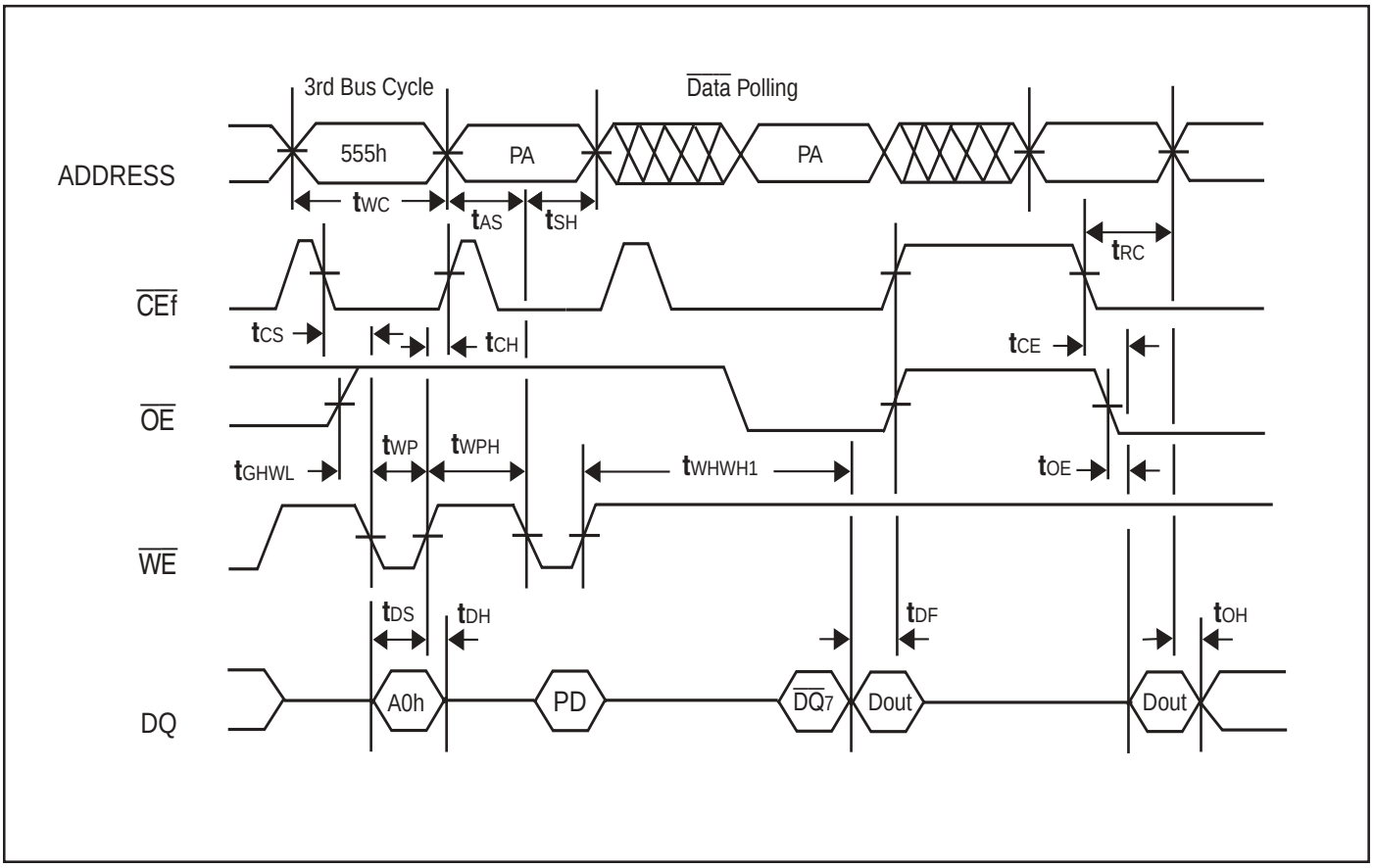
Symbol	Parameter	-70 ns Min.	-70 ns Max.	Unit
t_{VLHT}	Voltage Transition Time[2]	4	-	µs
t_{VIDR}	Rise Time to V_{ID}[2]	500	-	ns
t_{VACCR}	Rise Time to V_{ACC}	500	-	ns
t_{RB}	Recovery Time from RY/$\overline{BY}$	0	-	ns
t_{RP}	$\overline{RESET}$ Pulse Width	500	-	ns
t_{EOE}	Delay Time from Embedded Output Enable	-	70	ns
t_{RH}	$\overline{RESET}$ High Level Period Before Read	200	-	ns
t_{BUSY}	Program/Erase Valid to RY/$\overline{BY}$ Delay	-	90	ns
t_{TOW}	Erase Time-out Time [3]	50	-	µs
t_{SPD}	Erase Suspend Transition Time [4]	-	20	µs

Note:

1. This does not include the preprogramming time.
2. This timing is for Sector Protection Operation.
3. The time between writes must be less than “tTOW ” otherwise that command will not be accepted and erasure will start. The Sector Erase command(s) would begin at time-out (tTOW) after the last rising edge of either $\overline{CE}$f or $\overline{WE}$ signals.
4. When the Erase Suspend command is written during the Sector Erase operation, the device will take a maximum of “tSPD” to suspend the erase operation.

FLASH WRITE CYCLE

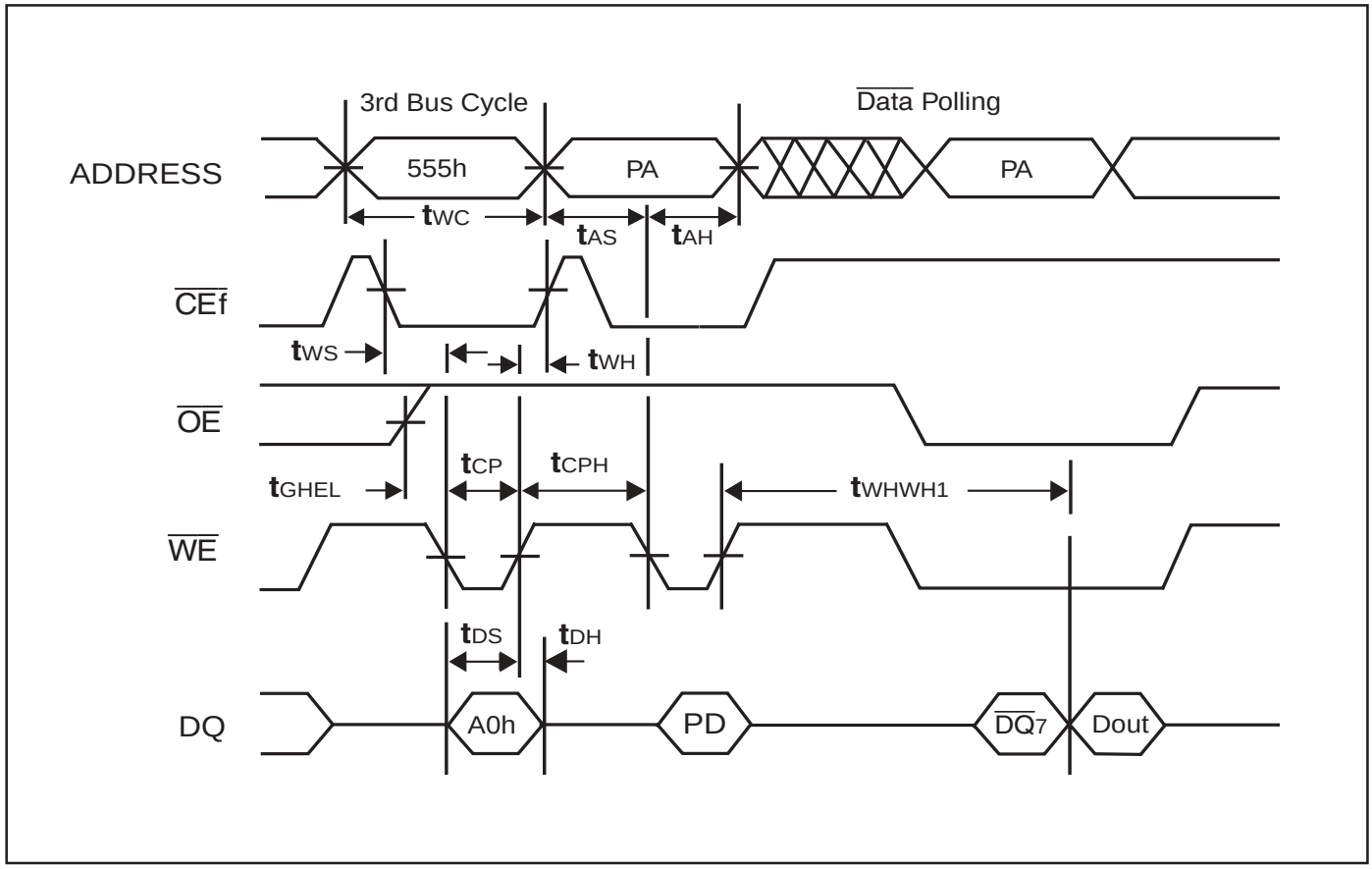
($\overline{WE}$ CONTROL)



Notes:

1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. DQ7 is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles out of four bus cycle sequence.
6. These waveforms are for the ×16 mode (the addresses differ from ×8 mode, i.e. AAAh).

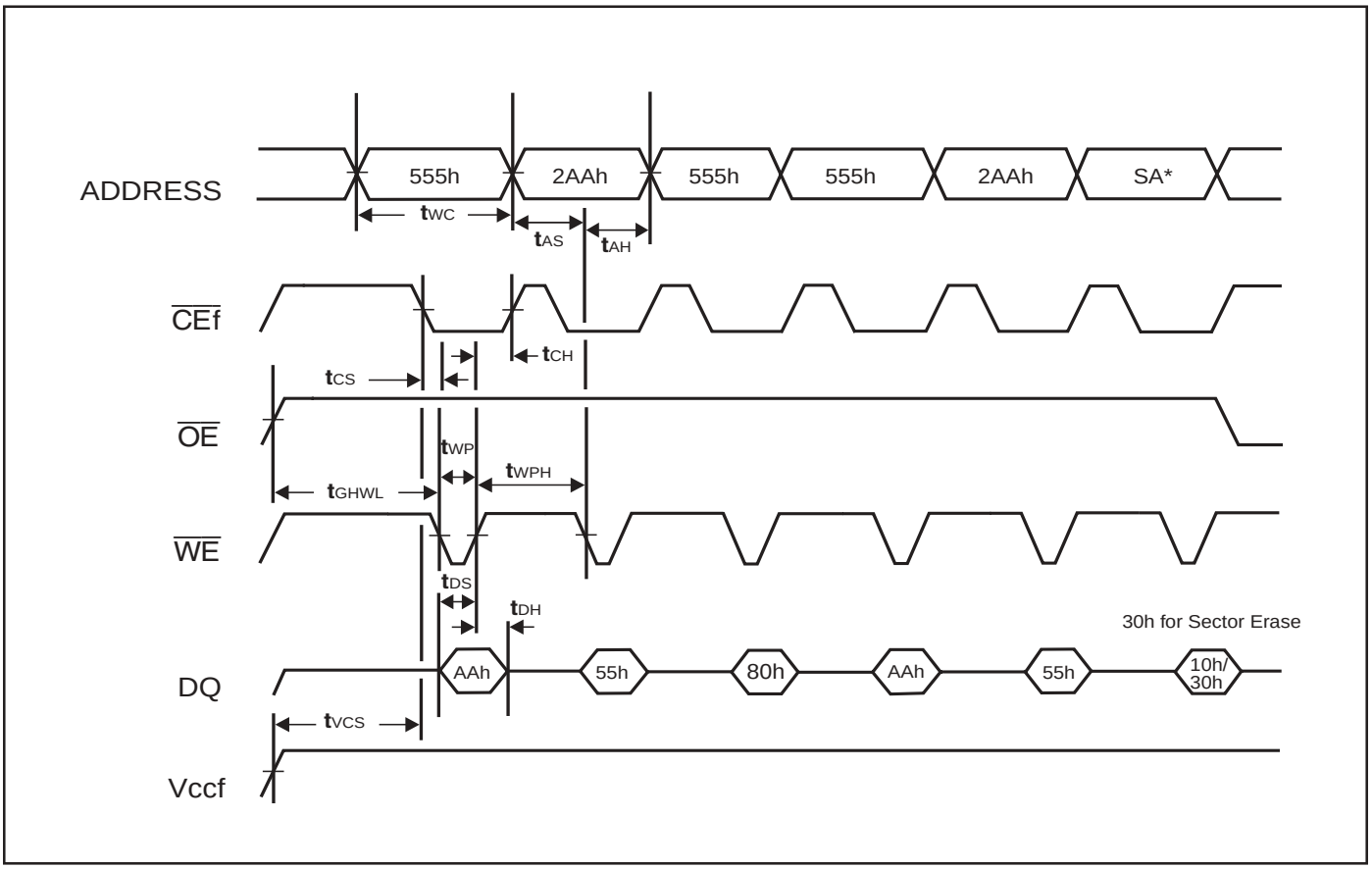
FLASH WRITE CYCLE ($\overline{CEf}$ CONTROL)



Notes:

1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. DQ7 is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles out of four bus cycle sequence.
6. These waveforms are for the ×16 mode.

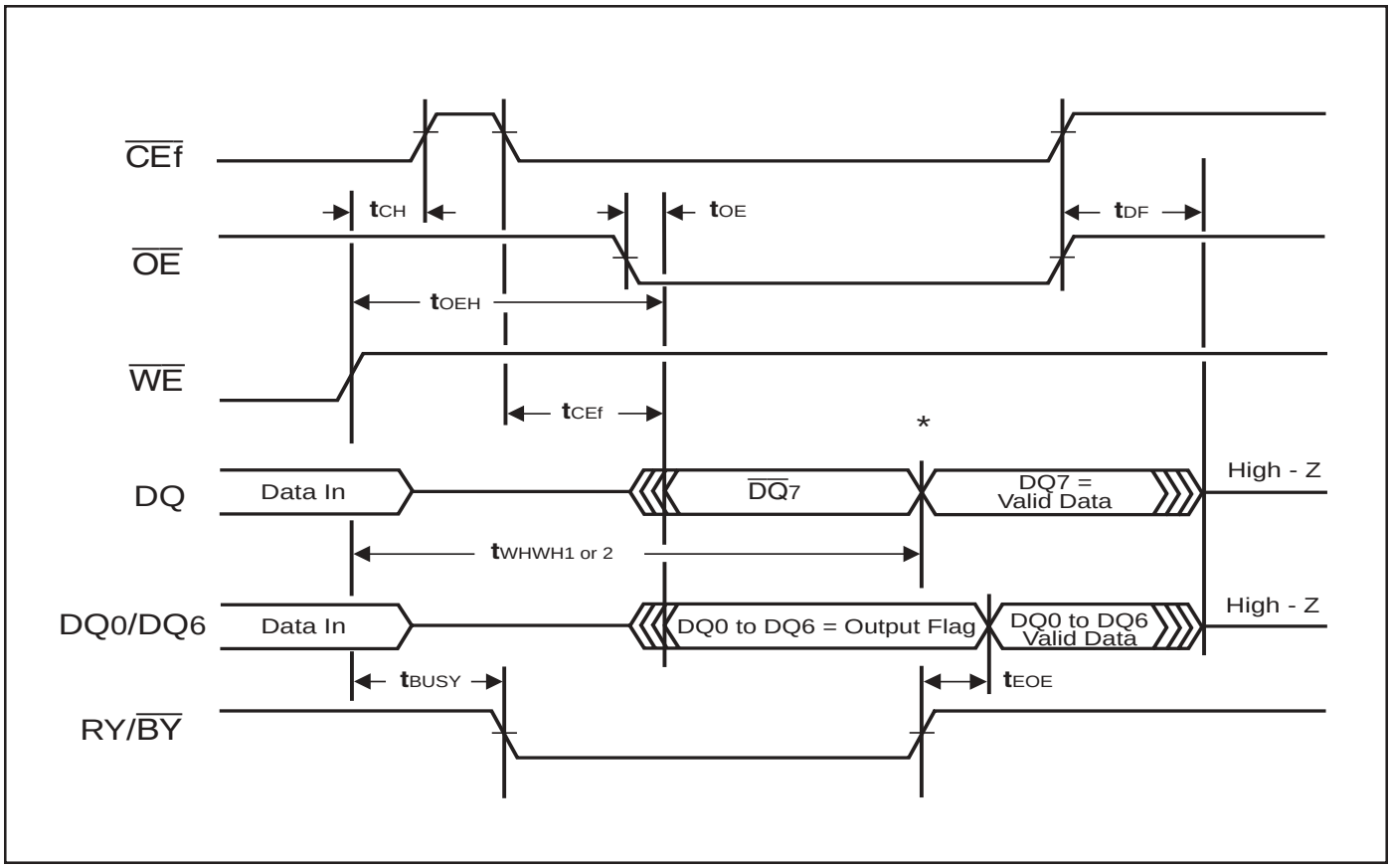
FLASH AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS



*SA is the sector address for Sector Erase. Address = 555h for Chip Erase.

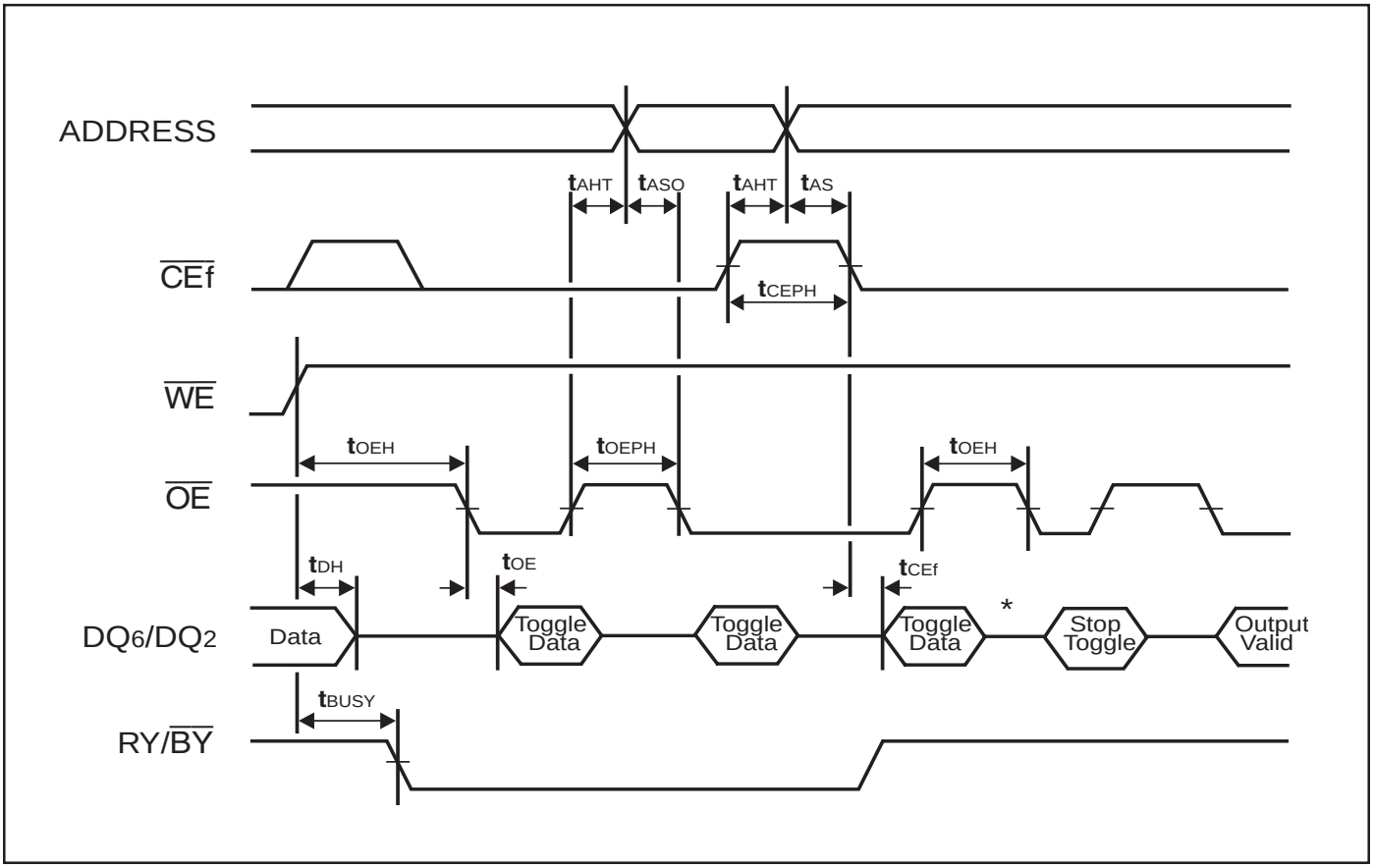
Note:
These waveforms are for the ×16 mode.

FLASH AC WAVEFORMS
FOR DATA POLLING DURING EMBEDDED ALOGRITHM OPERATIONS



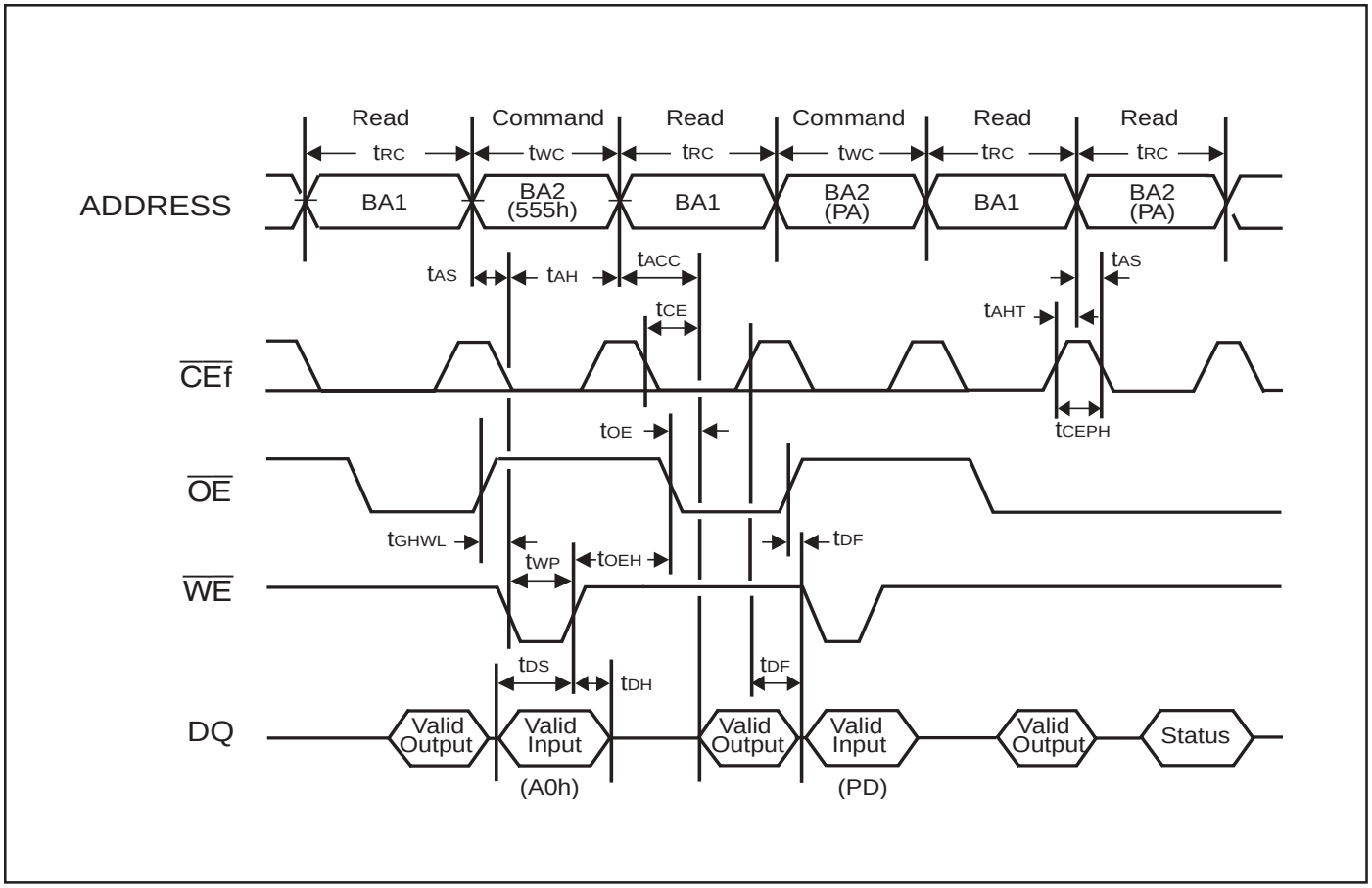
*DQ7 = Valid Data (the device has completed the Embedded operation.)

FLASH AC WAVEFORMS
FOR TOGGLE BIT DURING EMBEDDED ALGORITHM OPERATIONS



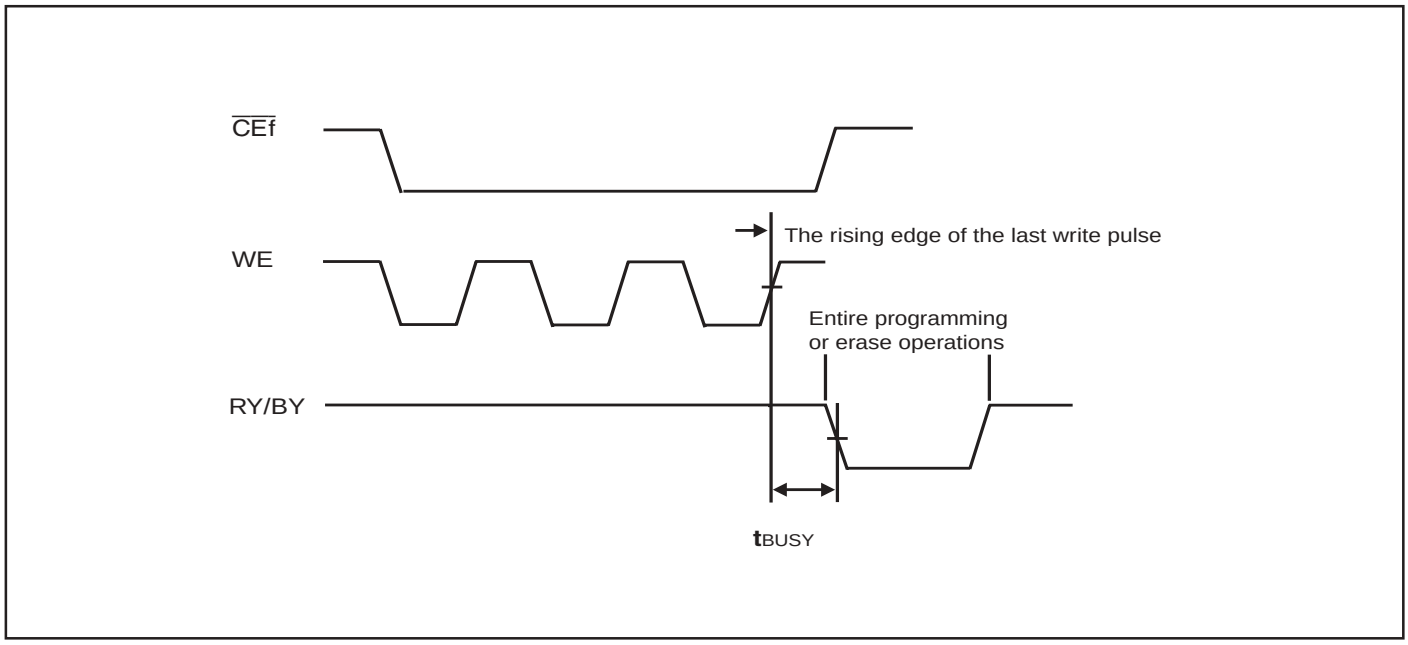
* DQ6 stops toggling (the device has completed the Embedded operation).

FLASH BACK-TO-BACK READ/WRITE TIMING DIAGRAM

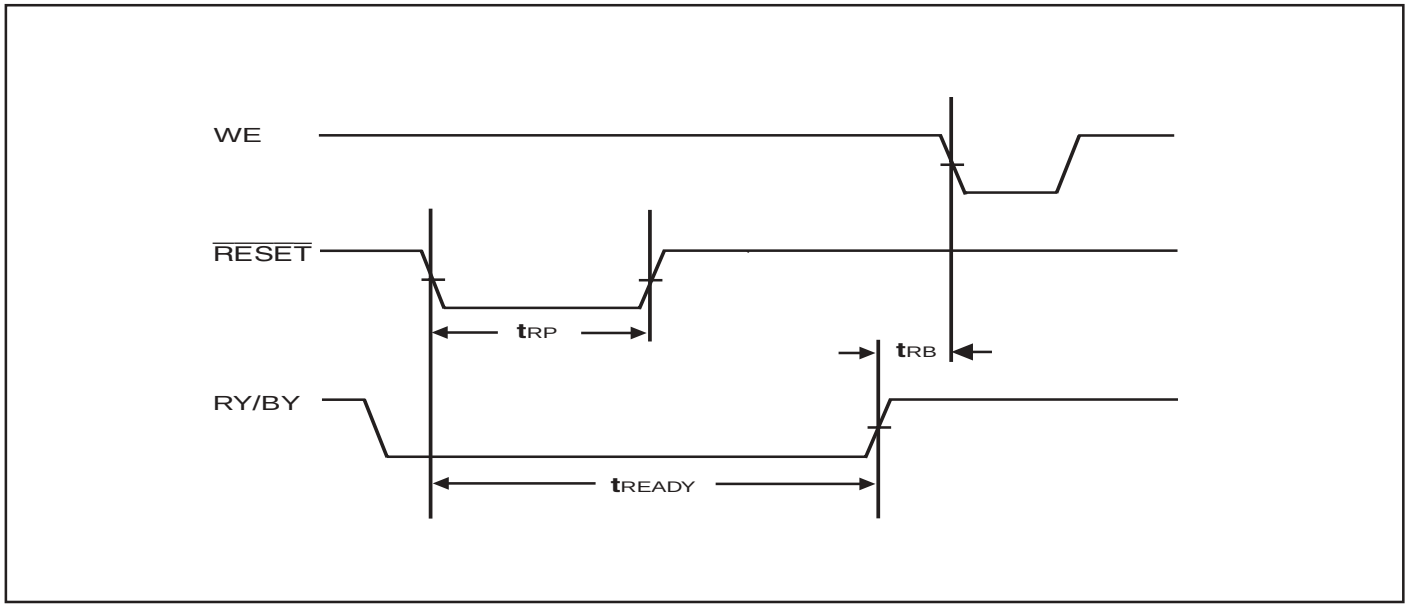


Note:
This is example of Read for Bank 1 and Embedded Algorithm (program) for Bank 2.
BA1: Address of Bank 1.
BA2: Address of Bank 2.

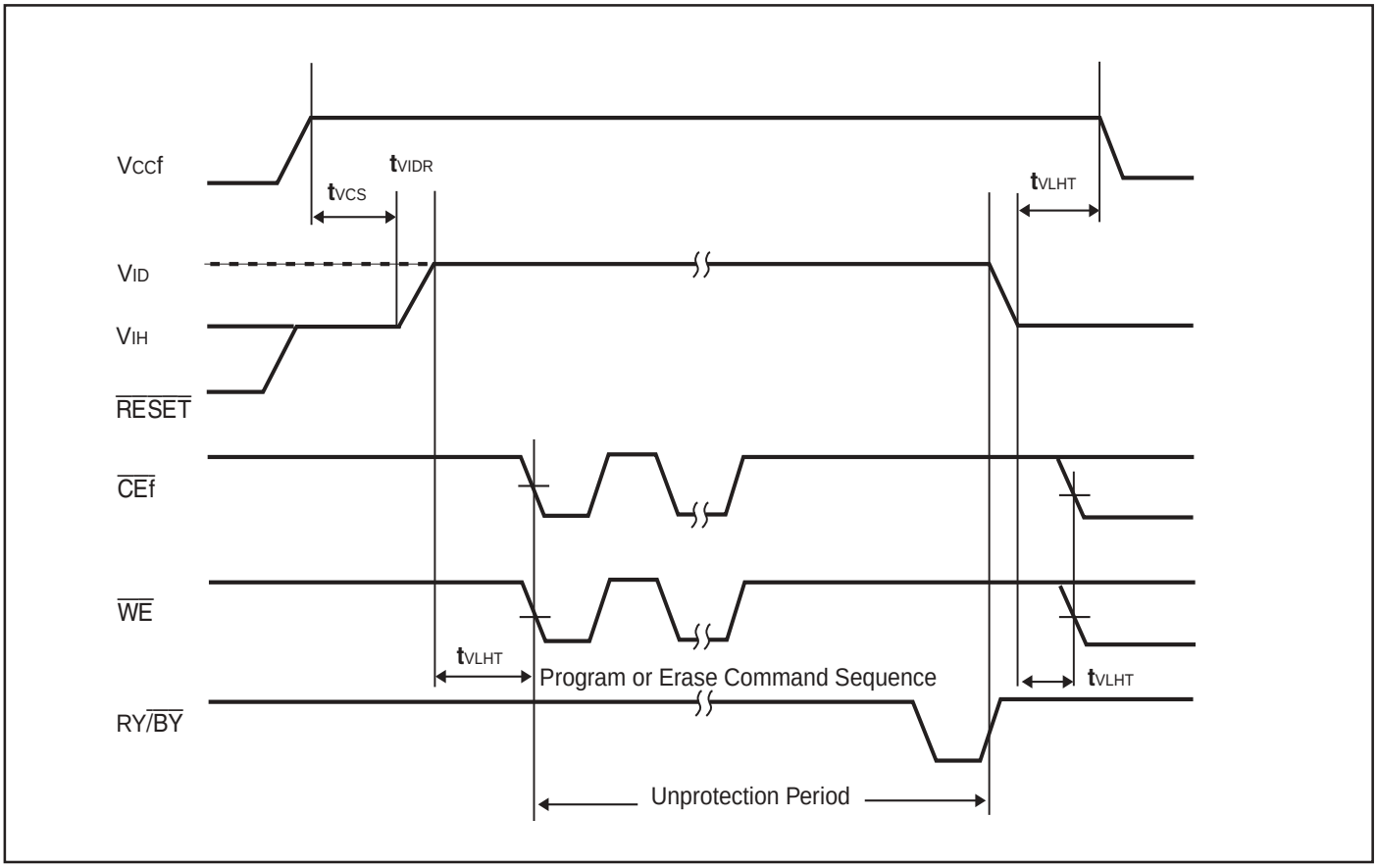
FLASH RY/$\overline{BY}$ TIMING DIAGRAM DURING WRITE/ERASE OPERATIONS



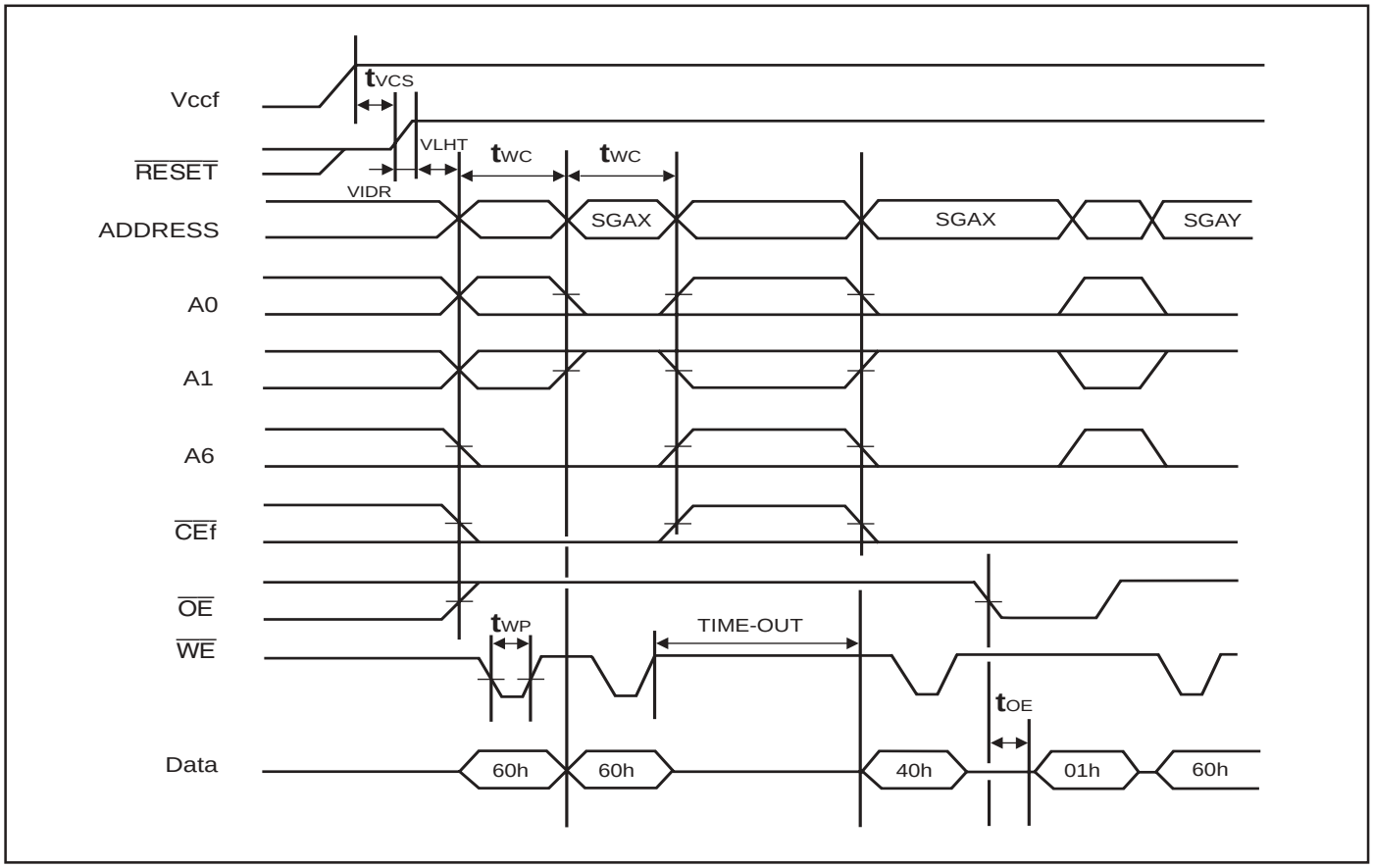
FLASH $\overline{RESET}$, RY/$\overline{BY}$ TIMING DIAGRAM



FLASH TEMPORARY SECTOR GROUP UNPROTECTION

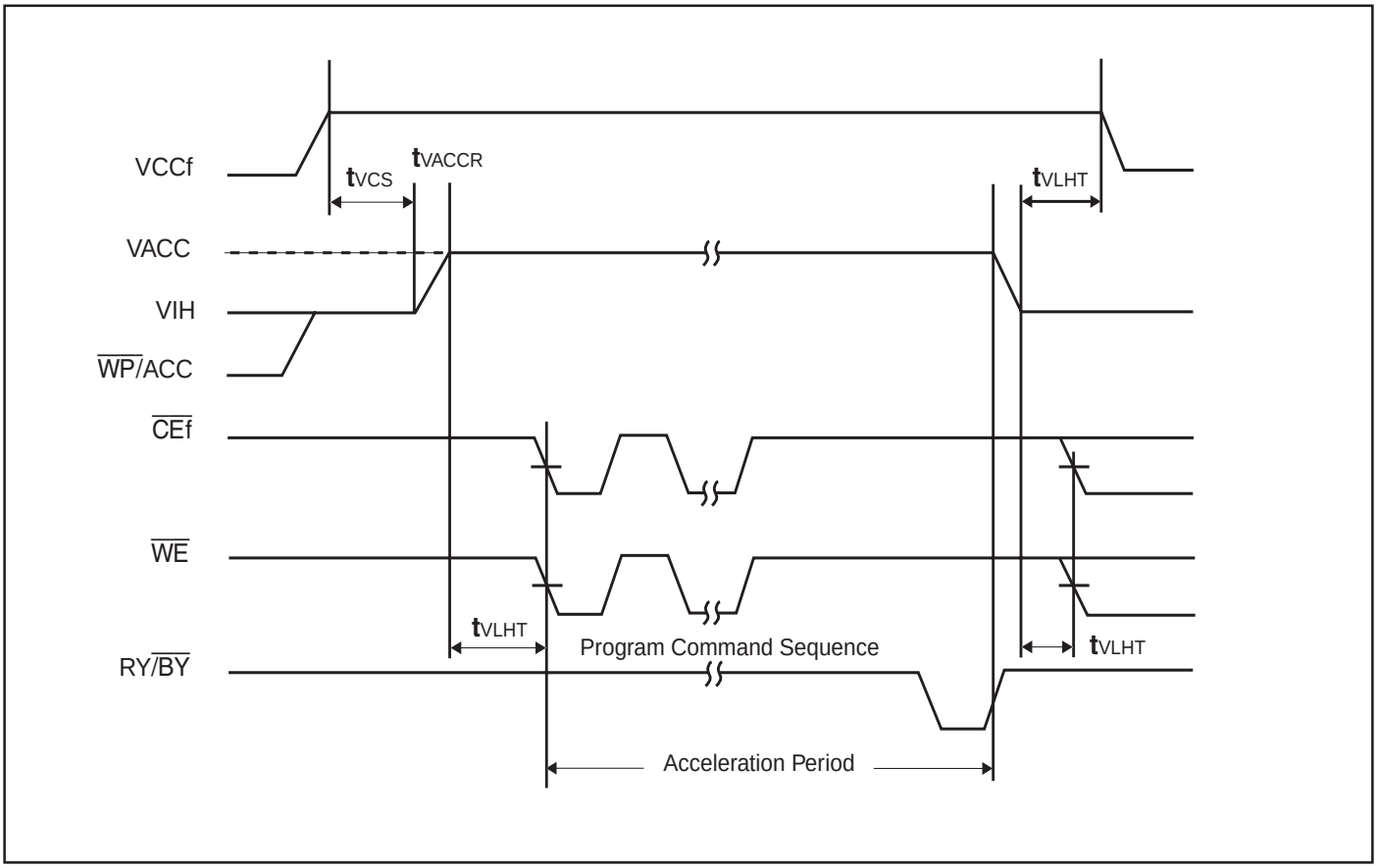


FLASH EXTENDED SECTOR GROUP PROTECTION



SGAx: Sector Group Address to be protected. SGAy: Next Group Sector Address to be protected
UNPROTECTION: Implement with A6 = 1, A1 = 1, A0 = 0. Time-out approximately 15 ms.
TIME-OUT : Time-Out window = 250 µs (Min.)

FLASH ACCELERATED PROGRAM



SRAM POWER SUPPLY CHARACTERISTICS

(Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I_{CC1}	Vcc Dynamic Operating Supply Current	V_{CCS} = V_{CCS} Max., $\overline{CE1}_s$ = V_{IL}, $CE2_s$ = V_{IH}, f = 10Mhz	—	40	mA
I_{CC2}	Operating Supply Current	V_{CCS} = Max., $\overline{CE1}_s$ = 0.2V, $CE2_s$ = V_{CCS} - 0.2V, f = 1Mhz	—	8	mA
I_{SB1}	CMOS Standby Current (CMOS Inputs)	V_{CCS} = V_{CCS} Max., $\overline{CE1}_s \geq V_{CCS} - 0.2V$, AND $CE2_s \geq V_{CCS} - 0.2V$, OR $CE2_s \leq 0.2V$,	—	10	µA

SRAM READ CYCLE SWITCHING CHARACTERISTICS(1)

(Over Operating Range)

		70 ns		
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
t_{RC}	Read Cycle Time	70	—	ns
t_{AA}	Address Access Time	—	70	ns
t_{OHA}	Output Hold Time	10	—	ns
t_{ACE1}	$\overline{CE1}_s$ Access Time	—	70	ns
t_{DOE}	$\overline{OE}$ Access Time	—	35	ns
t_{HZOE}(2)	$\overline{OE}$ to High-Z Output	—	25	ns
t_{LZOE}(2)	$\overline{OE}$ to Low-Z Output	0	—	ns
t_{HZCE1}(2)	$\overline{CE1}_s$ to High-Z Output	0	25	ns
t_{LZCE1}(2)	$\overline{CE1}_s$ to Low-Z Output	5	—	ns
t_{BA}	$\overline{LB}_s$, $\overline{UB}_s$ Access Time	—	70	ns
t_{HZB}	$\overline{LB}_s$, $\overline{UB}_s$ to High-Z Output	0	25	ns
t_{LZB}	$\overline{LB}_s$, $\overline{UB}_s$ to Low-Z Output	0	—	ns

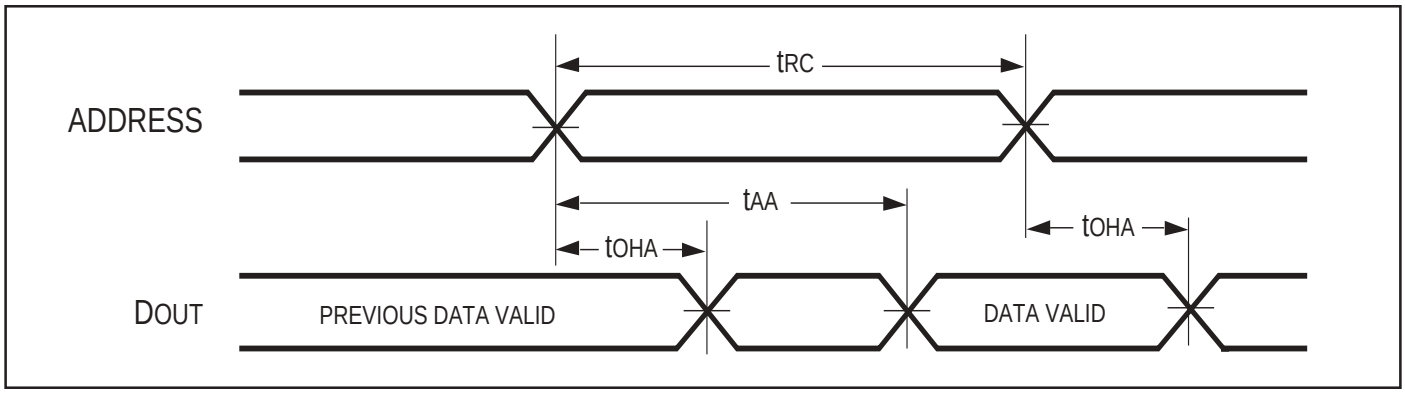
Notes:
1. See SRAM AC Test Conditions
2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

SRAM AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to Vccs
Input Rise and Fall Times	5 ns
Input and Output Timing and Reference Level	0.5 x V_{CC}
Output Load	1TTL gate and 30pf

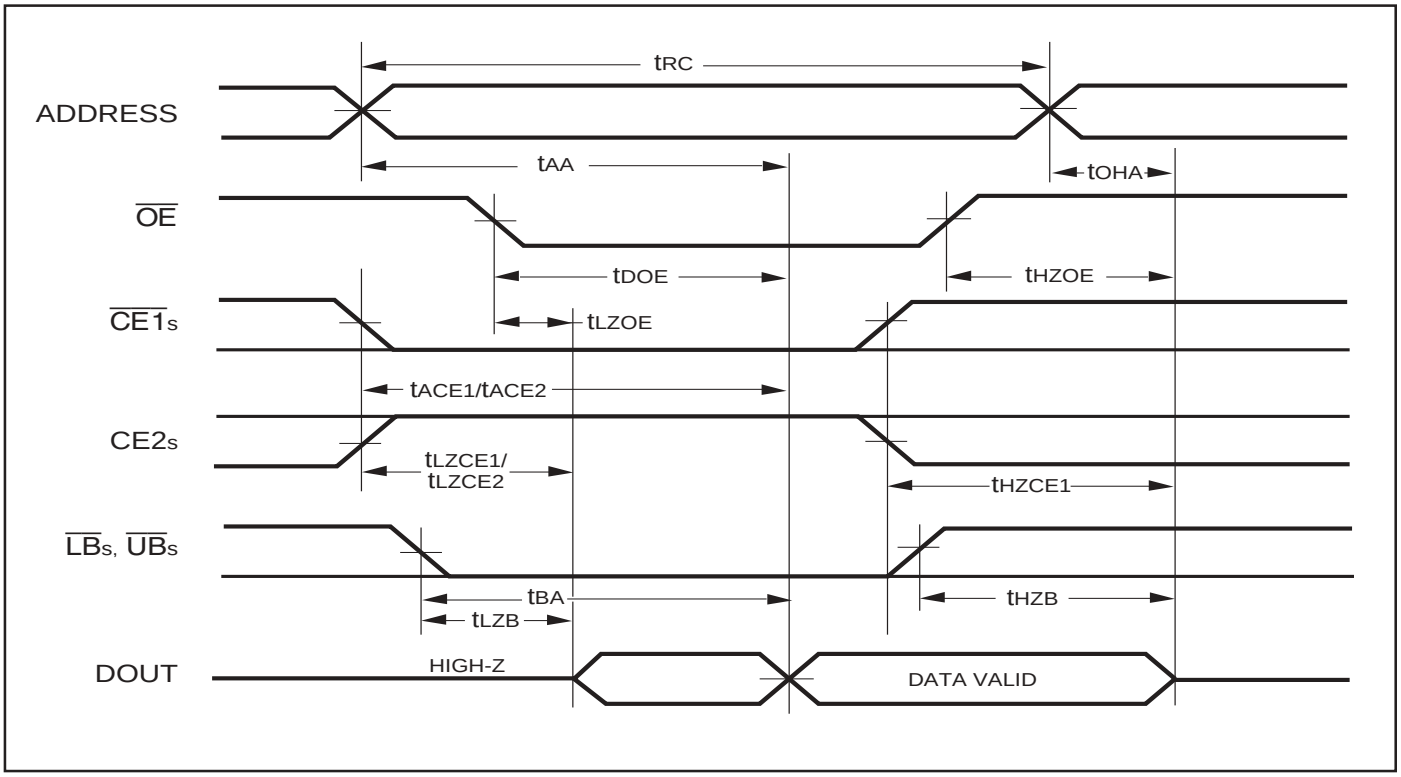
AC WAVEFORMS

SRAM READ CYCLE NO. 1[1,2] (Address Controlled) ($\overline{CE1}_s$ = $\overline{OE}$ = V_{IL}, $\overline{UB}_s$ or $\overline{LB}_s$ = V_{IL})



AC WAVEFORMS

SRAM READ CYCLE NO. 2[1,3] ($\overline{CE1}_s$, $\overline{OE}$, AND $\overline{UB}_s$/ $\overline{LB}_s$ Controlled)



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE1}$, $\overline{UB}_s$, or $\overline{LB}_s$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE1}$ LOW transition.

WRITE CYCLE SWITCHING CHARACTERISTICS[1]

(Over Operating Range)

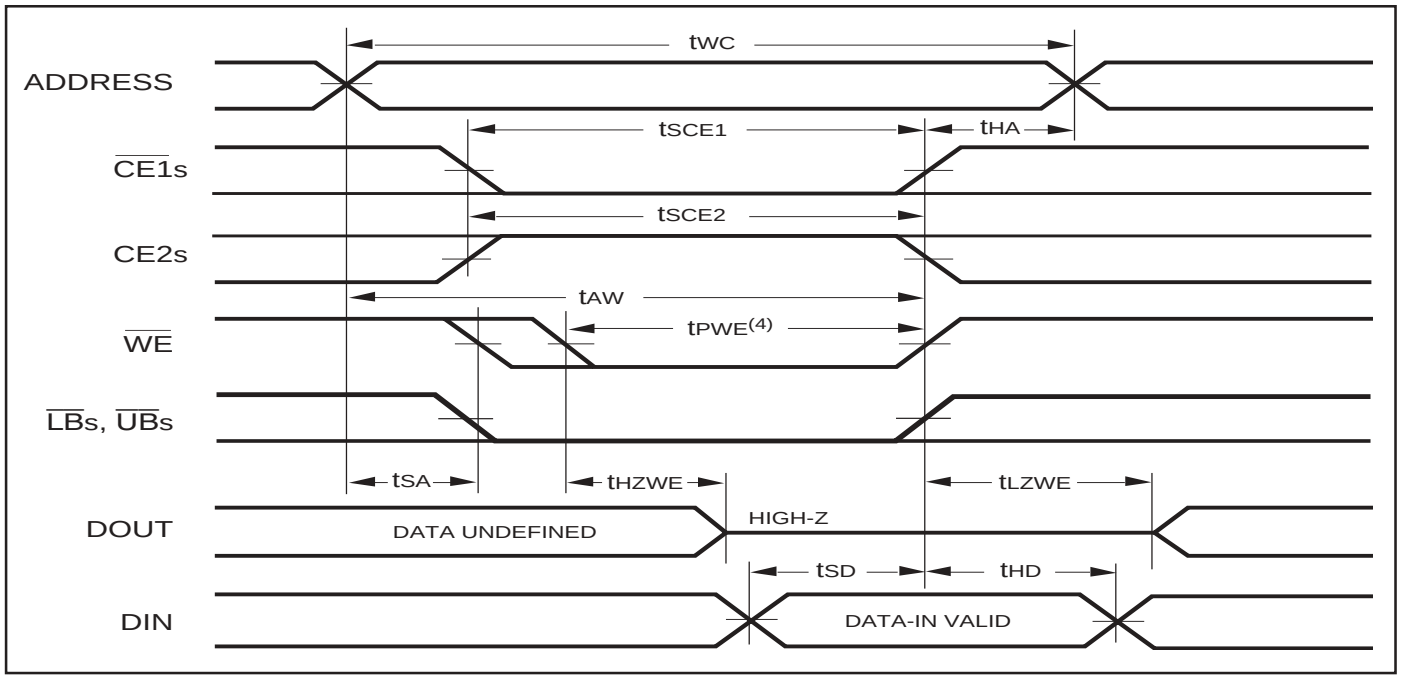
Symbol	Parameter	70ns Min.	70ns Max.	Unit
t_{WC}	Write Cycle Time	70	—	ns
t_{SCE1}	$\overline{CE1}_s$ to Write End	55	—	ns
t_{AW}	Address Setup Time to Write End	55	—	ns
t_{HA}	Address Hold from Write End	0	—	ns
t_{SA}	Address Setup Time	0	—	ns
t_{PWB}	$\overline{LB}_s$,$\overline{UB}_s$ Valid to End of Write	55	—	ns
t_{PWE}	$\overline{WE}$ Pulse Width	50	—	ns
t_{SD}	Data Setup to Write End	30	—	ns
t_{HD}	Data Hold from Write End	0	—	ns
t_{HZWE}[2]	$\overline{WE}$ LOW to High-Z Output	—	25	ns
t_{LZWE}[2]	$\overline{WE}$ HIGH to Low-Z Output	0	—	ns

Notes:
1. See SRAM AC Test Conditions.
2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

AC WAVEFORMS

SRAM WRITE CYCLE NO. 1[1,2]

($\overline{CE1}_s$ Controlled, $\overline{OE}$ = HIGH or LOW)

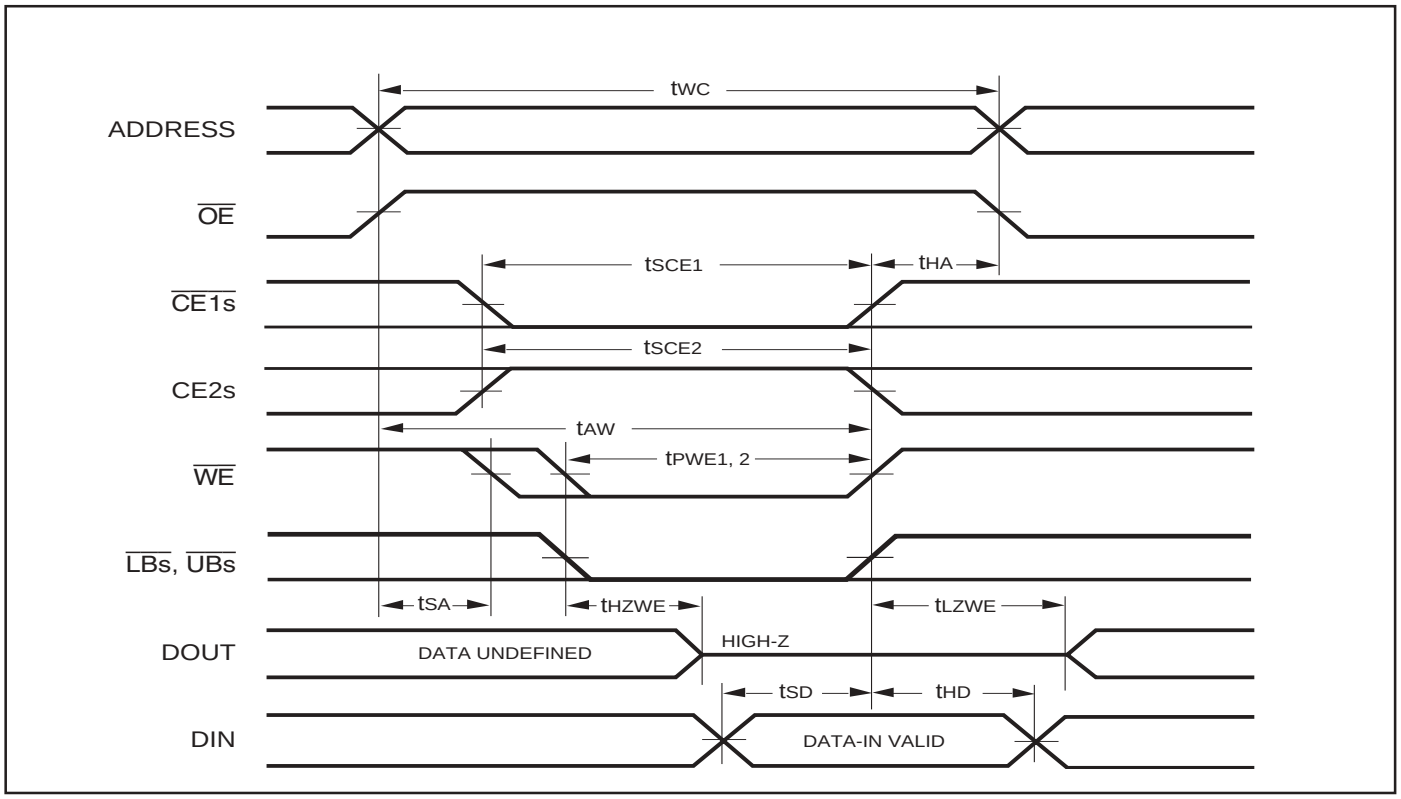


Notes:

1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the $\overline{CE1}_s$ and $\overline{WE}$ inputs and at least one of the $\overline{LB}_s$ and $\overline{UB}_s$ inputs being in the LOW state.
2. WRITE = ($\overline{CE1}_s$) [($\overline{LB}_s$) = ($\overline{UB}_s$)] ($\overline{WE}$).

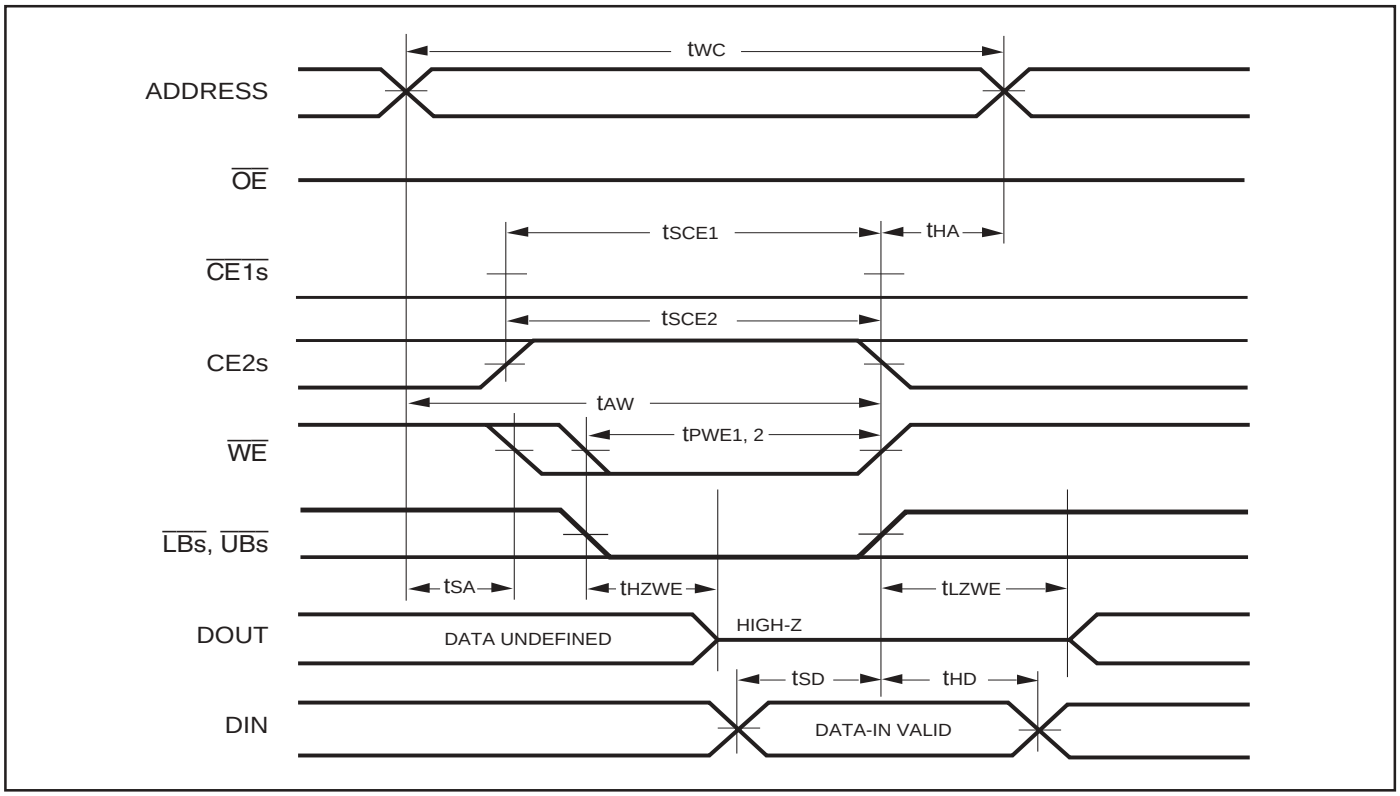
SRAM WRITE CYCLE NO. 2

($\overline{WE}$ Controlled: $\overline{OE}$ is HIGH During Write Cycle)



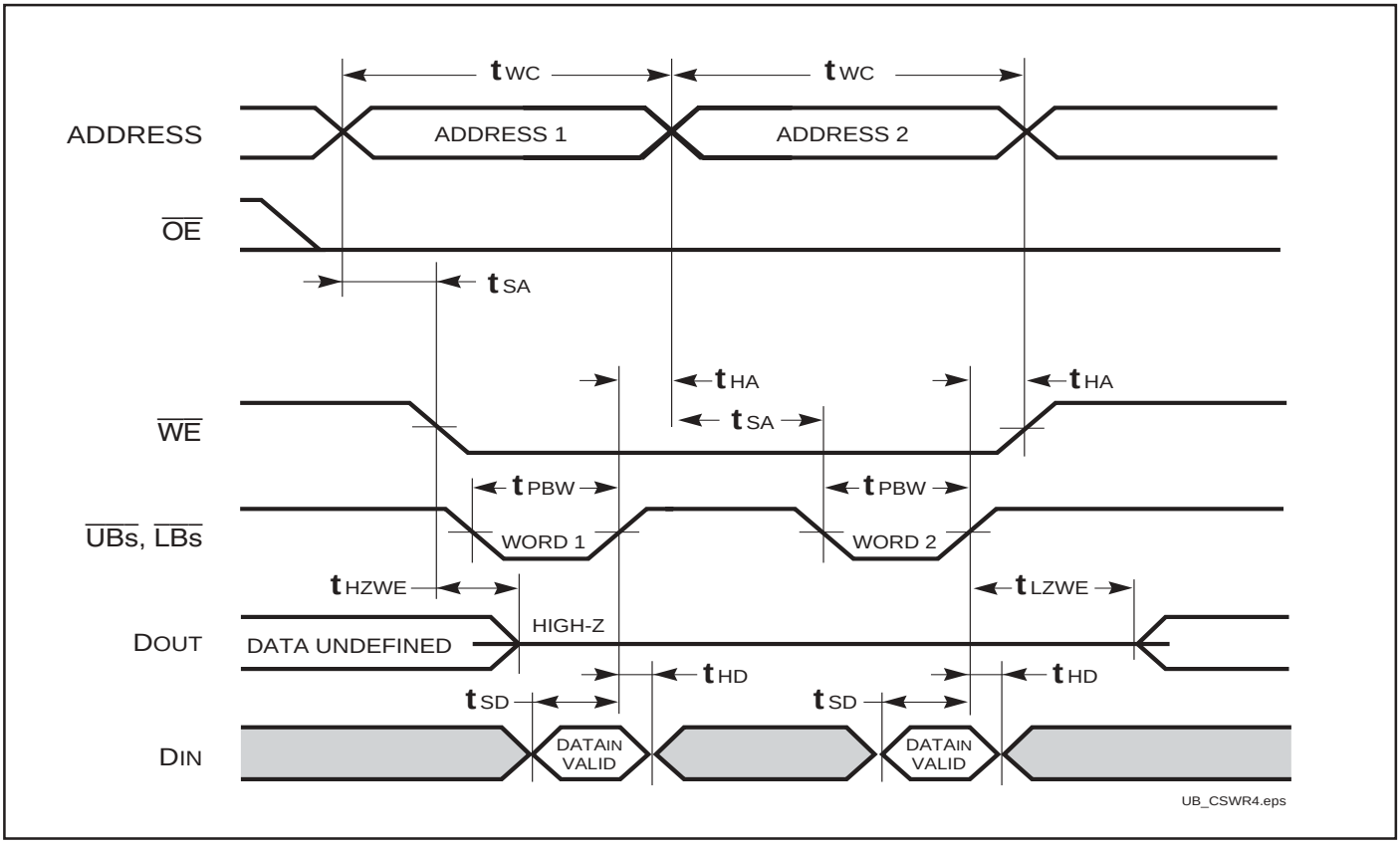
SRAM WRITE CYCLE NO. 3

($\overline{WE}$ Controlled: $\overline{OE}$ is LOW During Write Cycle)



WRITE CYCLE NO. 4

($\overline{UB}_s$/$\overline{LB}_s$ Controlled, $\overline{CE1}$s is LOW, CE2s is HIGH)

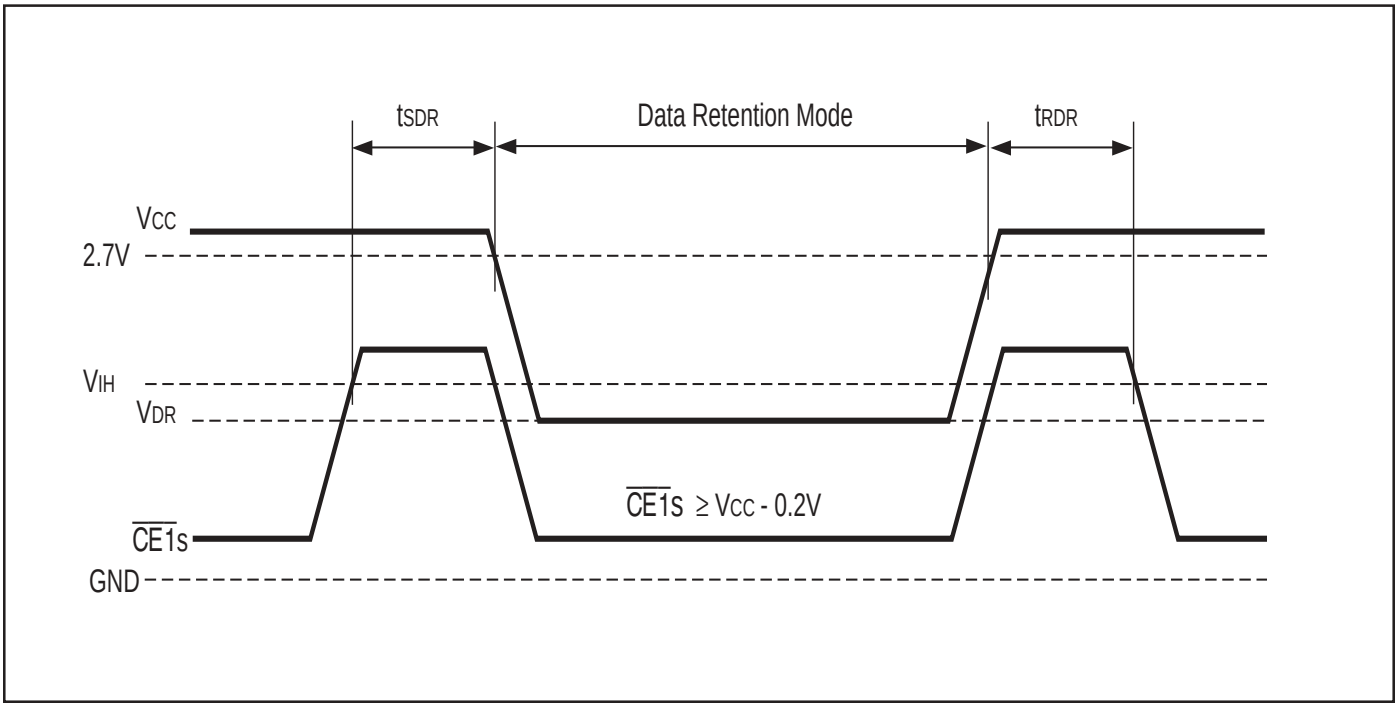


SRAM DATA RETENTION SWITCHING CHARACTERISTICS

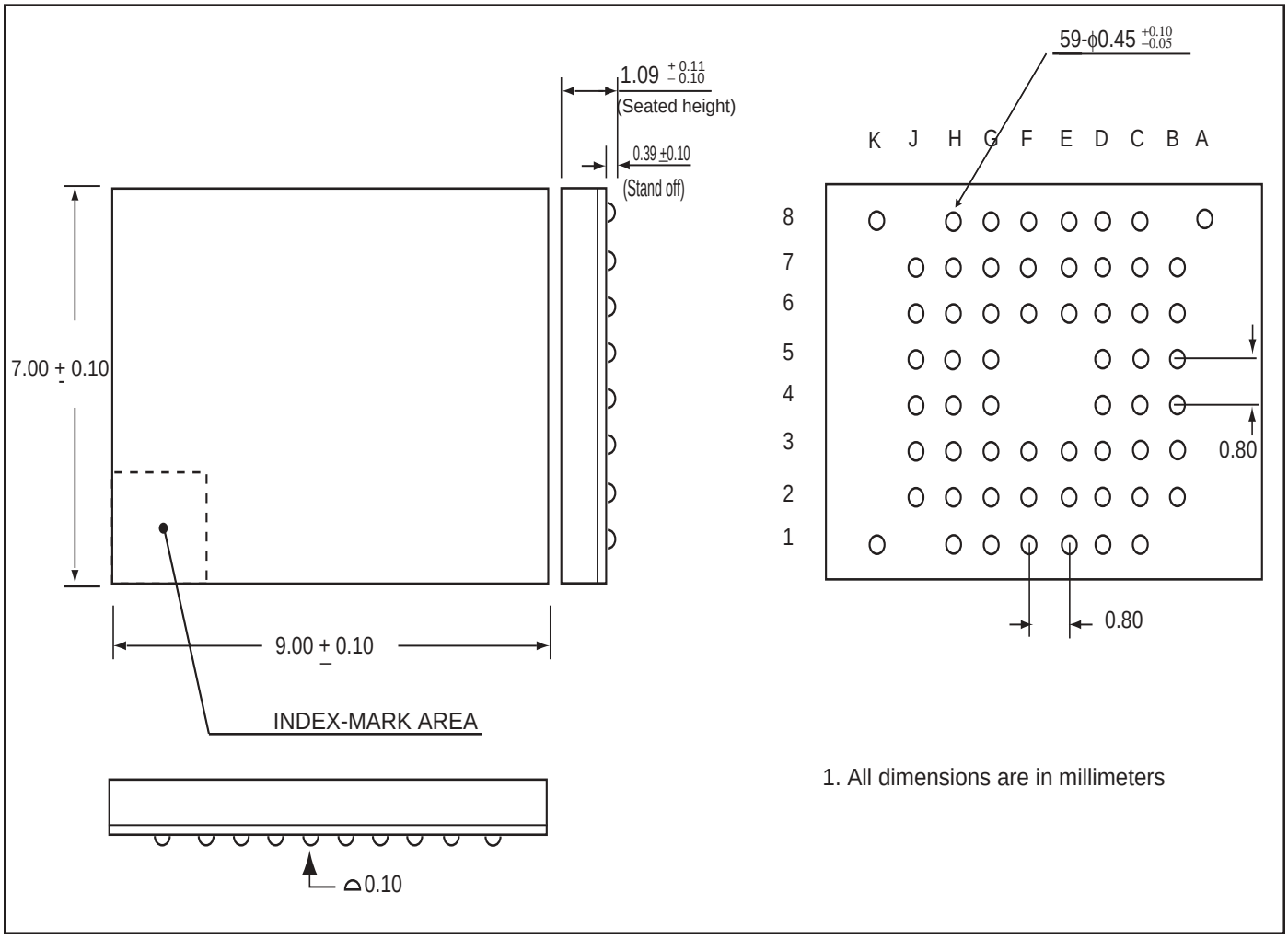
Symbol	Parameter	Test Condition	Min.	Max.	Unit
V_{DR}	Vcc for Data Retention	See Data Retention Waveform	1.5	3.3	V
I_{DR}	Data Retention Current	Vcc = 3.0V, $\overline{CS1} \geq$ Vcc – 0.2V	—	10	µA
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform	0	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform	t_{RC}	—	ns

SRAM DATA RETENTION WAVEFORM

($\overline{CE1}$ Controlled)



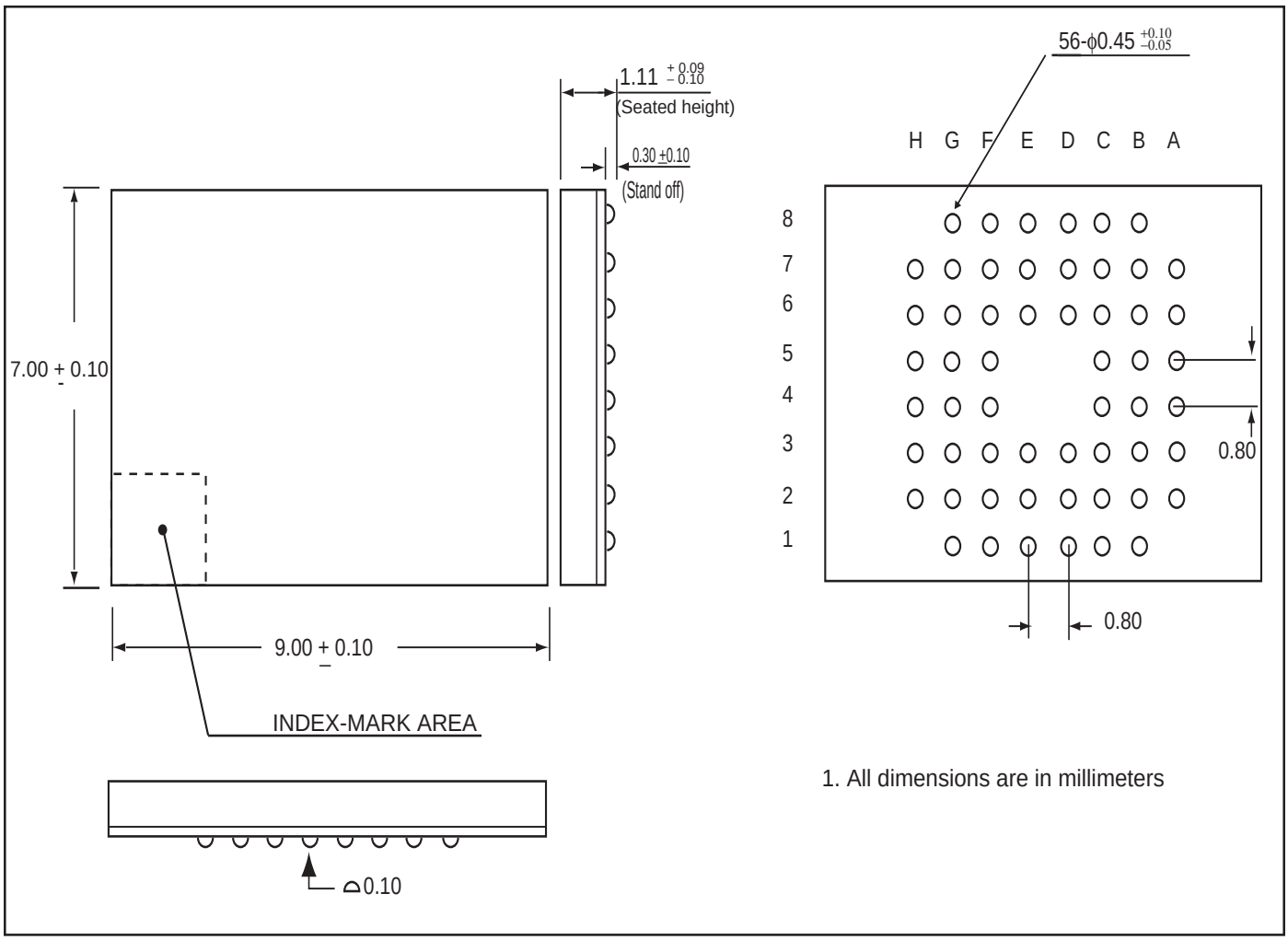
MINI BALL GRID ARRAY – 59-Ball BGA
PACKAGE CODE:B 9.00 mm x 7.00 mm Body, 0.8 mm Ball Pitch



1. All dimensions are in millimeters

MINI BALL GRID ARRAY – 56-Ball BGA

PACKAGE CODE:M 9.00 mm x 7.00 mm Body, 0.8 mm Ball Pitch



1. All dimensions are in millimeters

ORDERING INFORMATION

Industrial Range: -30°C to +85°C

Part No.	SRAM Data Bus	Boot Section	Flash Bank Organization	Flash Speed(ns)	SRAM Speed(ns)	Order Package
IS71V16F32GSB04-7070BI	16	Bottom	User Configurable	70	70	59-ball BGA
IS71V16F32GST04-7070BI	16	Top	User Configurable	70	70	59-ball BGA
IS71V16F32GSB04-7070MI	16	Bottom	User Configurable	70	70	56-ball BGA
IS71V16F32GST04-7070MI	16	Top	User Configurable	70	70	56-ball BGA