
DDR FEMMA SODIMM MODULE

512 MByte (64M x 64 / 72)

1GByte (128M x 64 / 72)

Unbuffered 200 Pin - PC1600/2100 DDR SODIMM

General Description:

This memory module is a high density Unbuffered DDR synchronous dynamic RAM module organized as x64 or x72 in a 200-pin Small Outline Dual In-Line Memory Module (SODIMM) package. The module utilizes eighteen (18) X8 DDR SDRAM devices in a TSOP II 400 mil package. A zero delay buffer drives the input clock to all DDR SDRAM devices. A 256 Byte Serial EEPROM contains the module configuration information. The EEPROM can be configured to a customer's specifications.

These modules utilize a double data rate architecture to achieve high speed operation, offering substantial advances in operating performance, including the ability to synchronously burst data at a high rate with automatic column-address generation, interleave between internal banks in order to hide precharge time, and the capability to randomly change column address on each clock cycle during burst.

Features:

- ◆ High density: 512 MB (64M x 64) or 512MB (64Mx72 - ECC)
1024 MB (128M x 64) or 1024MB (128Mx72 - ECC)
- ◆ Cycle time: 10 ns (100 MHz)
7.5 ns (133 MHz)
- ◆ Double-data-rate architecture; two data transfers per clock cycle
- ◆ Fast data transfer rates PC1600 or PC2100
- ◆ JEDEC Standard 200 Pin Unbuffered DDR SODIMM Pinout
- ◆ Utilizes 200 Mb/s and 266 Mb/s DDR SDRAM components
- ◆ Single power supply of 2.5V \pm 0.2V
- ◆ 2.5V I/O (SSTL_2 compatible)
- ◆ Bi-directional data strobe (DQS) transmitted/received with data
- ◆ Unbuffered Control and Address Lines
- ◆ On-board PLL Clock Driver (2 msec settling time)
- ◆ 8K Refresh in 64ms (7.8 usec per row)
- ◆ Auto Precharge and Auto Refresh Modes handled by SDRAM Devices
- ◆ Programmable Burst Type, Burst Length and CAS Latency of SDRAM Devices
- ◆ Serial Presence Detect with EEPROM
- ◆ Package Height: 1.25 inches (+/- 10mils)
- ◆ Patented

Absolute Maximum Ratings*:

Item	Symbol	Rating	Unit
Supply voltage (V_{DD} Relative to V_{SS})	V_{DD}	-1V to 3.6V	V
Supply voltage	V_{DDQ}	-1V to 3.6V	V
I/O voltage relative to V_{SS}	$V_{I/O}$	$V_{DDQ} \pm 0.5V$	
Operating temperature	T_{opr}	0 – 70	°C
Storage temperature	T_{stg}	-55 – 150	°C
Short circuit output current	I_{out}	50	mA

* Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions:

(Voltage referenced to V_{DD} . $T_A = 0$ to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	2.3	2.5	2.7	V
I/O Supply Voltage	V_{DDQ}	2.3		2.7	V
Input high voltage	V_{IH}	$V_{REF} + 0.18$		$V_{dd} + 0.3$	V
Input low voltage	V_{IL}	-0.3		$V_{REF} - 0.18$	V

Capacitance:

($T_A = 25^\circ\text{C}$, $V_{DD} = 2.5V \pm 0.2V$)

Parameter	Symbol	Max.	Unit
Input capacitance (/CS0~/CS1)	C_{IN}	32	pF
Input capacitance (/DQMBs)	C_{IN}	6.4	pF
Input capacitance (CK0)	C_{IN}	4	pF
Input capacitance (/RAS, /CAS, /WE, A0-A12)	C_{IN}	64	pF
Input/Output capacitance (DQ0~DQ63, CB0~CB7, DQS0~DQS8)	$C_{I/O}$	11	pF

Pin Names:

A0-A9, A11-A12	Address input	/WE	Write enable
A10/AP	Address input/Auto precharge	DM0-DM8	Data – in mask
BA0-BA1	Bank select	VDD	Power supply
DQ0-DQ63	Data input/output	VSS	Ground
DQS0-DQS8	Data strobe input/output	VREF	Power supply for reference
CB0-CB7	Data check bits	VDDSPD	EEPROM power supply
CK2,/CK2	Clock input	SDA	Serial data I/O
CKE0-CKE1	Clock enable input	SCL	Serial clock
/S0-/S1	Chip select input	SA0-2	Address in EEPROM
/RAS	Row address strobe	VDDID	VDD ID flag
/CAS	Column address strobe	DU	Reserved

Pinout:

No.	Designation	No.	Designation	No.	Designation	No.	Designation	No.	Designation
1	VREF	41	DQ16	81	VDD	121	/S0	161	Vss
2	VREF	42	DQ20	82	VDD	122	/S1	162	VSS
3	VSS	43	DQ17	83	CB3	123	DU	163	DQ48
4	VSS	44	DQ21	84	CB7	124	DU	164	DQ52
5	DQ0	45	VDD	85	DU	125	VSS	165	DQ49
6	DQ4	46	VDD	86	DU	126	VSS	166	DQ53
7	DQ1	47	DQS2	87	VSS	127	DQ32	167	VDD
8	DQ5	48	DM2	88	VSS	128	DQ36	168	VDD
9	VDD	49	DQ18	89	CK2	129	DQ33	169	DQS6
10	VDD	50	DQ22	90	VSS	130	DQ37	170	DM6
11	DQS0	51	VSS	91	/CK2	131	VDD	171	DQ50
12	DM0	52	VSS	92	VDD	132	VDD	172	DQ54
13	DQ2	53	DQ19	93	VDD	133	DQS4	173	Vss
14	DQ6	54	DQ23	94	VDD	134	DM4	174	VSS
15	VSS	55	DQ24	95	CKE1	135	DQ34	175	DQ51
16	VSS	56	DQ28	96	CKE0	136	DQ38	176	DQ55
17	DQ3	57	VDD	97	DU/A13	137	VSS	177	DQ56
18	DQ7	58	VDD	98	DU/BA2	138	VSS	178	DQ60
19	DQ8	59	DQ25	99	A12	139	DQ35	179	VDD
20	DQ12	60	DQ29	100	A11	140	DQ39	180	VDD
21	VDD	61	DQS3	101	A9	141	DQ40	181	DQ57
22	VDD	62	DM3	102	A8	142	DQ44	182	DQ61
23	DQ9	63	VSS	103	VSS	143	VDD	183	DQS7
24	DQ13	64	VSS	104	VSS	144	VDD	184	DM7
25	DQS1	65	DQ26	105	A7	145	DQ41	185	VSS
26	DM1	66	DQ30	106	A6	146	DQ45	186	VSS
27	VSS	67	DQ27	107	A5	147	DQS5	187	DQ58
28	VSS	68	DQ31	108	A4	148	DM5	188	DQ62
29	DQ10	69	VDD	109	A3	149	VSS	189	DQ59
30	DQ14	70	VDD	110	A2	150	VSS	190	DQ63
31	DQ11	71	CB0	111	A1	151	DQ42	191	VDD
32	DQ15	72	CB4	112	A0	152	DQ46	192	VDD
33	VDD	73	CB1	113	VDD	153	DQ43	193	SDA
34	VDD	74	CB5	114	VDD	154	DQ47	194	SA0
35	CK0 (NC)	75	VSS	115	A10/AP	155	VDD	195	SCL
36	VDD	76	VSS	116	BA1	156	VDD	196	SA1
37	/CK0 (NC)	77	DQS8	117	BA0	157	VDD	197	VDDSPD
38	VSS	78	DM8	118	/RAS	158	/CK1 (NC)	198	SA2
39	VSS	79	CB2	119	/WE	159	VSS	199	VDDID
40	VSS	80	CB6	120	/CAS	160	CK1 (NC)	200	DU

DC Characteristics:

($V_{DD} = 2.5V \pm 0.2V$, $V_{SS}=0V$, $T_A=0$ to $+70^{\circ}C$)

Parameter ¹	Symbol	PC2100 Max.	PC1600 Max.	Unit
Operating current (No Burst, $T_{CK}=\min.$ $T_{RC}=\min.$)	I_{DD1}	1965	1865	mA
Precharge Standby Current ($CKE=V_{IL}$, $T_{CK} = \min.$ Bank idle) ($CKE=V_{IH}$, $T_{CK} = \min.$ Bank idle)	I_{DD2}	200 550	200 550	mA
Active Standby Current ($CKE=V_{IL}$, $T_{CK} = \min.$) ($CKE=V_{IH}$, $T_{CK} = \min.$)	I_{DD3}	370 820	320 730	mA
Burst Mode Current ($t_{CK}=\min.$)	I_{DD4}	2300	1700	mA
Refresh Current (DIMM both banks) ($t_{CK}=\min.$, $t_{RC}=\min.$, $t_{RRD}=\min.$, Auto Refresh)	I_{DD5}	5200	4800	mA
Self Refresh Current ($CKE=V_{IL}$)	I_{DD6}	208	208	mA

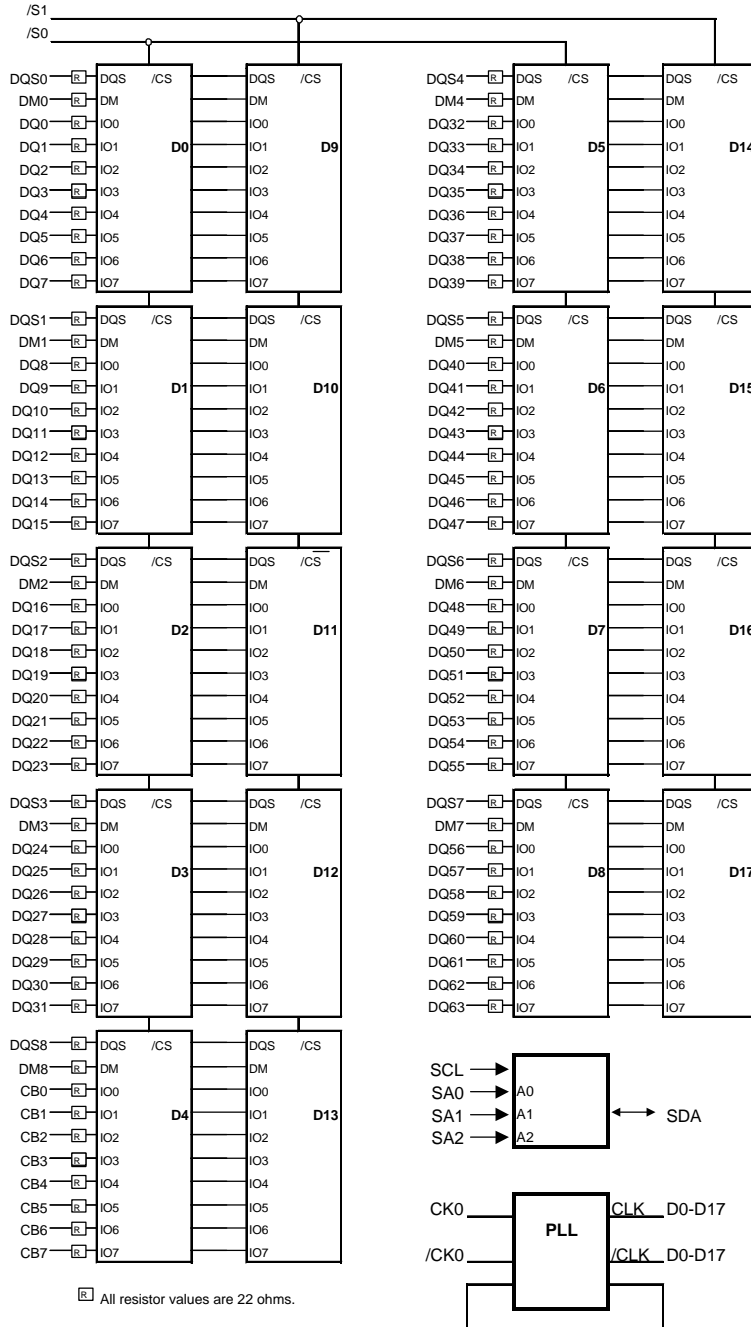
AC Electrical Characteristics:

($V_{DD} = 2.5V \pm 0.2V$, $V_{SS}=0V$, $T_A=0$ to $+70^{\circ}C$)

Parameter	Symbol	PC2100 Min.	PC2100 Max.	PC1600 Min.	PC1600 Max.	Unit
Row to row active delay	t_{RRD}	15		15		ns
RAS to CAS delay	t_{RCD}	20		20		ns
Row precharge time	t_{RP}	20		20		ns
Row active time	t_{RAS}	40	120K	40	120K	ns
Row cycle time	t_{RC}	65		65		ns
Number of valid output data		3		3		Ea
Clock Cycle Time	t_{CK}	7.5		10		ns
Clock to Valid Output Delay	T_{AC}	-0.75	+0.75	-0.8	+0.8	ns
Clock High Pulse Width	t_{CH}	0.45	0.55	0.45	0.55	ns
Clock Low Pulse Width	t_{CL}	0.45	0.55	0.45	0.55	ns
Input Setup Time	T_{IS}	1		1		ns
Input Hold Time	T_{IH}	0.9		0.9		ns

¹ Module Idd calculated based upon Mitsubishi 512Mb component Idd.

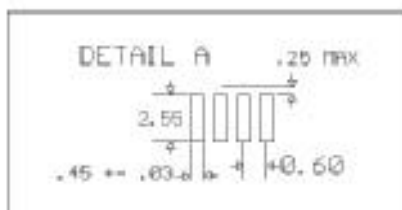
Functional Block Diagram:



Architectural drawing of the front side of a building facade. The drawing shows a symmetrical design with a central entrance area and side wings. Key dimensions include a total width of 67.60, a central width of 47.40, and various heights and radii (R = 2.00). A circular feature is labeled "DETAIL A". The drawing is oriented with "FRONT SIDE" at the top.



DDR SODIMM DIMENSIONS
ALL DIMENSIONS ARE IN mm



Part Numbers:
512MB DDR FEMMA SODIMM

 KT6464D8FN^sUA-xxCⁿⁿ
Part Number Decoder:

s = Clock		xx = DRAM		nn = CAS Latency	
3 =	133MHz	14 =	Samsung	20 =	2
0 =	100MHz	04 =	Elpida	25 =	2.5
		06 =	Hynix		
		07 =	Micron		
		08 =	Mitsubishi		
		15 =	Infineon		
		17 =	Nanya		
		00 =	Non-specific		

512MB DDR FEMMA ECC SODIMM

 KT6472D8FN^sUA-xxCⁿⁿ
Part Number Decoder:

s = Clock		xx = DRAM		nn = CAS Latency	
3 =	133MHz	14 =	Samsung	20 =	2
0 =	100MHz	04 =	Elpida	25 =	2.5
		06 =	Hynix		
		07 =	Micron		
		08 =	Mitsubishi		
		15 =	Infineon		
		17 =	Nanya		
		00 =	Non-specific		

1GB DDR FEMMA SODIMM
KT12864D8FN*sUA-xxCnn*
Part Number Decoder:

s = Clock		xx = DRAM		nn = CAS Latency	
3 =	133MHz	14 =	Samsung	20 =	2
0 =	100MHz	04 =	Elpida	25 =	2.5
		06 =	Hynix		
		07 =	Micron		
		08 =	Mitsubishi		
		15 =	Infineon		
		17 =	Nanya		
		00 =	Non-specific		

1GB DDR FEMMA ECC SODIMM
KT12872D8FN*sUA-xxCnn*
Part Number Decoder:

s = Clock		xx = DRAM		nn = CAS Latency	
3 =	133MHz	14 =	Samsung	20 =	2
0 =	100MHz	04 =	Elpida	25 =	2.5
		06 =	Hynix		
		07 =	Micron		
		08 =	Mitsubishi		
		15 =	Infineon		
		17 =	Nanya		
		00 =	Non-specific		

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For further information on this product, please contact:
Kentron Technologies, Inc.
155 West Street
Wilmington, MA 01887
Phone: 978/988-9100
Fax 978/988-5550
<http://www.kentrontech.com>