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1. General Description

HE83755 is a member of 8-bit Micro-controller series developed by King Billion Electronics Ltd. Users can choose any one of combination among【2048 dots LCD Driver + 16 Bit I/O Port】…【1792 dots LCD Driver + 24 Bit I/O Port】etc. which is determined by mask options. The built-in OP comparator can be used with light, voice, temperature and humility sensor or used to detect the battery low. The 7-bit current-type D/A converter and PWM drive output provide the complete speech output mechanism. The built-in DTMF generator can generate the PSTN dialing tone directly. The 512K bytes ROM size can be used in the storage of large speech data, image and text etc. It can be applicable to the medium systems such as small-scale dictionary, data bank, pocket dialer, automatic dialer machine, medium level educational toy, lower second voice recording system or used with external command mode SRAM or Flash RAM for higher second voice recording etc.

The instruction sets of HE80000 series are quite easy to learn and simple to use. Only about thirty instructions with four-type addressing mode are provided. Most of instructions take only 3 oscillator clocks (machine cycles). The performance of HE83755 is enough for most of battery operation system.

2. Features

- Operation Voltage： 2.4V – 5.5V
- System Clock： DC ~ 8MHz @ 5.0V
  DC ~ 4MHz @ 2.4V
- Clock Source: Internal/External Fast clock, Internal/External slow clock
- Dual Clock System： Normal (Fast) clock 32.768KHz ~ 8MHz
  Slow clock 32.768 KHz
- Operation Mode： DUAL、FAST、SLOW、IDLE、SLEEP Mode.
- Internal ROM: 512K Bytes (64K Program ROM, 448K Data ROM)
- Internal RAM: 4K Bytes.
- Watch dog timer (WDT) to prevent deadlock condition.
- 16~24 Bi-directional I/O ports.
- 2048~1792 dots LCD driver with built-in regulator for LCD display.
- LCD COM X SEG : 32 X 64
- LCD Bias : 1/7
- LCD Charge Pump: 3/2, 2, and 3 times of VDD
- One 7-bits current-type DAC output.
- One built-in OP comparator.
- PWM device.
- Built-in DTMF Generator.
- Recording function
- Speech recognition function
- Two external interrupts and three internal timer interrupts.

3. Pin Description

122 121	**FXI,** **FXO**	B, O	External fast clock input/output pins are used to connect crystal or RC to generate the 32.768KHz ~ 8MHz system clock.	Mask option setting： MO_FCK/SCKN= 00：Slow Clock only 01：Illegal 10：Dual Clock 11：Fast Clock only MO_FOSCE = 0：Internal fast osc. = 1：External fast osc. MO_FXTAL = 0：RC osc. for fast clock = 1：X'tal osc. for fast clock MO_SXTAL = 0：RC for 32768 Hz clock = 1：X'tal for 32768 Hz clock Use OP1 and OP2 to switch among different operation mode (NORMAL, SLOW, IDEL and SLEEP). In Dual Clock mode, the main system clock is still the Fast Clock. The 32768 Hz clock is for LCD and Timer 1 only.
125 124	**SXI,** **SXO**	I, O	External slow clock input/output pins used to connect the 32.768KHz crystal to generate slow clock for system operation (slow mode), LCD display or timer 1 clock source.	
120	**RSTP_N**	I	System Reset.	Level trigger, active low. Except for using this pin, using mask option (MO_PORE=1) could enable IC build-in Power-on reset circuit. Besides, MO_WDTE can set Watch Dog Timer： MO_WDTE=0：Disable Watch Dog Timer =1：Enable Watch Dog Timer
123	**TSTP_P**	I	Test Pin	Please bond this pin and add a test point on PCB for debugging. Leave this pin floating is OK.
139.. 142 1..4	**PRTC[7:0]**	B	8-pin bi-directional I/O port.	Mask options： MO_CPP[7..0] = 1 ~ Push-pull. = 0 ~ Open-drain. I/O shall be set to output "1" state before reading, whenever use them as input (No tri-state structure).
131.. 138	**PRTD[7:0]**	B	8-pin bi-directional I/O port. PRTD[7..2] as wake-up pin. PRTD[7..6] as external interrupt pin.	Mask options： MO_DPP[7..0] = 1 ~ Push-pull. = 0 ~ Open-drain. I/O shall be set to output "1" state before reading, whenever use them as input (No tri-state structure).
23..30	**PRT14[7:0]/** **SEG[63:56]**	B/ O	8-pin bi-directional I/O port that is shared with LCD segment pin.	Mask options： MO_LIO14[7..0] = 1 ~ LCD Pin. = 0 ~ I/O Pin. MO_14PP[7..0] = 1 ~ Push-pull. = 0 ~ Open-drain. I/O shall be set to output "1" state before reading, whenever use them as input (No tri-state structure).
22..7 87..102	**COM[31:0]**	O	LCD common Output	LCD Data filled from "**Page1,** 00H", please refer the LCD RAM map.
31..86	**SEG[55:0]**	O	LCD segment Output	
104	**LC2**	B	Charge Pump Switch 1	Add one 0.1 μF capacitor between LC1 and LC2.

103	**LC1**	B	Charge Pump Switch 2	Please refer the application circuit.
107	**L V3**	B	Charge Pump V3	LV3< 9 Volts. Please refer the application circuit.
106	**L V2**	B	Charge Pump V2	
105	**L V1**	B	Charge Pump V1	
108..112	**LR[4..0]**	B	LCD Resister level 4 ~ 1	Please refer the application circuit.
113	**L VG**	I	LCD Virtual Ground	Please refer the application circuit.
5	**PWMP**	O	The PWM positive output can drive speaker or buzzer directly.	Set the bit2 of VOC register as one to turn on PWM.
6	**PWMN**	O	The PWM positive output can drive speaker or buzzer directly.	Set the bit2 of VOC register as one to turn on PWM.
115	**VO**	O	D/A output.	Bit 1 of VOC = '1' , Turn on DA
116	**DAO**	O	DAC Voice Output	Set the bit1 (DA=1) of VOC register to turn on DAC with VO output.
117	**OPIN**	I	OPAMP negative input pin.	Built-in OP comparator. Set Bit 0 of VOC = '1' , Turn on OP
118	**OPIP**	I	OPAMP positive input pin.	
119	**OPO**	O	OPAMP output pin.	
128	**DTMFO**	O	DTMF Output	Through PRT12 we can turn on/off DTMF and write data. Using Mask Option MO_DTMFSCK set the clock source of DTMF block. MO_DTMFSCK=0 →Clock Source=3.579545MHz =1 → Clock Source=32768 Hz
127	**MUTE**	O	MUTE Output for Dialer	User can turn on/off MUTE pin by port12.
129	**SDO**	O	Serial Data Output	We can turn on/off SDO block or write data by port12.
130	**KEYTONE**	O	1024-Hz 50% duty square wave	User can turn on/off key tone by port12.
126	**VDD**	P	Positive Power Input	Add a 0.1 µF capacitor as by-pass capacitor between VDD and GND.
114	**GND**	P	Power Ground Input	

I: Input, O: Output, B: Bidirectional, P: Power.

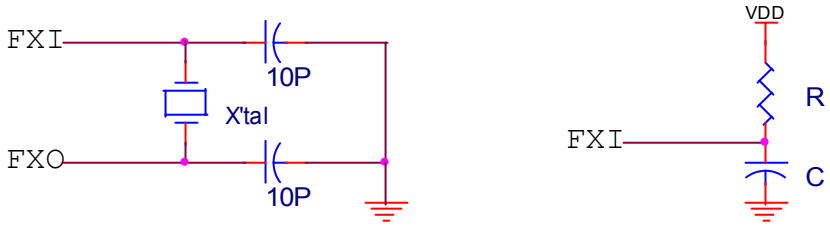
4. LCD Display RAM Map

Page 1	SEG [7:0]	SEG [15:8]	SEG [23:16]	SEG [31:24]	SEG [39:32]	SEG [47:40]	SEG [55:48]	SEG [63:56]
COM0	00H	20H	40H	60H	80H	A0H	C0H	E0H
COM1	01H	21H	41H	61H	81H	A1H	C1H	E1H
COM2	02H	22H	42H	62H	82H	A2H	C2H	E2H
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
COM29	1DH	3DH	5DH	7DH	9DH	BDH	DDH	FDH
COM32	1EH	3EH	5EH	7EH	9EH	BEH	DEH	FEH
COM31	1FH	3FH	5FH	7FH	9FH	BFH	DFH	FFH

5. Oscillators

The MCU is equipped with two clock sources with a variety of selections on the types of oscillators to choose from. System designer can select oscillator types based on the cost target, timing accuracy requirements etc. Crystal, Resonator or the RC oscillator can be used as fast clock source, components should be placed as close to the pins as possible. The type of oscillator used is selected by mask option MO_FXTAL.

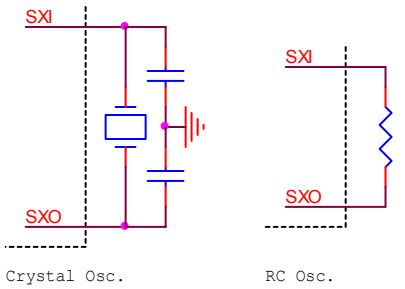
FXI (Bi-direction), FXO (Output)



Mask Option	Description
MO_FXTAL	0: RC Oscillator. 1: Crystal Oscillator.
MO_FCK	0: Fast clock disable 1: Fast clock enable

SXI (Bi-direction), SXO (Output)

Two types of oscillator, crystal and RC, can be used as slow clock selectable by mask option MO_SXTAL. If used time keeping function or other applications that required the accurate timing, crystal oscillator is recommended. If the timing accuracy is not important, then RC type oscillator can be used to save cost.



Mask Option	Description
MO_SXTAL	0: RC Oscillator. 1: Crystal Oscillator.
MO_SCKN	0: Slow clock enable 1: Slow clock disable

With two clock sources available, the system can switch among operation modes of Normal, Slow, Idle,

and Sleep modes by the setting of OP1 and OP2 registers as shown in tables below to suit the needs of application such as power saving, etc.

OP1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	DRDY	STOP	SLOW	INTE	T2E	T1E	Z	C
Mode	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	-	-

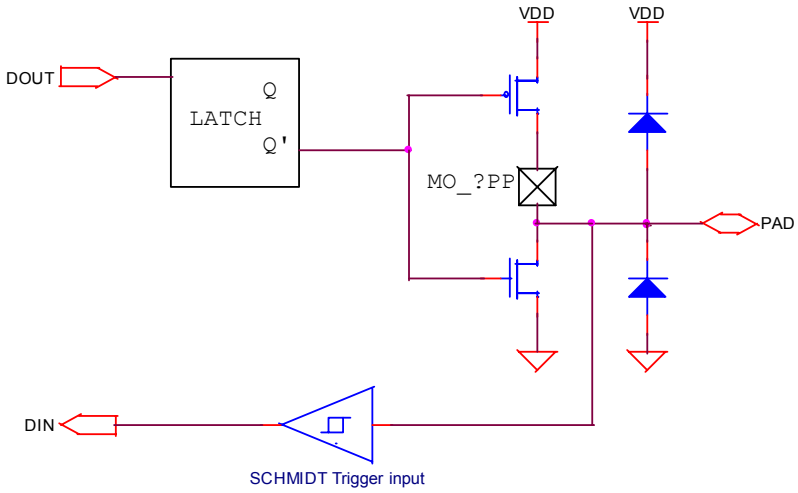
OP2	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	IDLE	PNWK	TCWK	TBE	TBS[3:0]			
Mode	R/W	R	R	R/W	W	W	W	W
Reset	0	x	x	0	x	x	x	x

6. General Purpose I/O

There are two dedicated general purpose I/O port, PRTC and PRTD, while PRT14[7:0] are multiplexed with LCD segment driver pins. All the I/O Ports are bi-directional and of non- tri-state output structure. The output has weak sourcing (50 μA) and stronger sinking (1 mA) capability and each can be configured as push-pull or open-drain output structure individually by mask option.

When the I/O port is used as input, the weakly high sourcing can be used as weakly pull-up. Open drain can be used if the pull-up is not required and let the external driver to drive the pin. Please note that a floating pad could cause more power consumption since the noise could interfere with the circuit and cause the input to toggle. A '1' needs to be written to port first before reading the input data from the I/O pin. If the PMOS is used as pull-up, care should be taken to avoid the constant power drain by DC path between pull-up and external circuit.

The input port has built-in Schmidt trigger to prevent it from chattering. The hysteresis level of Schmidt trigger is 1/3 VDD.



As pads of PRT14 are shared with LCD segment driver, the function of the pad is determined by mask options. Following table is the setting for MO_LIO14[...] and MO_14PP[...] and others related to LCD display setting and pin assignment features.

MO_LIO14[…]	MO_14PP[...]	I/O Port	LCD Pin
0	0	Open-drain output	--
0	1	Push-pull output	--
1	0	--	xx
1	1	--	LCD Display

--: Function not available.

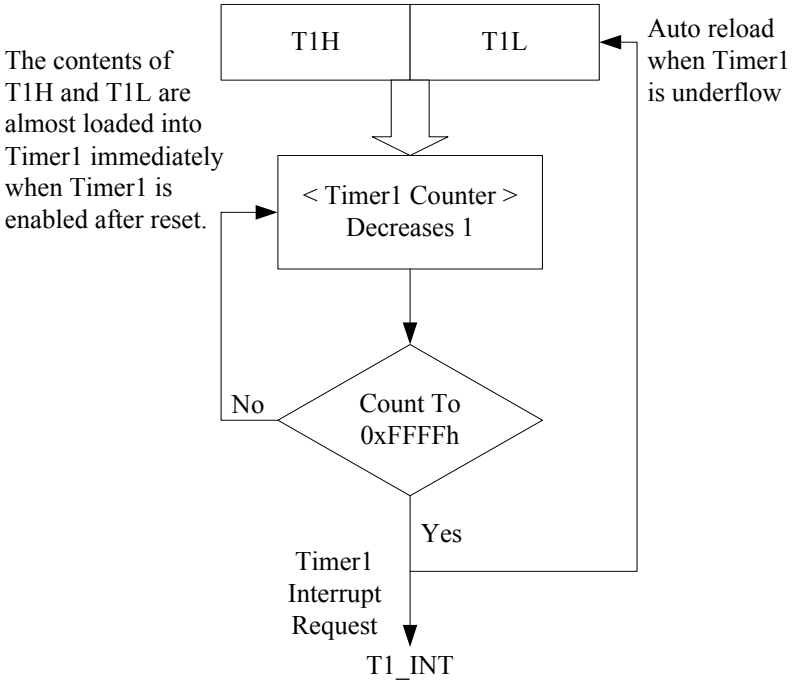
xx: Displayable, but may have abnormal leakage current, do not use.

7. Timer1

The Timer1 consists of two 8-bit write-only preload registers T1H and T1L and 16-bit down counter. If Timer1 is enabled, the counter will decrement by one with each incoming clock pulse. Timer1 interrupt will be generated when the counter underflows - counts down to FFFFH. And the counter will be automatically reloaded with the value of T1H and T1L.

The clock source of Timer1 is derived from slow clock “SCK” at dual clock or slow clock only mode. And it comes from the fast clock “FCK” at fast clock only mode.

Please note that the interrupt is generated when counter counts from 0000H to FFFFH. If the value of T1H and T1L is N, and count down to FFFFH, the total count is N+1. The content of counter is zero when system resets. Once it is enabled to count at this moment, interrupt will be generated immediately and value of T1H and T1L will be loaded since it counts to FFFFH. So the T1H and T1L value should be set before enabling Timer1.



The Timer1 related control registers are list as below:

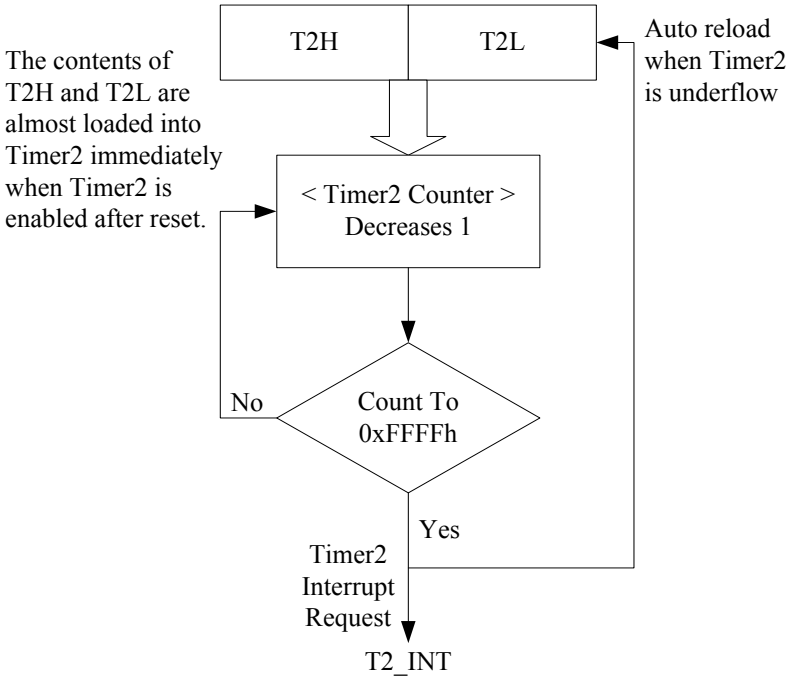
Register	Address	Field	Bit position	Mode	Description
IER	0x02	TC1_IER	2	R/W	0: TC1 interrupt is disabled. (default) 1: TC1 interrupt is enabled.
T1L	0x03	T1L[7:0]	7~0	W	Low byte of TC1 pre-load value
T1H	0x04	T1H[7:0]	7~0	W	High byte of TC1 pre-load value
OP1	0x09	TC1E	2	R/W	0: TC1 is disabled. (default) 1: TC1 is enabled.

8. Timer2

Timer2 is similar in structure to Timer1 except that clock source of Timer2 comes from the system clock "Fsys"/1.5. The system clock "Fsys" varies depending on the operation modes of the MCU.

The Timer2 consists of two 8-bit write-only preload registers T2H and T2L and 16-bit down counter. If Timer2 is enabled, counter will decrement by one with each incoming clock pulse. Timer2 interrupt will be generated when the counter underflows - counts down to FFFFH. And it will be automatically reloaded with the value of T2H and T2L.

Please note that the interrupt signal is generated when counter counts from 0000H to FFFFH. If the value of counter is N, and count down to FFFFH, the total count is N+1. The content of counter is zero when system resets. Once it is enabled to count at this time, the interrupt will be generated immediately and value of T2H and T2L will be loaded since the counter counts to FFFFH. So the T2H and T2L value should be set before enabling Timer2.



The Timer2 related control registers are list as below:

Register	Address	Field	Bit position	Mode	Description
IER	0x02	TC2_IER	1	R/W	0: TC2 interrupt is disabled. (default) 1: TC2 interrupt is enabled.
T2L	0x05	T2L[7:0]	7~0	W	Low byte of TC2 pre-load value
T2H	0x06	T2H[7:0]	7~0	W	High byte of TC2 pre-load value
OP1	0x09	TC2E	3	R/W	0: TC2 is disabled. (default) 1: TC2 is enabled.

9. Time Base

The TB timer is used to generate time-out interrupt at fixed period. The time-out frequency of TB is determined by dividing slow clock with a factor selected in OP2[3..0]. TBE (Time Base Enable) bit controls enable or disable of the circuit.

OP2	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	IDLE	PNWK	TCWK	TBE	TBS[3..0]			
Mode	R/W	R	R	R/W	R/W	R/W	R/W	R/W
Reset	0	-	-	0	-	-	-	-

TBE	Function
0	Disable Time Base
1	Enable Time Base

For example, if the slow clock is 32768 Hz, then the interrupt frequency is as shown in following table.

TBS[3..0]	Interrupt Frequency

TBS[3..0]	Interrupt Frequency
0000	16.384 KHz
0001	8.192 KHz
0010	4.096 KHz
0011	2.048 KHz
0100	1.024 KHz
0101	512 Hz
0110	256 Hz
0111	128 Hz
1000	64 Hz
1001	32 Hz
1010	16 Hz
1011	8 Hz
1100	4 Hz
1101	2 Hz
1110	1 Hz
1111	0.5 Hz

10. Watch Dog Timer

Watch Dog Timer (WDT) is designed to reset system automatically and prevents system dead lock caused by abnormal hardware activities or program execution. The WDT needs to be enabled in Mask Option.

MO_WDTE	Function
0	WDT disable
1	WDT enable

Using the WDT function, the "CLRWDT" instruction needs to be executed in every possible program path when the program runs normally in order to clears the WDT counter before it overflows, so that the program can operate normally. When abnormal conditions happen to cause the MCU to divert from normal path, the WDT counter will not be cleared and reset signal will be generated to reset the system.

The WDT clock source is the same as TC1 (Timer1 clock), and the WDT reset signal is generated when the counter had counted 32768 clock. The WDT can function in Normal, Slow and Idle Mode. However, WDT will not function during Sleep Mode (as the TC1 clock has stopped).

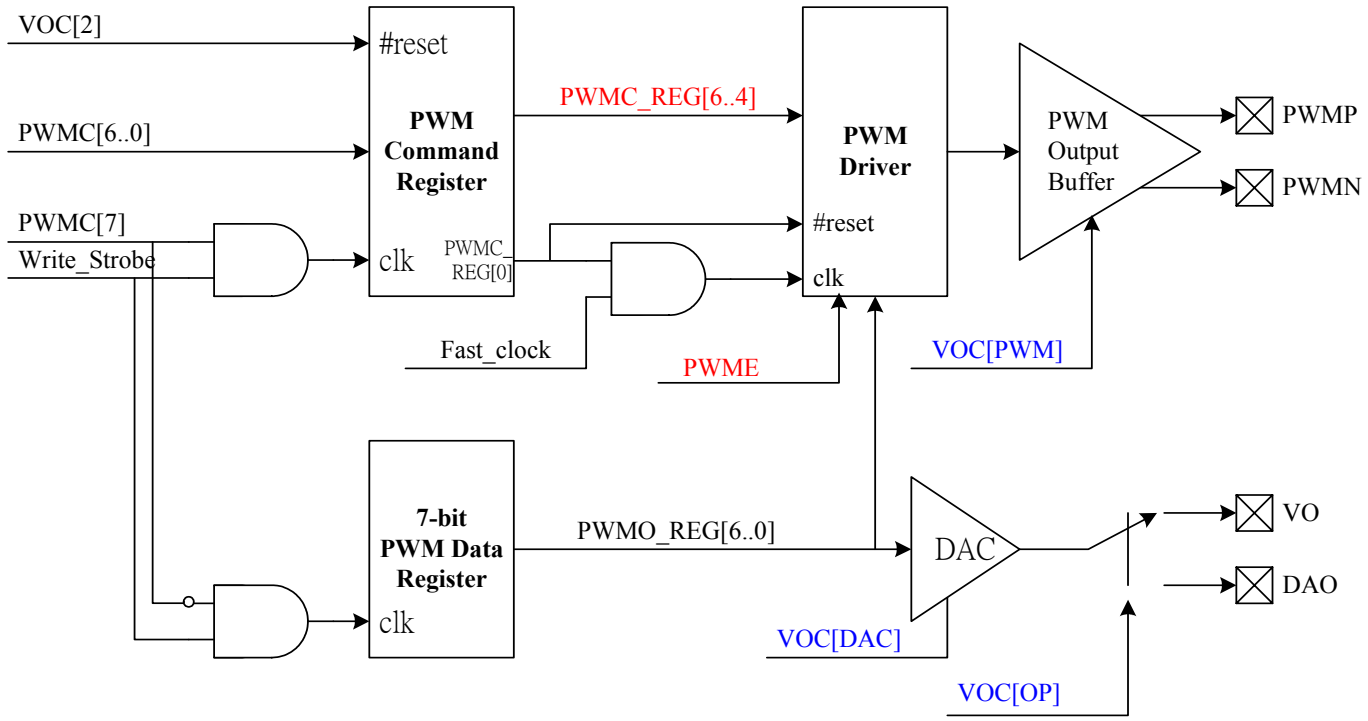
11. PWM & DAC

The 7-bit DAC/PWM voice output is available for user. The 7-bit voice output is controlled by PWMC and VOC register, and the PWMC is a command/data register which is determined by PWMC[7] bit. The Digital-to-Analog converter converts the 7-bit unsigned speech data which is written into PWMC data register to proportional current output.

PWMC register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Data Mode	0	DAC and PWM Output Data						
Control Mode	1	PWM O/P driver			Reserved			PWME

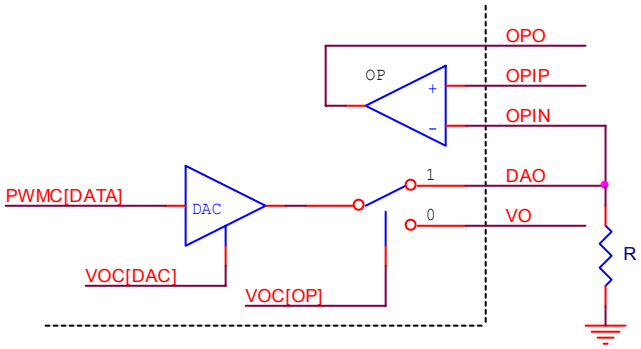
When users write data into the PWMC register, the PWMC[7] bit will determines the data written into PWM command register or 7-bit data register and the data register is also sent to the DA converter shown as the below diagram.

7-bit Voice Output Architecture



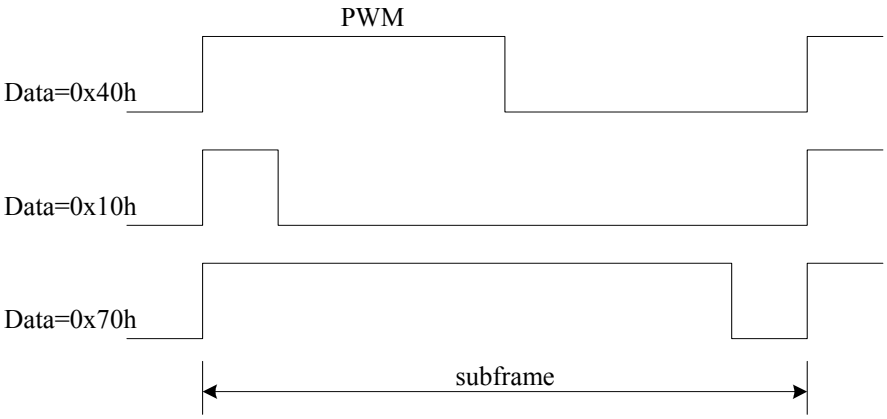
VOC	address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	0x13	-	-	-	-	-	PWM	DAC	OP
Reset	-	-	-	-	-	-	0	0	0
PWM: '1' PWM output enabled; '0' PWM output disabled. DAC: '1' DAC enabled; '0' DAC disabled. OP: '1' DAC uses DAO pin as output pin; '0' DAC uses VO pin as output pin.									

There are two output paths for the DAC. Either VO or DAO can be selected as output port of DAC by VOC register when it is enabled. The VO output is primarily intended for speech generation, although it is not necessary so, while the DAO output path can be used in conjunction with built-in OP comparator to function as an Analog-to-Digital Converter as required in applications such as speech recording, speech recognition or sensor interfaces.



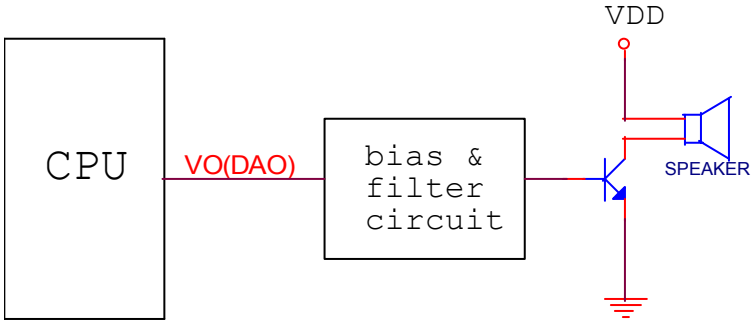
The DAC is enabled by DAC bit of VOC register. When DAC is enabled, the DAC output path can be selected to output to DAO or VO pin by OP bit of VOC register.

The fast clock is used to provide as PWM driver time base, and user shall set the PWMC[7]='1' and VOC[2]='1' to enable the PWM output. When the system enters into sleep or idle mode, it will automatically turn off the voice device by clearing VOC[2:0] to "000". In order to activate voice output again when the system returns and enter into normal mode, the related bits of VOC register need to be set again.



When the DAC is used as sound generator, the bias & filter circuit is used for bias voltage setting and waveform filter regulation and the DAC is output to the VO (Voice Output) pin and please see application notes for detailed calculation example and application. The driving capability of DAC is shown below.

	Condition	Min.	Typ.	Max.	Unit
VO/DAO	V_{DD}=3V;VO=0~2V;Data=7Fh	2.5	3		mA



The PWM output volume can be adjusted by command register PWMC[6..4]. The bit 6 and 5 control 2 time driver, while bit 4 controls 1 time driver, thus it has 5 levels of driver output. By turning on/off the internal drivers, the sound level of PWM output can be turned up and down. Please note that this adjustment apply only to PWM, but not DA output.

PWM Output Driver Selection

PWMC[6..4]	Number of Driver
000	off
001	1
010	2
011	3
100	2
101	3
110	4
111	5

12. Absolute Maximum Rating

Item	Sym.	Rating	Condition
Supply Voltage	V_{dd}	-0.5V ~ 8V	
Input Voltage	V_{in}	-0.5V ~ V_{dd}+0.5V	
Output Voltage	V_o	-0.5V ~ V_{dd}+0.5V	
Operating Temperature	T_{op}	0^0C ~ 70^0C	
Storage Temperature	T_{st}	-50^0C ~ 100^0C	

13. Recommended Operating Conditions

ITEM	SYM.	RATING	CONDITION
Supply Voltage	V_{dd}	2.4V ~ 5.5V	
Input Voltage	V_{ih}	0.9 V_{dd} ~ V_{dd}	
	V_{il}	0.0V ~ 0.1V_{dd}	
Operating Frequency	Fmax	8MHz	V_{dd} =5.0V
		4MHz	V_{dd} =2.4V
Operating Temperature	T_{op}	0^0C ~ 70^0C	
Storage Temperature	T_{st}	-50^0C ~ 100^0C	

14. AC/DC Characteristics

Testing condition : TEMP=25℃, VDD=3V+/-10%, GND=0V

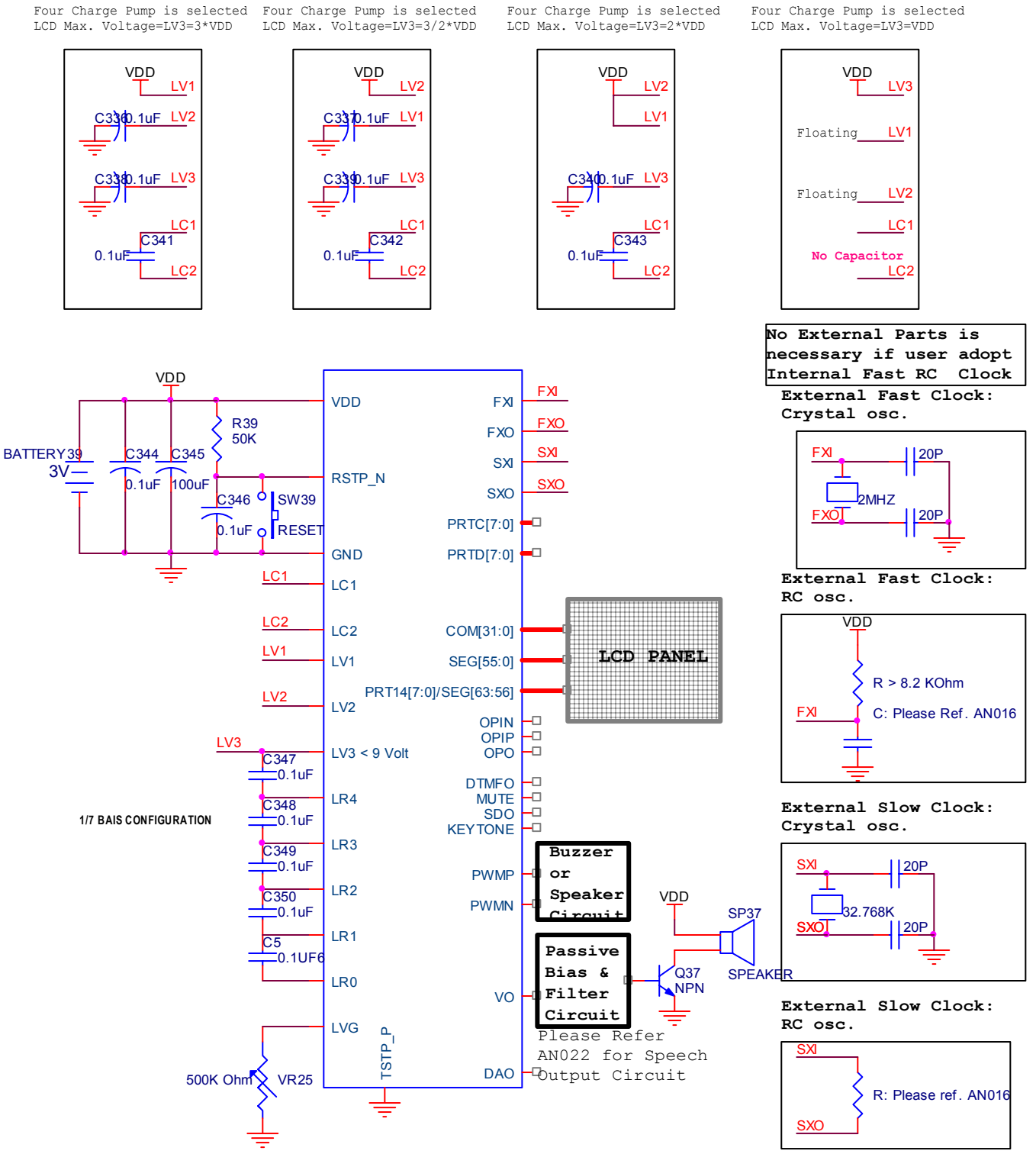
	PARAMETER		CONDITION	MIN	TYP	MAX	UNIT
I_{Fast}	NORMAL Mode Current	System	2M ext. R/C		1	1.5	mA
I_{Slow}	SLOW Mode Current	System	32.768K X'tal LCD Disable		15	25	μA
I_{Idle}	IDLE Mode Current	System	32.769K X'tal LCD Disable		10	20	μA
I_{LCD}	Extra Current if LCD ON	System	LCD Enable, LCD option=300Kohm LV3=6 Volt		40	45	μA
			LCD Enable, LCD option=30Kohm, LV3=6 Volt		300	330	
I_{Sleep}	Sleep Mode Current	System				1	μA
I_{PWM}	PWM Output Current	PWMP, PWMN*2	With 32Ω Loading	10	14		mA
			With 64Ω Loading	6	8		mA
			With 100Ω Loading	4	5		mA
I_{oVO}	DAC Output Current	VO, DAO	V_{DD}=3V;VO=0~2V, Data=7F	2.5	3		mA
V_{iH}	Input High Voltage	I/O pins		0.8 V_{DD}			V
V_{iL}	Input Low Voltage	I/O pins				0.2 V_{DD}	V
V_{hys}	Input Hysteresis Width	I/O, RSTP_N	Threshold=2/3V_{DD}(input from low to high) Threshold=1/3V_{DD}(input from high to low)		1/3 V_{DD}		V
I_{oH}	Output Drive Current	I/O pull-high*1	V_{oL}=2.0V	50			μA
I_{oL_1}	Output Sink Current	I/O pull-low*1	V_{oL}=0.4V	1.0			mA
I_{iL_1}	Input Low Current	RSTP_N	V_{iL}=GND, pull high Internally		20		μA
I_{iL_2}	Input Low Current	I/O	V_{iL}=GND, if pull high Internally by user		100		μA

Note:

*1: Drive Current Spec. for Push-Pull I/O port only Sink Current Spec. for both Push-Pull and Open-Drain I/O port.

*2: This Spec. base on one driver only. There are five build-in drivers, so user just multiplies the number of driver he used to one driver current to get the total amount of current. (I_{PWM} * N; N=0,1,2,3,4,5)

15. Application Circuit



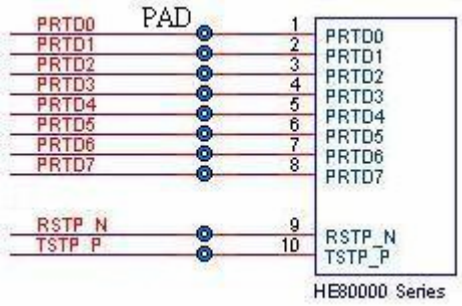
16. Important Note

- **Please always take in mind that ICE is different from IC which is your target body. ICE is the whole set of HE80000 series IC, but each IC is a subset of ICE. Never use any hardware resource that your target IC didn't have these resources, especially RAM and register. KBIDS and compiler cannot prevent user to use some hardware resources that don't exist in your target IC. Please check the following table and refer to the abbreviation in HE80000 user's manual.**

- **To access any address larger than 64KB, users must update TPP first, TPH, and then TPL. Only follow this order, the pre-charge circuit of ROM will work correctly. 5us waiting is necessary before LDV instruction is executed since Data ROM is a low speed ROM. Users can not emulate this accessing process in ICE. So 5us delay should be added by firmware.**

- **LCD driving circuit must be turn off before IC goes into sleep mode.**

- **Please bonds the TSTP_P, RSTP_N and PRTD [7:0] with test points on PCB (can be soldered and probed) as you can, then some testing can be performed on PCB if necessary. The TSTP_P is suggested to connect to ground by a 0 ohm resistor. The following figure is an example (Testing point with through hole).**



17. Updated History

Version	Date	Update History
V1.0	9/29/03	New Created