

KAF - 1301E

1280 (H) x 1024 (V) Pixel

Full-Frame CCD Image Sensor

Performance Specification

Eastman Kodak Company

Image Sensor Solutions

Rochester, New York 14650-2010

Revision 3

February 5, 2003



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1.1 Features

- **1.3M Pixel Area CCD**
- **1280H x 1024V (16 mm) Pixels**
- **Transparent Gate True Two Phase**
- **Technology (Enhanced Spectral Response)**
- **20.48 mm H x 16.38 mm V Photosensitive Area**
- **2-Phase Register Clocking**
- **Low Dark Current ($<15\text{pA}/\text{cm}^2$ @ 25°C)**

1.2 Description

The KAF-1301E is a high performance monochrome area CCD (charge-coupled device) image sensor with 1280H x 1024V photo-active pixels designed for a wide range of image sensing applications in the 400nm to 1000 nm wavelength band. Typical applications include military, scientific, and industrial imaging. A 75dB dynamic range is possible when operating at room temperature.

The sensor is built with a true two-phase CCD technology. This technology simplifies the support circuits that drive the sensor and reduces the dark current without compromising charge capacity.

The transparent gate results in spectral response increased ten times at 400nm, compared to a front side illuminated standard poly silicon gate technology. The sensitivity is increased 50% over the rest of the visible wavelengths.

Total chip size is 22.0 mm x 17.1 mm and is housed in a 36-pin package with an integral copper tungsten back plate providing excellent thermal conductivity.

The sensor consists of 1296 parallel (vertical) CCD shift registers each 1028 elements long. These registers act as both the photosensitive elements and as the transport circuits that allow the image to be sequentially read out of the sensor. The elements of these registers are arranged into a 1280 x 1024 photosensitive array surrounded by a light shielded dark reference of 16 columns and 4 rows. Parallel (vertical) CCD registers transfer the image one line at a time into a single 1304 element (horizontal) CCD shift register. The horizontal register transfers the charge to a single output amplifier. The output amplifier is a two-stage source follower that converts the photo-generated charge to a voltage for each pixel.

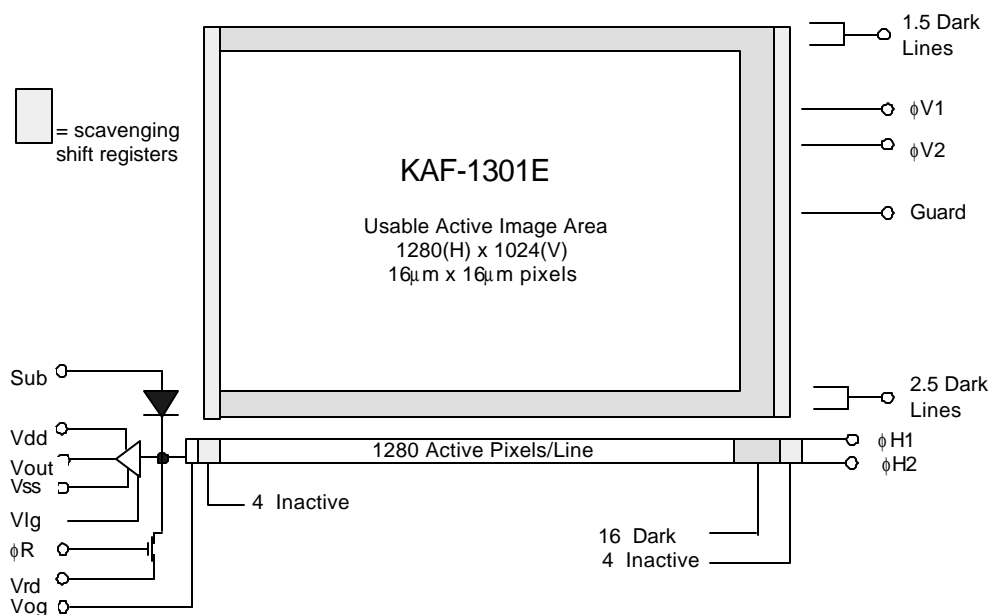


Figure 1 - Functional Block Diagram



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1.3 Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the sensor. These photon-induced electrons are collected locally by the formation of potential wells at each photo-gate or pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the pixel's capacity is reached, the charge will 'bloom' into vertically adjacent pixels. During the integration period, the $\phi V1$ and $\phi V2$ register clocks are held at a constant (low) level.

See Figure 5 - Timing Diagrams.

1.4 Charge Transport

Referring again to Figure 5 - Timing Diagrams, the integrated charge from each photo gate is transported to the output using a two step process. Each line (row) of charge is first transported from the vertical CCD to the horizontal CCD register using the $\phi V1$ and $\phi V2$ register clocks. The horizontal CCD is presented a new line on the falling edge of $\phi V2$ while $\phi H1$ is held high. The horizontal CCD then transports each line, pixel by pixel, to the output structure by alternately clocking the $\phi H1$ and $\phi H2$ pins in a complementary fashion. On each falling edge of $\phi H1$ a new charge packet is transferred onto a floating diffusion and sensed by the output amplifier.

1.5 Output Structure

Charge presented to the floating diffusion (FD) is converted into a voltage and current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on FD. Once the signal has been sampled by the system electronics, the reset gate (ϕ_R) is clocked to remove the signal and FD is reset to the potential applied by VRD. More signal at the floating diffusion reduces the voltage seen at the output pin. To activate the output structure, an off-chip load must be added to the Vout pin of the device - see Figure 4. The amplifier has a 45 MHz bandwidth.

1.6 Dark Reference Pixels

Surrounding the peripheral of the device is a border of light shielded pixels. These can be used to track the dark level if the temperature of the array is allowed to vary. Each line has 16 trailing pixels that are connected to vertical CCD registers covered with aluminum. There are also 2.5 dark lines at the start of every frame and 1.5 dark lines at the end of each frame. That is, the light shield covering the dark reference rows extend into the adjacent photo-active row. This provides better rejection of unwanted optical signal at the expense of lower response in the adjacent photo-active rows. Under normal circumstances, these pixels do not respond to light. However, dark reference pixels in close proximity to an active pixel, or the outer bounds of the chip (including the first two lines out), can scavenge signal depending on light intensity and wavelength and therefore will not represent the true dark signal.

1.7 Dummy Pixels

Within the horizontal shift register are 4 leading and 4 trailing additional phases that are not associated with a column of pixels within the vertical register. These pixels contain only horizontal shift register dark current and do not respond to light. A few leading dummy pixels may scavenge false signal depending on operating conditions.

There are several columns of dummy vertical CCD adjacent to the photo active and light shielded vertical CCD that act to scavenge unwanted stray signal away from the imaging area. These columns are not connected to the horizontal register so their presence does not have to be taken into account when clocking out each line. They transfer their charge in a direction opposite of the photo-active columns and the charge is removed through a connection to Vdd.



2.1 Pin Description

Pin	Symbol	Description	Pin	Symbol	Description
3, 4, 33, 34	ϕ_{V2}	Vertical (Parallel) CCD Clock - Phase 2	16	VLG	Amplifier Load Gate
5, 6, 31, 32	ϕ_{V1}	Vertical (Parallel) CCD Clock - Phase 1	17	VOUT	Video Output
2	N/C	No connect	18	VDD	Amplifier Supply
12	VOG	Output Gate	23	ϕ_{H1}	Horizontal CCD Clock - Phase 1
13	ϕ_R	Reset Clock	24	ϕ_{H2}	Horizontal CCD Clock - Phase 2
14	VRD	Reset Drain	30	VSUB	Substrate (Ground)
15	VSS	Amplifier Supply Return	All others	N/C	No Connection (open pin)

Notes:

Pin 2 is connected to an internal test node and must be left floating (a real 'No Connect').

All other unlabelled pins are 'No Connects' and are not connected internally.

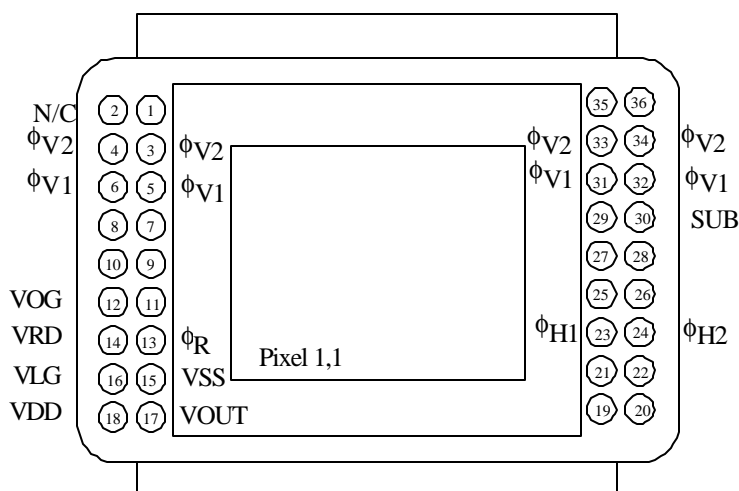


Figure 3 - Package Pin Designations



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3.1 Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Units	Notes
Diode Pin Voltages	Vdiode	0	20	V	1,2
Gate Pin Voltages - Type 1	Vgate1	-16	16	V	1,3
Gate Pin Voltages - Type 2	Vgate2	0	16	V	1,4
Inter-Gate Voltages	Vg-g		16	V	5
Output Bias Current	Iout		-10	mA	6
Output Load Capacitance	Cload		15	pF	6

Notes:

1. Referenced to pin VSUB.
2. Includes pins: VRD, VDD, VSS, VOUT.
3. Includes pins: $\phi V1$, $\phi V2$, $\phi H1$, $\phi H2$.
4. Includes pins: VOG, VLG, ϕR
5. Voltage difference between overlapping gates. Includes: $\phi V1$ to $\phi V2$, $\phi H1$ to $\phi H2$, $\phi V2$ to $\phi H1$, $\phi H2$ to VOG.
6. Avoid shorting output pins to ground or any low impedance source during operation.

Caution:

This device contains limited protection against Electrostatic Discharge (ESD) and is rated as Class 0 (<250V per JESD22 Human Body Model test), or Class A (<200V JESD22 Machine Model test.) See ISS Application Note MTD/PS-0224, Electrostatic Discharge Control. Devices should be handled in accordance with strict ESD protective procedures.

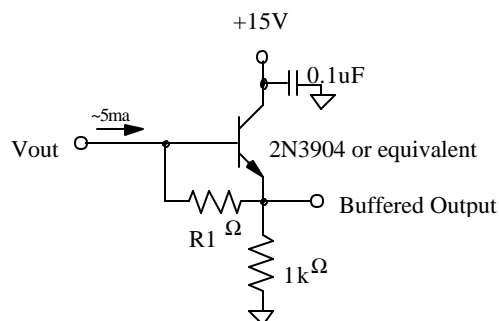


3.2 DC Operating Conditions

Description	Symbol	Min.	Nom.	Max.	Units	Max. DC Current (mA)	Notes
Reset Drain	VRD	10.5	11.0	11.25	V	0.01	
Output Amplifier Return	VSS	1.5	2.0	2.5	V	-0.5	
Output Amplifier Supply	VDD	14.5	15	15.5	V	I _{out}	
Amplifier load gate	VLG	V _{ss} + 0.0	V _{ss} + 1.0	V _{ss} + 1.5	V	0.01	
Substrate	VSUB	0	0	0	V	0.01	
Output Gate	VOG	5.0	5.5	5.7	V	0.01	
Video Output Current	I _{out}		-5	-10	mA	-	1

Notes:

1. An output load sink must be applied to V_{out} to activate output amplifier - see Figure below.



The value of R1 depends on the desired output current according to the following formula: $R1 = 0.7 / I_{out}$

The optimal output current depends on the capacitance that needs to be driven by the amplifier and the bandwidth required. 5mA is recommended for capacitance of 12pF and pixel rates up to 20 MHz.

Figure 4 - Typical output load for pixel rates of up to 10 MHz.



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3.3 AC Operating Conditions

Description	Symbol	Level	Min.	Nom.	Max.	Units	Effective Capacitance
Vertical CCD Clock - Phase 1	$\phi V1$	Low	-10.0	-9.0	-8.5	V	24nF (all $\phi V1$ pins)
		High	$\phi V1$ Low + 10.0	$\phi V1$ Low + 10.0	$\phi V1$ Low + 10.0	V	
Vertical CCD Clock - Phase 2	$\phi V2$	Low	-10.0	-9.0	-8.5	V	24nF (all $\phi V2$ pins)
		High	$\phi V2$ Low + 10.0	$\phi V2$ Low + 10.0	$\phi V2$ Low + 10.0	V	
Horizontal CCD Clock - Phase 1	$\phi H1$	Low	-2.5	-2.0	-1.75	V	100pF
		High	$\phi H1$ Low + 10.0	$\phi H1$ Low + 10.0	$\phi H1$ Low + 10.0	V	
Horizontal CCD Clock - Phase 2	$\phi H2$	Low	-2.5	-2.0	-1.75	V	100pF
		High	$\phi H2$ Low + 10.0	$\phi H2$ Low + 10.0	$\phi H2$ Low + 10.0	V	
Reset Clock	ϕR	Low	2.5	5.0	5.25	V	5pF
		High	9.0	10.0	10.5	V	

Notes:

1. All pins draw less than 10uA DC current.
2. Capacitance values relative to VSUB.

3.4 AC Timing Conditions

Description	Symbol	Min.	Nom.	Max.	Units	Notes
$\phi H1, \phi H2$ Clock Frequency	f_H		4	10	MHz	1, 2, 3
$\phi V1, \phi V2$ Clock Frequency	f_V		142	200	kHz	1, 2, 3
Pixel Period (1 Count)	t_e	100	250		ns	
$\phi H1, \phi H2$ Setup Time	t_{fHS}	0.5	1		μs	
$\phi V1, \phi V2$ Clock Pulse Width	t_{fV}	5	7		μs	2
Reset Clock Pulse Width	t_{fR}	10	20		ns	4
Readout Time	$t_{readout}$	156.7	357.7		ms	5
Integration Time	t_{int}					6
Line Time	t_{line}	152.4	348		μs	7

Notes:

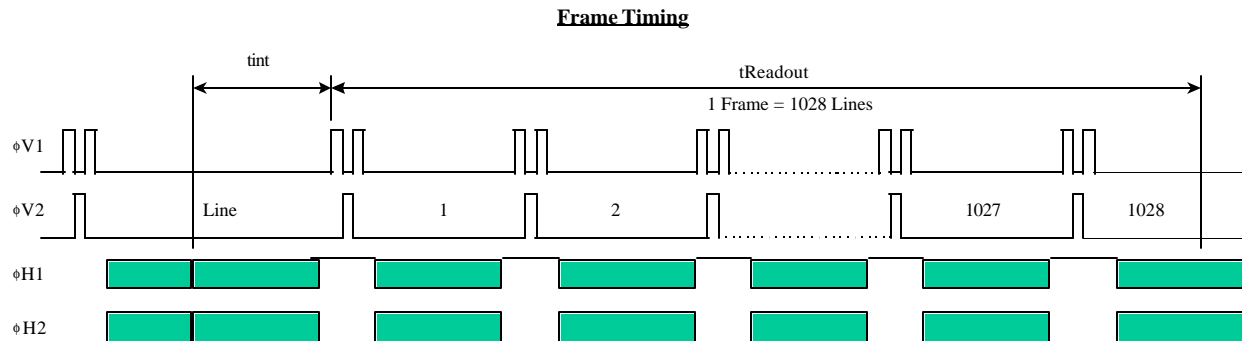
1. 50% duty cycle values.
2. CTE may degrade above the nominal frequency.
3. Rise and fall times (10/90% levels) should be limited to 5-10% of clock period. Cross-over of register clocks should be between 40-60% of amplitude.
4. f_R should be clocked continuously.
5. $t_{readout} = (1028 * t_{line})$
6. Integration time is user specified. Longer integration times will degrade noise performance due to accumulated dark signal.
7. $t_{line} = (3 * t_{\phi}) + t_{\phi HS} + (1304 * t_e) + t_e$



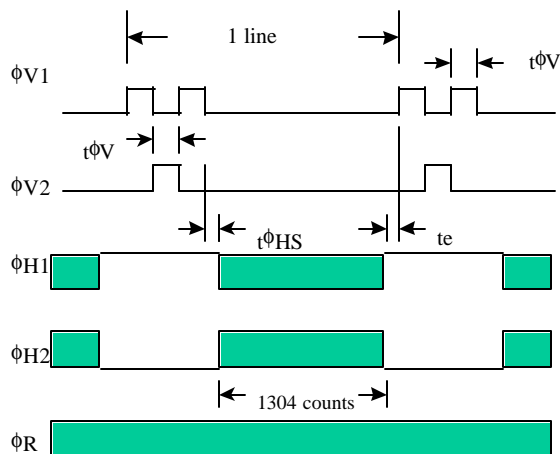
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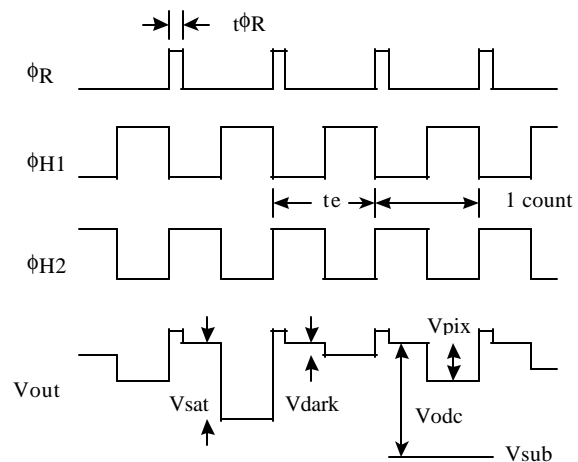
3.5 AC Timing Diagrams



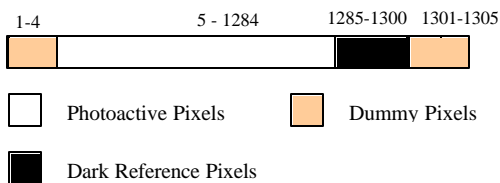
Line Timing Detail



Pixel Timing Detail



Line Content



V_{sat} Saturated pixel video output signal
 V_{dark} Video output signal in no light situation, not zero due to
 V_{pix} Pixel video output signal level. more electrons = more
 V_{dc} Video level offset with respect to v_{sub}
 V_{sub} Analog Ground

* See Image Acquisition - section 1.3 (page 4)

Figure 5 - Timing Diagrams



4.1 Performance Specifications

All values measured at 25°C, and nominal operating conditions. These parameters exclude defective pixels.

Description	Symbol	Min.	Nom.	Max.	Units	Notes
Saturation Signal						
Vertical CCD capacity	Nsat	200000	220000		electrons / pixel	1
Horizontal CCD capacity		400000	440000			
Output Node capacity		110000	120000	140000		
Red Quantum Efficiency ($\lambda=650\text{nm}$)	Rr		63		%	
Green Quantum Efficiency ($\lambda=550\text{nm}$)	Rg		55		%	
Blue Quantum Efficiency ($\lambda=450\text{nm}$)	Rb		40		%	
Photoresponse Non-Linearity	PRNL		1	2	%	2
Photoresponse Non-Uniformity	PRNU		1	3	%	3
Dark Signal	Jdark		90	240	electrons / pixel / sec	4
			6	15	pA/cm ²	
Dark Signal Doubling Temperature		5	6.3	7.5	°C	
Dark Signal Non-Uniformity	DSNU		90	240	electrons / pixel / sec	5
Dynamic Range	DR	74	77		dB	6
Charge Transfer Efficiency	CTE	0.99995	0.99998			
Output Amplifier DC Offset	Vdc	Vrd +1	Vrd+2	Vrd+2.5	V	7
Output Amplifier Bandwidth	f _{-3dB}		45		Mhz	8
Output Amplifier Sensitivity	Vout/Ne~	9	10	11	uV/e~	
Output Amplifier output Impedance	Zout	175	200	250	Ohms	
Noise Floor	ne~		15	20	electrons	9

Notes:

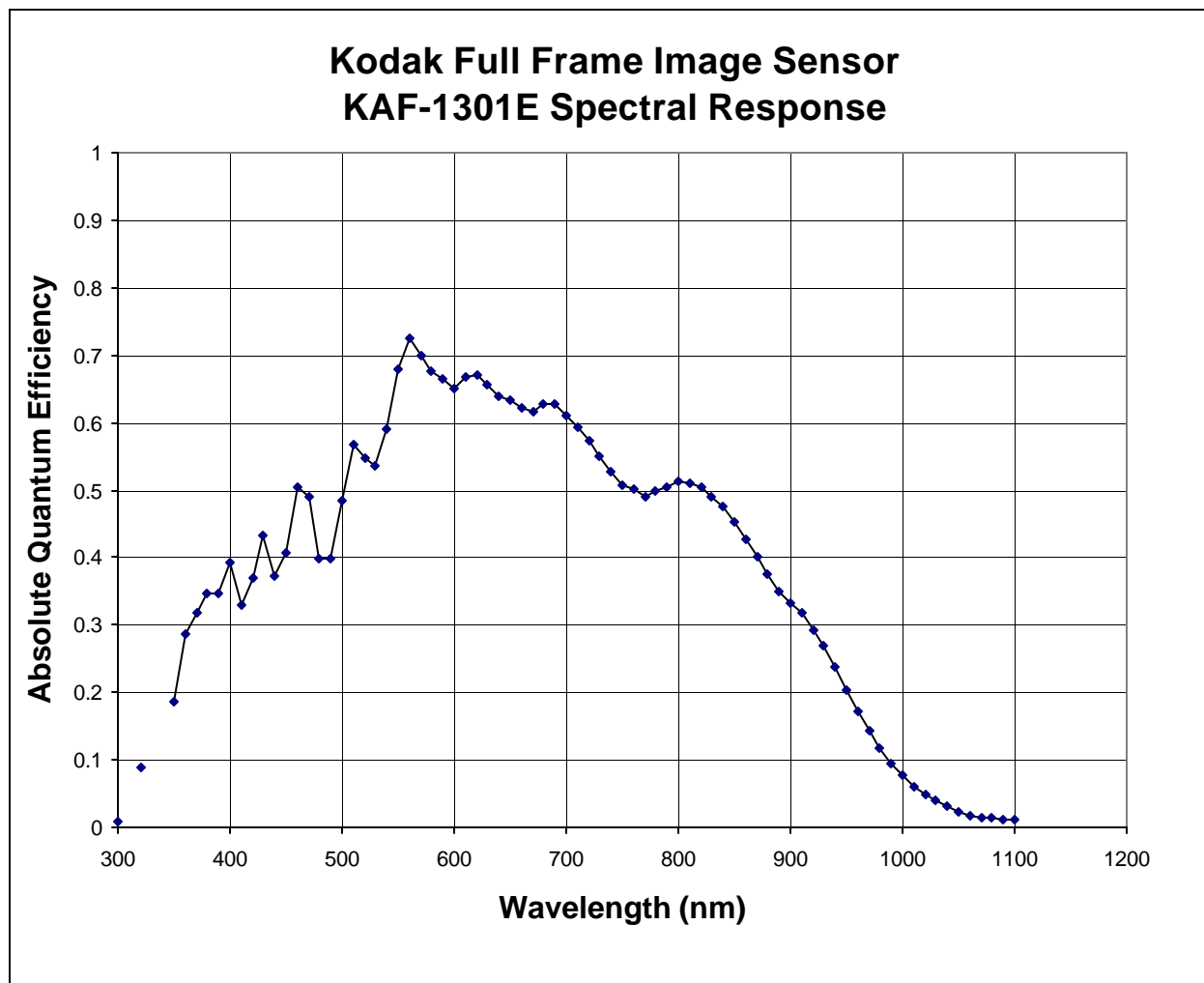
- For pixel binning applications, electron capacity up to 300000 can be achieved with modified CCD inputs. Each sensor may have to be optimized individually for these applications. Some performance parameters may be compromised to achieve the largest signals.
- Worst case deviation from straight line fit, between 1% and 90% of Vsat.
- One Sigma deviation of a 128x128 sample when CCD illuminated uniformly.
- Average of all pixels with no illumination at 25°C.
- Average dark signal of any of 10 x 8 blocks within the sensor. (each block is 128 x 128 pixels)
- $20\log (N_{\text{sat}} / n_{\text{e~}})$ where Nsat is the output node capacity, at nominal operating frequency and 25 °C.
- Video level offset with respect to ground
- Last output amplifier stage only. Assumes 10pF off-chip load..
- Output noise at -10°C, pixel rate = 1 MHz, 15MHz bandwidth, and tint = 0.



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4.2 Typical Performance Characteristics



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4.3 Cosmetic Specification

Defect tests performed at T=25°C.

Point Defects	Cluster Defects	Column Defects	Trap Defects
≤20	≤4	0	≤4

Point Defect	DARK: A pixel which deviates by more than 6% from neighboring pixels when illuminated to 70% of saturation, OR BRIGHT: A Pixel with dark current > 7500 e/pixel/sec at 25C.
Cluster Defect	A grouping of not more than 5 adjacent point defects
Column Defect	A grouping of >5 contiguous point defects along a single column, OR A column containing a pixel with dark current > 20,000e/pixel/sec, OR A column that does not meet the minimum vertical CCD charge capacity, OR A column which loses more than 150e under 2Ke illumination.
Trap Defect	A column that loses more than 50 and fewer than 150 electrons under 2000 e/pixel illumination.
Neighboring pixels	The surrounding 128 x 128 pixels or ±64 columns/rows.
Defect Separation	Column and cluster defects are separated by no less than two (2) pixels in any direction (excluding single pixel defects).
Defect Region Exclusion	Defect region excludes the outer two (2) rows and columns at each side/end of the sensor.



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5.1 Quality Assurance and Reliability

Quality Strategy: All image sensors will conform to the specifications stated in this document. This will be accomplished through a combination of statistical process control and inspection at key points of the production process. Typical specification limits are not guaranteed but provided as a design target. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

Replacement: All devices are warranted against failure in accordance with the terms of Terms of Sale. This does not include failure due to mechanical and electrical causes defined as the liability of the customer below.

Liability of the Supplier: A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer

Liability of the Customer: Damage from mechanical (scratches or breakage), electrical (ESD), or other electrical misuse of the device beyond the stated absolute maximum ratings, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

Cleanliness: Devices are shipped free of mobile contamination inside the package cavity. Immovable particles and scratches that are within the imager pixel area and the corresponding cover glass region directly above the pixel sites are also not allowed. The cover glass is highly susceptible to particles and other contamination. Touching the cover glass must be avoided. See ISS Application Note MTD/PS-0237, Cover Glass Cleaning, for further information.

ESD Precautions: Devices are shipped in static-safe containers and should only be handled at static-safe workstations. See ISS Application Note MTD/PS-0224 for handling recommendations.

Reliability: Information concerning the quality assurance and reliability testing procedures and results are available from the Image Sensor Solutions and can be supplied upon request. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

Test Data Retention: Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

Mechanical: The device assembly drawing is provided as a reference. The device will conform to the published package tolerances.

5.2 Ordering Information

Address all inquiries and purchase orders to:

Image Sensor Solutions
Eastman Kodak Company
Rochester, New York 14650-2010
Phone: (716) 722-4385
Fax: (716) 477-4947
Web: www.kodak.com/go/imagers
E-mail: imagers_a@kodak.com

Kodak reserves the right to change any information contained herein without notice. All information furnished by Kodak is believed to be accurate.



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WARNING: LIFE SUPPORT APPLICATIONS POLICY

Kodak image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company.

Product warranty is limited to replacement of defective components and does not cover injury, or property or other consequential damages.

Revision Changes:

Revision Number	Date Released	Description of Changes
0	2/2/00	Initial formal version.
1	1/13/01	Section 2.1: Corrected Package Drawing (Figure 1). Section 2.2: Corrected Note. Section 3.2: DC Operating Conditions – VOG Min. changed from 5.5V to 5.0V. Section 3.3: AC Operating Conditions – Reset Clock Low changed from 5.0 to 5.25V. Section 4.3: Cosmetic Specification – Column defect definition change from a minimum loss of 500e to a minimum loss of 150e at 2Ke illumination.
2	7/16/02	Updated ESD caution. (Section 3.1) Updated Quality and Reliability conditions. (Section 5.1) Single class device specified with Trap Defects defined. (Section 4.3) Added Trap Defect definition.
3	1/27/03	Removed obsolete table in Section 4.3.



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Package Drawing

See package drawing details in the following pages.



REVISION		
NO.	CHANGE	ECO/PCR # DATE

TABLE 1: KAF-1301NE ASSEMBLY DESCRIPTION AND PARTS LIST

PART NUMBER	MARKING CODE	DEVICE DESCRIPTION	DIE	PACKAGE	COVER	D/A ADHESIVE	BOND WIRE
1E9652	KAF-1301E S3NE S/N	MONOCHROME, ITO, TAPED CLEAR GLASS	1E9651	7B5258	7B5221	7B5597	7B5463
1E9816	KAF-1301E S3NE S/N	MONOCHROME, ITO, SEALED CLEAR GLASS	1E9651	7B5258	7B5221	7B5597	7B5463
COMPONENT NUMBER			①	②	③	④	⑤

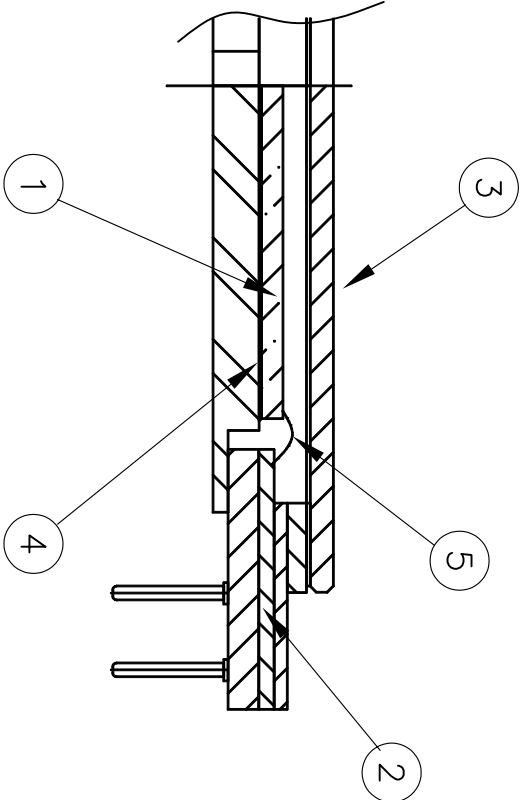
PIN OUT TABLE

PIN	FUNC.	PIN	FUNC.
1	N/C	19	N/C
2	N/C	20	N/C
3	ϕV2	21	N/C
4	ϕV2	22	N/C
5	ϕV1	23	ϕH1
6	ϕV1	24	ϕH2
7	N/C	25	N/C
8	N/C	26	N/C
9	N/C	27	N/C
10	N/C	28	N/C
11	N/C	29	N/C
12	OG	30	VSUB
13	ϕR	31	ϕV1
14	VRD	32	ϕV1
15	VSS	33	ϕV2
16	VLG	34	ϕV2
17	VOUT	35	N/C
18	VDD	36	N/C

NOTES:

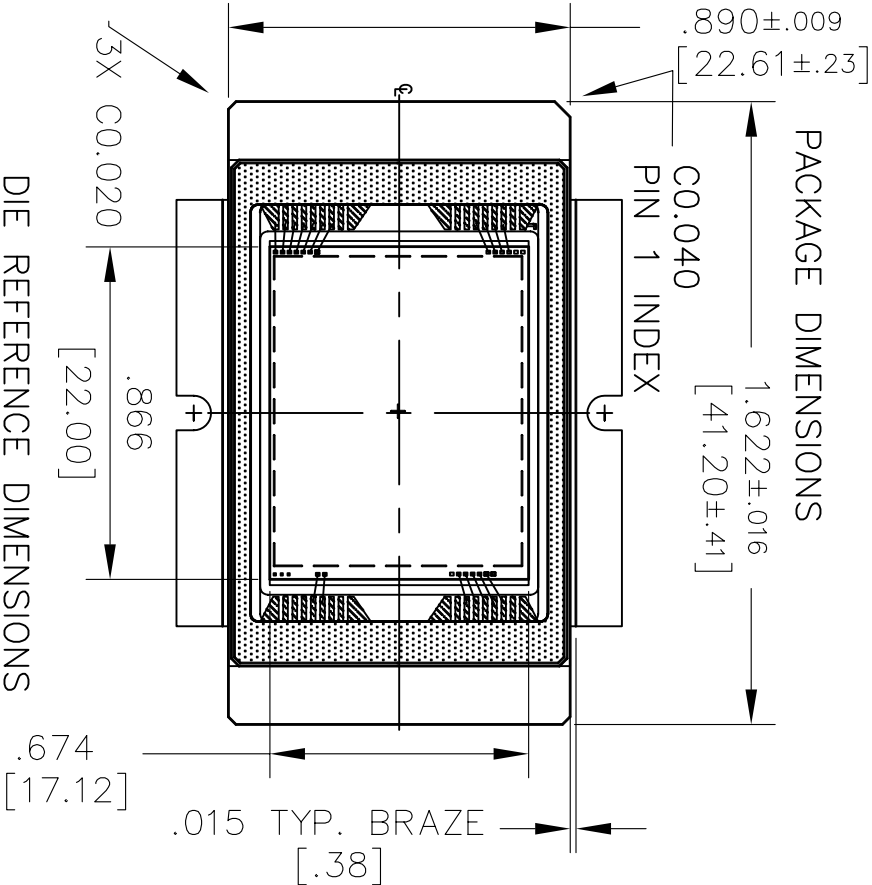
1. PINS 9 AND 30 ATTACHED TO DIE ATTACH SUBSTRATE.

DIMENSIONS		UNITS: IN [MM]	EASTMAN KODAK CO. IMAGE SENSORS SOLUTIONS ROCHESTER, NEW YORK
TOLERANCE: UNLESS OTHERWISE SPECIFIED			
CERAMIC ±1% NO LESS THAN 0.005"			
L/F ±1% NO MORE THAN 0.005"			NAME KAF-1301NE / S3NE ASSEMBLY
APPROVALS			
DESIGNED BY: M.J. CIMINELLI	DATE: 01/30/2003		
			DRAWING NUMBER KAF-1301NE
DATE APPROVED: See KAF-1301NE in System-9000			REV. 1
		SHEET 1 of 3	DWG. SIZE B

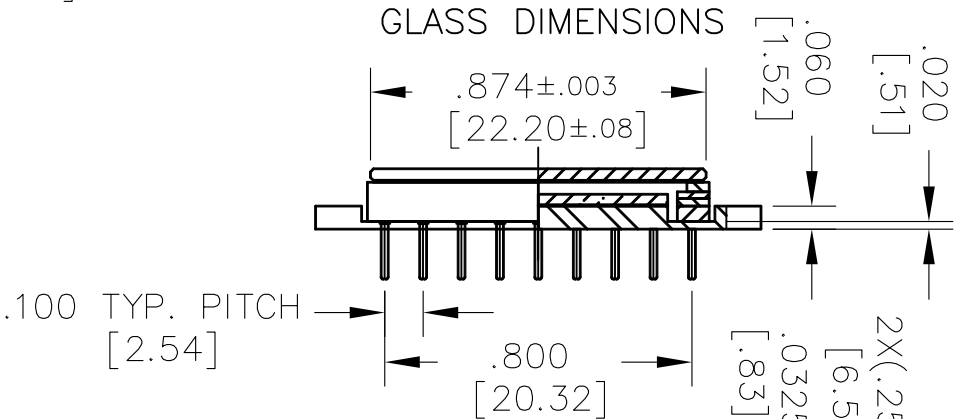


REVISION		
NO.	CHANGE	ECO/PCR # DATE

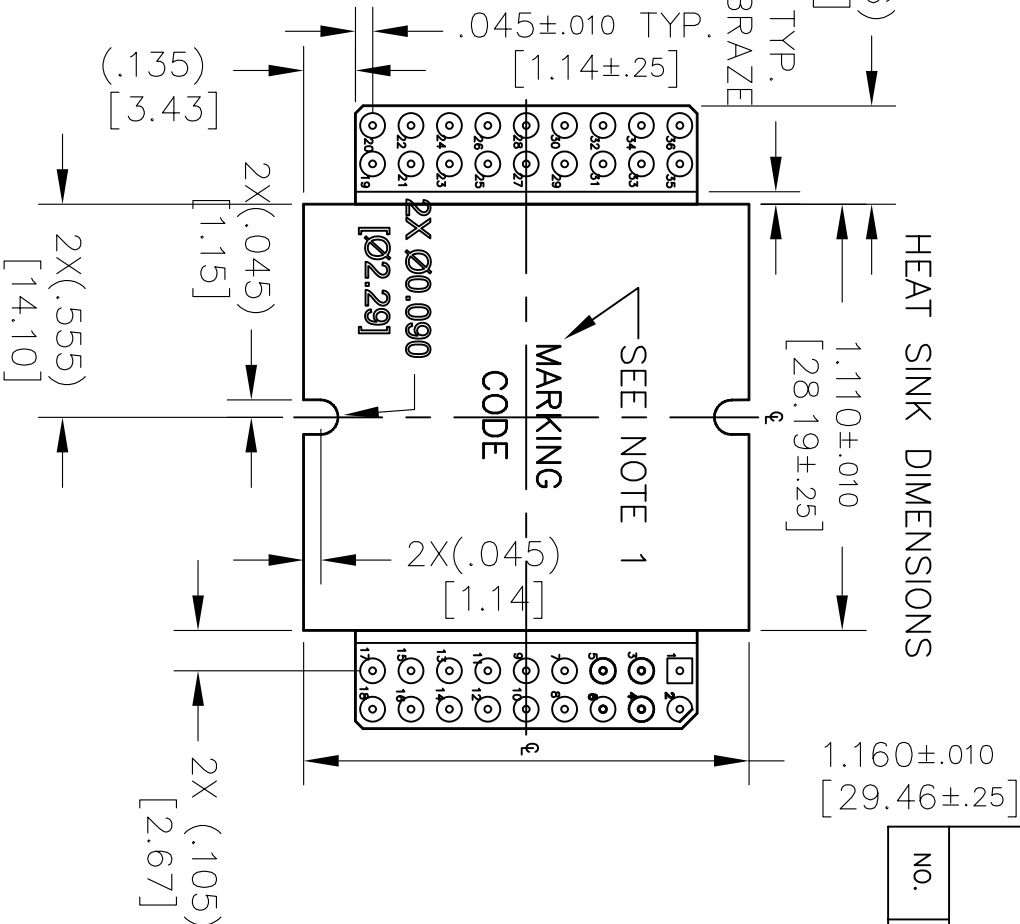
PACKAGE DIMENSIONS



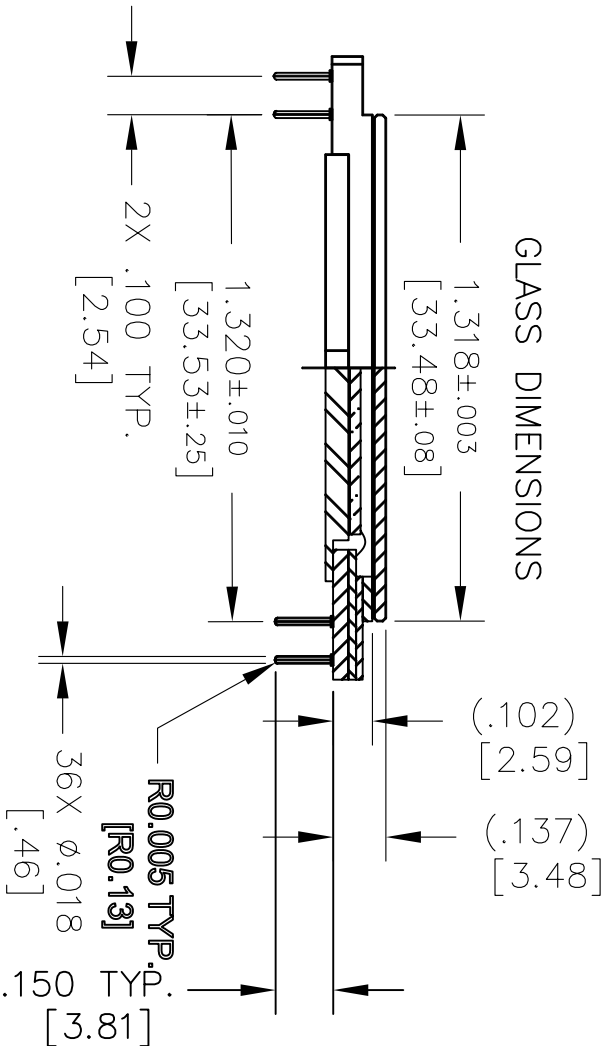
GLASS DIMENSIONS



HEAT SINK DIMENSIONS



GLASS DIMENSIONS

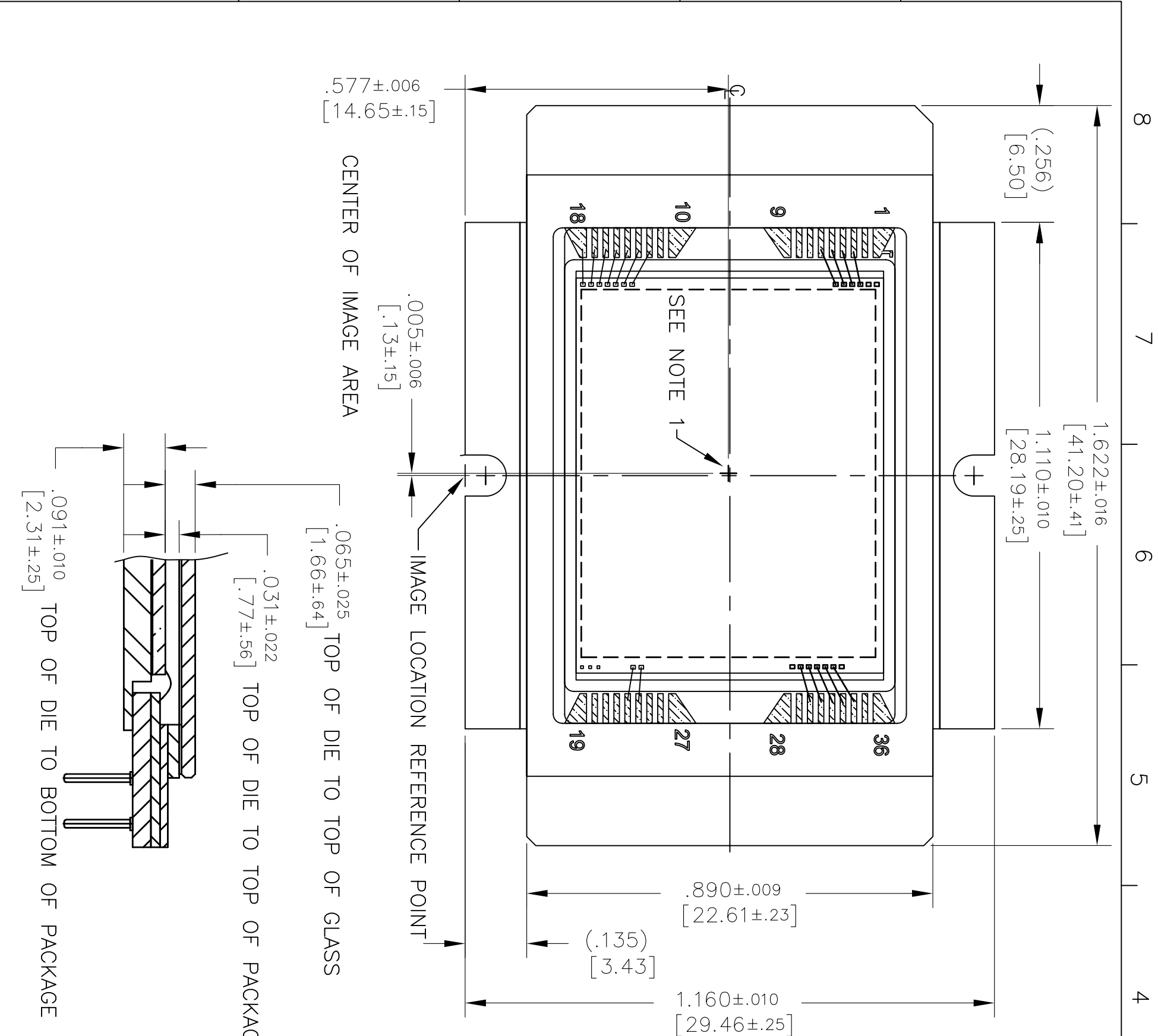


NOTES:

1. SEE TABLE 1 FOR MARKING CODE
2. COVER GLASS IS VISUALLY ALIGNED
3. OVER DIE – NO GUARANTEE OF LOCATION ACCURACY.

DIMENSIONS	UNITS: IN [MM]	EASTMAN KODAK CO. IMAGE SENSORS SOLUTIONS ROCHESTER, NEW YORK		
TOLERANCE: UNLESS OTHERWISE SPECIFIED CERAMIC ±1% NO LESS THAN 0.005" L/F ±1% NO MORE THAN 0.005"		NAME KAF-1301NE / S3NE		
APPROVALS		DRAWING NUMBER KAF-1301NE		
DESIGNED BY: M.J. CIMINELLI	DATE: 01/30/2003	REV. 1		
DATE APPROVED: See KAF-1301NE in System-9000		SHEET 2 of 3	DWG. SIZE B	

REVISION		
NO.	CHANGE	ECO/PCR # DATE



DIMENSIONS	UNITS: IN [MM]	EASTMAN KODAK CO.	
TOLERANCE: UNLESS OTHERWISE SPECIFIED		IMAGE SENSORS SOLUTIONS	
CERAMIC $\pm 1\%$ NO LESS THAN 0.005"		ROCHESTER, NEW YORK	
L/F $\pm 1\%$ NO MORE THAN 0.005"		NAME	
APPROVALS		KAF-1301NE / S3NE	
DESIGNED BY:	DATE:	DRAWING NUMBER	
M.J. CIMINELLI	01/30/2003	KAF-1301NE	
		REV.	
		1	
DATE APPROVED:		SHEET	
See KAF-1301NE in System-9000		3 of 3	
		DWG. SIZE	
		B	