

DEVICE  
PERFORMANCE  
SPECIFICATION

# **KODAK KAI-0330D**

## **Image Sensor**

648 (H) x 484 (V)  
Interline Transfer  
Progressive Scan CCD

June 3, 2003  
Revision 2.0

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## Features

- Front Illuminated Interline Architecture
- 648 (H) x 484 (V) Photosensitive Pixels
- 9.0 $\mu\text{m}$ (H) x 9.0 $\mu\text{m}$ (V) Pixel Size
- 5.83 mm(H) x 4.36 mm(V) Photosensitive Area
- Progressive Scan (Noninterlaced)
- Electronic Shutter
- Integral RGB Color Filter Array (optional)
- Advanced 2 Phase Buried Channel CCD
- On-Chip Dark Reference Pixels
- Low Dark Current
- Patented High Sensitivity Output Structure
- Dual Output Shift Registers
- Antiblooming Protection
- Negligible Lag
- Low Smear (0.01% with microlens)

## Processing

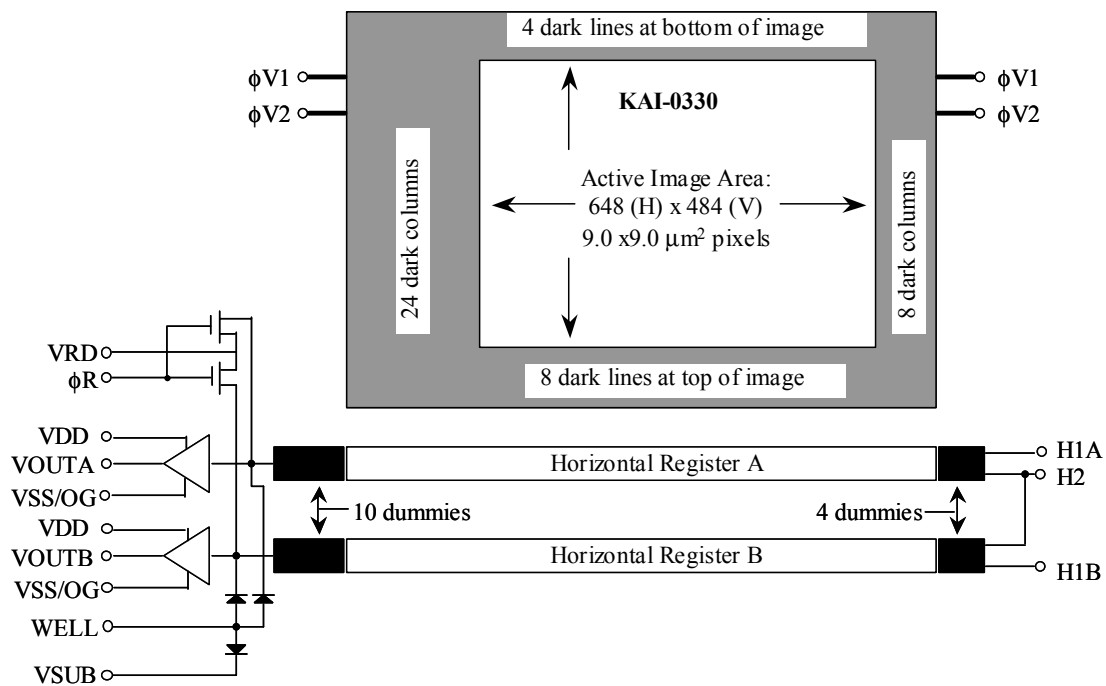


Figure 1 Functional Block Diagram

## Description

The KAI-0330D series is a VGA resolution charge coupled device (CCD) image sensor whose noninterlaced architecture makes it ideally suited for video, electronic still and motion/still camera applications. The device is built using an advanced true two-phase, double-polysilicon, NMOS CCD technology. The p+npn-photodetector elements eliminate image lag and reduce image smear while providing antiblooming protection and electronic-exposure control. The total chip size is 7.3 (H) mm x 5.52 (V) mm. The KAI-0330D comes in monochrome and color versions, both with microlens for sensitivity improvement.

Device	Color	Microlens
KAI-0330D	No	No
KAI-0330DM	No	Yes
KAI-0330DCM	Yes	Yes

## Architecture

The KAI-0330D consists of 648 x 484 photodiodes, 680 vertical (parallel) CCD shift registers (VCCDs), and dual 496 pixel horizontal (serial) CCD shift registers (HCCDs) with independent output structures. The device can be operated in either single or dual line mode. The advanced, progressive-scan architecture of the device allows the entire image area to be read out in a single scan. The active pixels are surrounded by an additional 32 columns and 12 rows of light-shielded dark reference pixels.

## Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the individual silicon photodiodes. These photoelectrons are collected locally by the formation of potential wells at each photosite. Below photodiode saturation, the number of photoelectrons collected at each pixel is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the photodiode's charge capacity is reached, excess electrons are discharged into the substrate to prevent blooming.

## Charge Transport

The accumulated or integrated charge from each photodiode is transported to the output by a three-step process. The charge is first transported from the photodiodes to the VCCDs by applying a large positive voltage to the phase-one vertical clock ( $\phi V1$ ). This reads out every row, or line, of photodiodes into the VCCDs.

The charge is then transported from the VCCDs to the HCCDs line by line. Finally, the HCCDs transport these rows of charge packets to the output structures pixel by pixel. On each falling edge of the horizontal clock,  $\phi H2$ , these charge packets are dumped over the output gate (OG, Figure 2) onto the floating diffusion (FDA and FDB, Figure 2).

Both the horizontal and vertical shift registers use traditional two-phase complementary clocking for charge transport. Transfer to the HCCDs begins when  $\phi V2$  is clocked high and then low (while holding  $\phi H1A$  high) causing charge to be transferred from  $\phi V1$  to  $\phi V2$  and subsequently into the A HCCD. The A register can now be read out in single line mode. If it is desired to operate the device in a dual line readout mode for higher frame rates, this line is transferred into the B HCCD by clocking  $\phi H1A$  to a low state, and  $\phi H1B$  to a high state while holding  $\phi H2$  low. After  $\phi H1A$  is returned to a high state, the next line can be transferred into the A HCCD. After this clocking sequence, both HCCDs are read out in parallel.

The charge capacity of the horizontal CCDs is slightly more than twice that of the vertical CCDs. This feature allows the user to perform two-to-one line aggregation in the charge domain during V-to-H transfer. This device is also equipped with a fast dump feature that allows the user to selectively dump complete lines (or rows) of pixels at a time. This dump, or line clear, is also accomplished during the V-to-H transfer time by clocking the fast dump gate.

## Output Structure

Charge packets contained in the horizontal register are dumped pixel by pixel, onto the floating diffusion output node whose potential varies linearly with the quantity of charge in each packet. The amount of potential change is determined by the expression  $\Delta V_{fd} = \Delta Q / C_{fd}$ . A three stage source-follower amplifier is used to buffer this signal voltage off chip with slightly less than unity gain.

The translation from the charge domain to the voltage domain is quantified by the output sensitivity or charge to voltage conversion in terms of  $\mu V/e^-$ . After the signal has been sampled off-chip, the reset clock ( $\phi_R$ ) removes the charge from the floating diffusion and resets its potential to the reset-drain voltage ( $V_{RD}$ ).

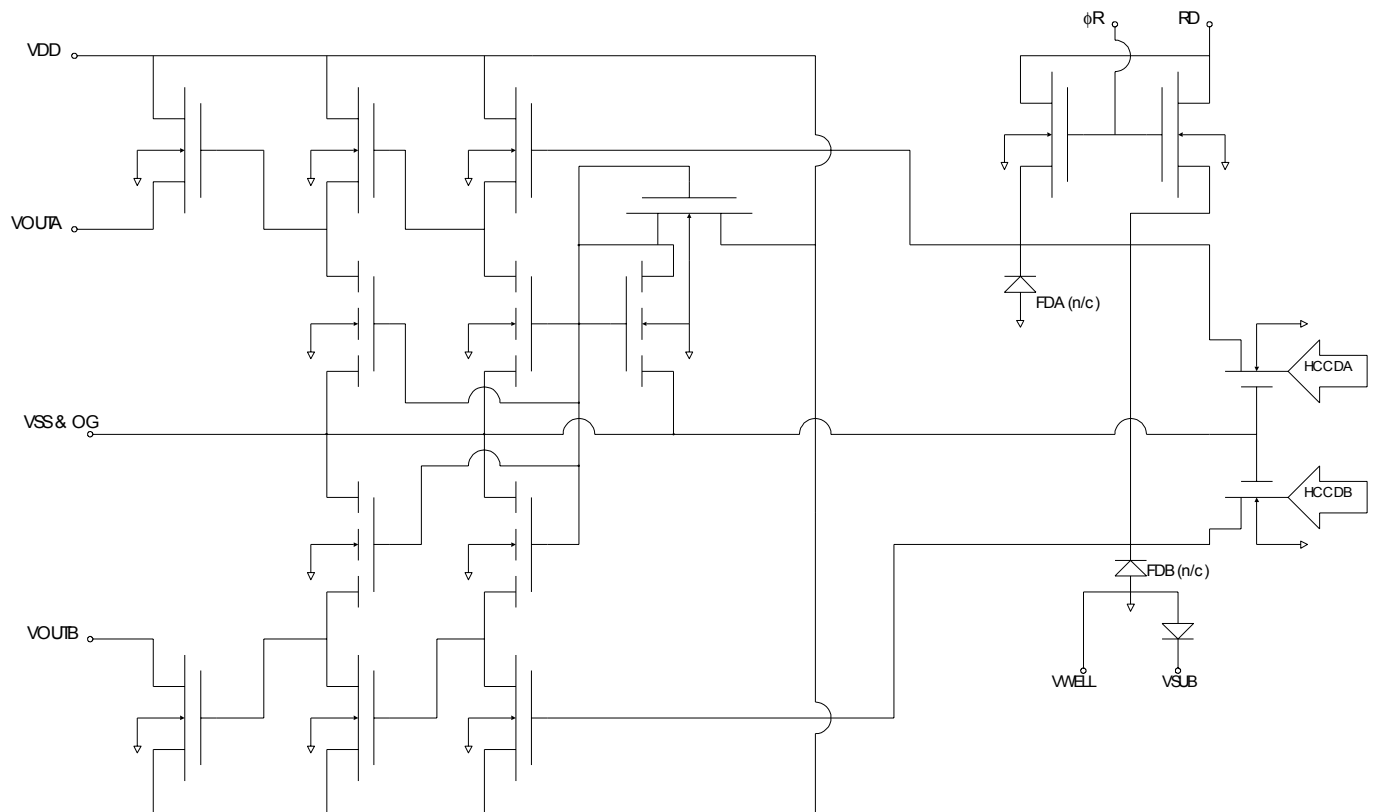


Figure 2 Output Structure

## Electronic Shutter

The KAI-0330D provides a structure for the prevention of blooming that may be used to realize a variable exposure time as well as performing the anti-blooming function. The anti-blooming function limits the charge capacity of the photodiode by draining excess electrons vertically into the substrate (hence the name Vertical Overflow Drain or VOD) . This function is controlled by applying a large potential to the device substrate (device terminal SUB). If a sufficiently large voltage pulse ( $VES \approx 40V$ ) is applied to the substrate, all photodiodes will be emptied of charge through the substrate, beginning the integration period. After returning the substrate voltage to the nominal value, charge can accumulate in the diodes and the charge packet is subsequently readout onto the VCCD at the next occurrence of the high level on  $\phi V1$ . The integration time is then the time between the falling edges of the substrate shutter pulse and  $\phi V1$ . This scheme allows electronic variation of the exposure time by a variation in the clock timing while maintaining a standard video frame rate.

Application of the large shutter pulse must be avoided during the horizontal register readout or an image artifact will appear due to feedthrough. The shutter pulse VES must be “hidden” in the horizontal retrace interval. The integration time is changed by skipping the shutter pulse from one horizontal retrace interval to another.

The smear specification is not met under electronic shutter operation. Under constant light intensity and spot size, if the electronic exposure time is decreased, the smear signal will remain the same while the image signal will decrease linearly with exposure. Smear is quoted as a percentage of the image signal and so the percent smear will increase by the same factor that the integration time has decreased. This effect is basic to interline devices.

## Color Filter Array (optional, for KAI-0330DCM only)

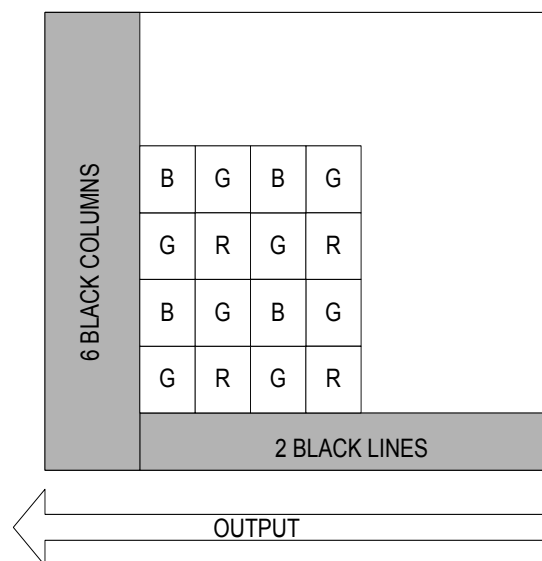


Figure 3 CFA Pattern



## Packaging Configuration

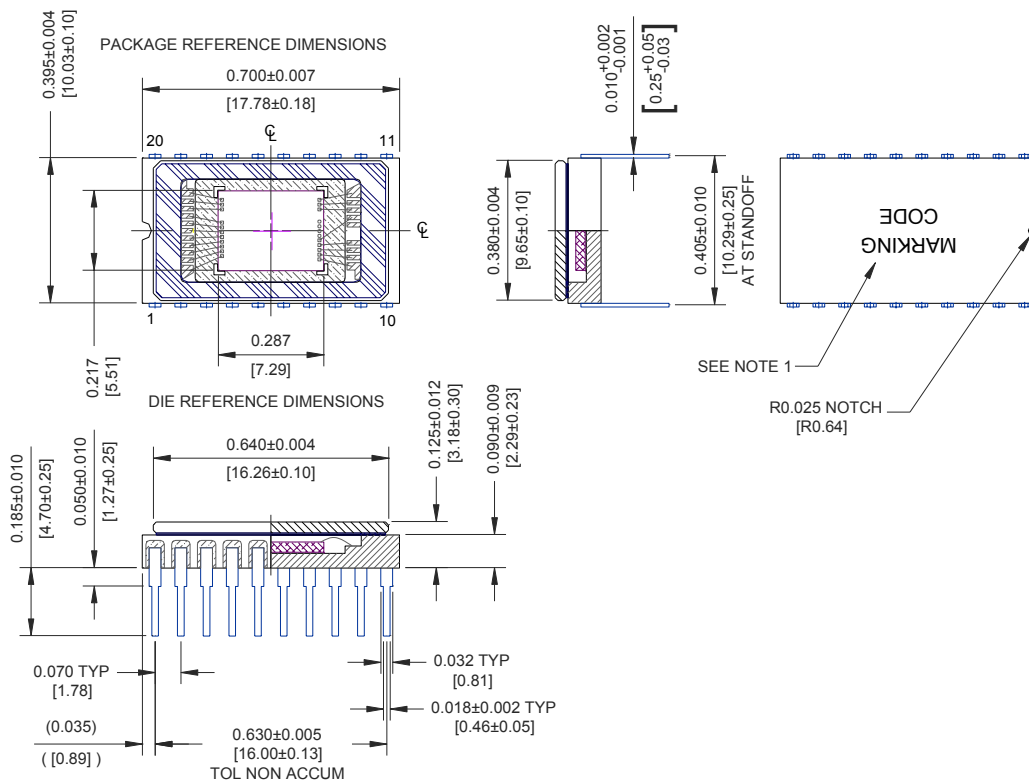


Figure 4 Device Drawing – Die Placement

Note 1:

Configuration	Marking Code
Monochrome	KAI-0330D SN
Monochrome, Microlens	KAI-0330DM SN
Color, Microlens	KAI-0330DCM SN

# Pin Description

PIN NO.	SYMBOL	DESCRIPTION	Notes
1	VoutA	Video Output Channel A	
2	Vss/OG	Output Amplifier Return and OG	
3	$\phi R$	Reset Clock	
4	Vrd	Reset Drain	
5	VoutB	Video Output Channel B	
6,8,13,16	Vwell	P-Well (Ground)	
7	$\phi H2$	A & B Horizontal CCD Clock - Phase 2	
9	$\phi H1B$	B Horizontal CCD Clock - Phase 1	
10,11	Vsub	Substrate	
12	$\phi H1A$	A Horizontal CCD Clock - Phase 1	
14	$\phi V1O$	Vertical CCD Clock - Phase 1, odd field	1
15	$\phi V1E$	Vertical CCD Clock - Phase 1, even field	1
17	$\phi V2E$	Vertical CCD Clock - Phase 2, even field	2
18	$\phi V2O$	Vertical CCD Clock - Phase 2, odd field	2
19	FDG	Fast Dump Gate	
20	VDD	Output Amplifier Supply	

Table 1 Package Pin Assignments

Notes:

1. Pins 14 and 15 must be connected together - only 1 Phase 1 clock driver is required.
2. Pins 17 and 18 must be connected together - only 1 Phase 2 clock driver is required.

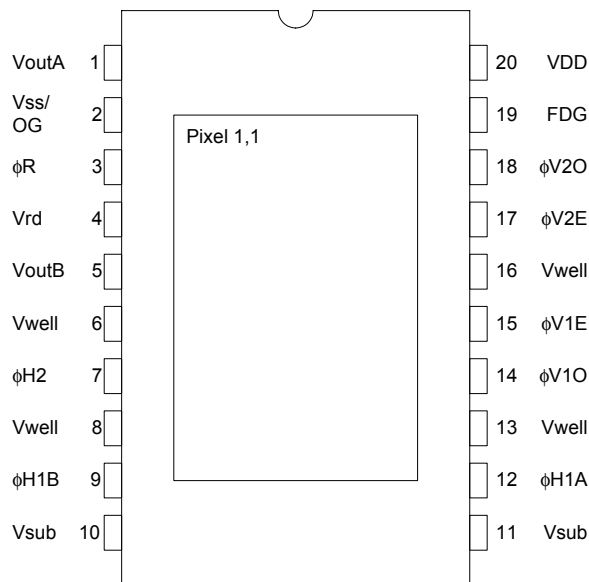


Figure 5 Pinout Diagram Top View

## Absolute Maximum Range

RATING	DESCRIPTION	MIN.	MAX.	UNITS	NOTES
Temperature (@ 10% ±5%RH)	Operation Without Damage	-50	+70	°C	
	Storage	-55	+70	°C	
Voltage (Between Pins)	SUB-WELL	0	+40	V	1
	VRD,VDD,OG&VSS-WELL	0	+15	V	2
	VOUTA & VOUTB – WELL	0	+15	V	2
	φV1 - φV2	-12	+20	V	2
	φH1A, φH1B - φH2	-12	+15	V	2
	φH1A, φH1B, φH2, FDG - φV2	-12	+15	V	2
	φH2 - OG & VSS	-12	+15	V	2
	φR – SUB	-20	0	V	1,2,4
	All Clocks – WELL	-12	+15	V	2
Current	Output Bias Current ( $I_{out}$ )	----	10	mA	3

Table 2 Absolute Maximum Ranges

- Notes:
1. Under normal operating conditions the substrate voltage should be above +7V, but may be pulsed to 40 V for electronic shuttering.
  2. Care must be taken in handling so as not to create static discharge which may permanently damage the device.
  3. Per Output.  $I_{out}$  affects the band-width of the outputs.
  4. φR should never be more positive than VSUB.

**Caution:** This device contains limited protection against Electrostatic Discharge (ESD) Devices should be handled in accordance with strict ESD procedures for Class 0 devices (JESD22 Human Body Model) or Class A (Machine Model). Refer to Application Note MTD/PS-0224, “Electrostatic Discharge Control”

**Caution:** Improper cleaning of the cover glass may damage these devices. Refer to Application Note MTD/PS-0237, “Cover Glass Cleaning for Image Sensors”

## DC Operating Conditions

SYMBOL	DESCRIPTION	MIN.	NOM.	MAX.	UNITS	PIN IMPEDANCE <sup>5</sup>	NOTES
VRD	Reset Drain	8.5	9	9.5	V	5pF, >1.2MΩ	
IRD	Reset Drain Current		0.2		mA		
VSS	Output Amplifier Return & OG		0		V	30pF, >1.2MΩ	
ISS	Output Amplifier Return Current		5		mA		
VDD	Output Amplifier Supply	12	15.0	15.5	V	30pF, >1.2MΩ	
Iout	Output Bias Current		5	10	mA		4
WELL	P-well	----	0.0	----	V	Common	1
GND	Ground	-----	0.0	----	V		1
FDG	Fast Dump Gate	-5.5	-5.0	-4.5	V	20pF, >1.2MΩ	2
SUB	Substrate	7	Vsub	15	V	1nF, >1.2MΩ	3

Table 3 DC Operating Conditions

- Notes:
1. The WELL and GND pins should be connected to P-well ground.
  2. The voltage level specified will disable the fast dump feature.
  3. This pin may be pulsed to Ves=40V for electronic shuttering
  4. Per output. Note also that I<sub>out</sub> affects the bandwidth of the outputs.
  5. Pins shown with impedances greater than 1.2 Mohm are expected resistances. These pins are only verified to 1.2 Mohm.
  6. The operating levels are for room temperature operation. Operation at other temperatures may or may not require adjustments of these voltages.

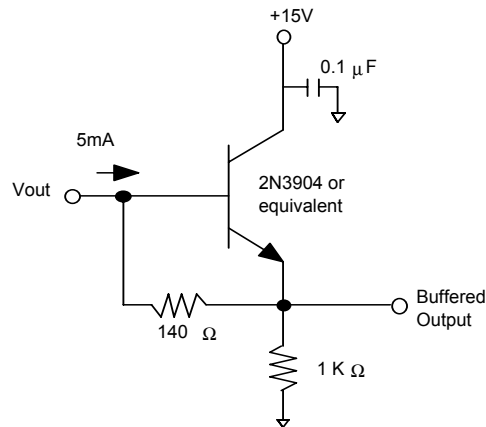


Figure 6 Recommended Output Structure Load Diagram

### Cautions:

In order to obtain maximum device performance, gate protection is not provided. Extreme care must be taken in handling to prevent electrostatic discharge that may permanently damage the device. Care must be taken not to short the outputs to ground or VDD during operations.

## AC Clock Level Conditions

SYMBOL	DESCRIPTION	Level	Min.	NOM.	MAX.	UNITS	PIN IMPEDANCE
$\phi V1$	Vertical CCD Clock	Low	-10.0	-9.5	-9.0	V	25nF, >1.2M $\Omega$
		Mid	0.0	0.2	0.4	V	
		High	8.5	9.0	9.5	V	
$\phi V2$	Vertical CCD Clock	Low	-10.0	-9.5	-9.0	V	25nF, >1.2M $\Omega$
		High	0.0	0.2	0.4	V	
$\phi H1A$	$\phi 1$ Horizontal CCD A Clock	Low	-7.5	-7.0	-6.5	V	100pF, > 1.2M $\Omega$
		High	2.5	3.0	3.5	V	
$\phi H1B^4$	$\phi 1$ Horizontal CCD B Clock (single register mode)	Low	-7.5	-7.0	-6.5	V	100pF, > 1.2M $\Omega$
$\phi H1B^4$	$\phi 1$ Horizontal CCD B Clock (dual register mode)	Low	-7.5	-7.0	-6.5	V	100pF, > 1.2M $\Omega$
		High	2.5	3.0	3.5	V	
$\phi H2$	$\phi 2$ Horizontal CCD Clock	Low	-7.5	-7.0	-6.5	V	125pF, > 1.2M $\Omega$
		High	2.5	3.0	3.5	V	
$\phi R$	Reset Clock	Low	-6.5	-6.0	-5.5	V	5pF, > 1.2M $\Omega$
		High	-0.5	0.0	0.5	V	
$\phi FDG^3$	Fast Dump Gate Clock	Low	-5.5	-5.0	-4.5	V	20pF, > 1.2M $\Omega$
		High	4.5	5.0	5.5	V	

Table 4 AC Clock Level Conditions

- Notes:
1. The AC and DC operating levels are for room temperature operation. Operation at other temperatures may or may not require adjustments of these voltages.
  2. Pins shown with impedances greater than 1.2 Mohm are expected resistances. These pins are only verified to 1.2 Mohm.
  3. When not used, refer to DC operating condition.
  4. For single register mode, set  $\phi H1B$  to -7.0 volts at all times rather than clocking it.

This device is suitable for a wide range of applications requiring a variety of different operating conditions. Consult Eastman Kodak in those situations in which operating conditions meet or exceed minimum or maximum levels.

## AC Timing Requirements for 30 MHz Operation

SYMBOL	DESCRIPTION	MIN	NOM	MAX	UNITS	NOTES	FIGURE
t $\phi$ R	Reset Pulse Width		10		nsec		Figure 9
t es	Electronic Shutter Pulse Width	10	25		$\mu$ sec		Figure 10
t int	Integration Time	0.1			msec	1	Figure 10
t $\phi$ Vh	Photodiode to VCCD Transfer Pulse Width	4	5		$\mu$ sec	2	Figure 7
t cd	Clamp Delay		15		nsec		Figure 9
t cp	Clamp Pulse Width		15		nsec		Figure 9
t sd	Sample Delay		35		nsec		Figure 9
t sp	Sample Pulse Width		15		nsec		Figure 9
t rd	Vertical Readout Delay	10	----	----	$\mu$ sec		Figure 7
t $\phi$ V	$\phi$ V1, $\phi$ V2 Pulse Width	2	2.5		$\mu$ sec		Figure 8
Clock Frequency t $\phi$ H	$\phi$ H1A, $\phi$ H1B, $\phi$ H2	----	----	30	MHz		Figure 9
t $\phi$ AB	Line A to Line B Transfer Pulse Width	2	2.5		$\mu$ sec		Figure 12
t $\phi$ Hd	Horizontal Delay	2	2.5		$\mu$ sec		Figure 8
t $\phi$ Vd	Vertical Delay	25			nsec		Figure 8
t $\phi$ HVES	Horizontal Delay with Electronic Shutter	1			$\mu$ sec		Figure 10

Table 5 AC Timing Requirements for 30 MHz Operation

- Notes:
1. Integration time varies with shutter speed. It is to be noted that smear increases when integration time decreases below readout time (frame time). Photodiode dark current increases when integration time increases, while CCD dark current increases with readout time (frame time).
  2. Antiblooming function is off during photodiode to VCCD transfer.

## Frame Timing - Single Register Readout

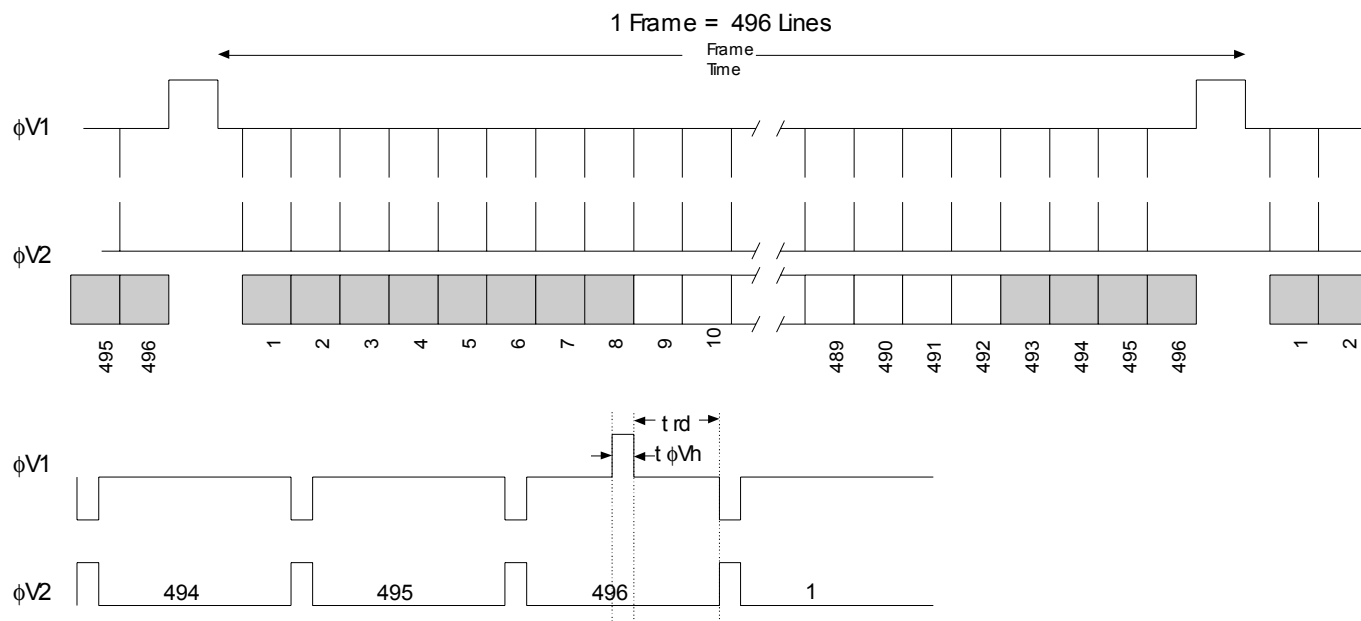


Figure 7 Frame Timing - Single Register Readout

Note : When no electronic shutter is used, the integration time is equal to the frame time.

## Line Timing - Single Register Readout

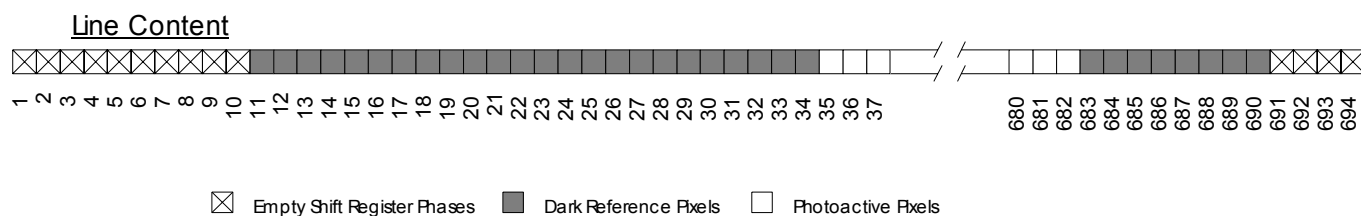
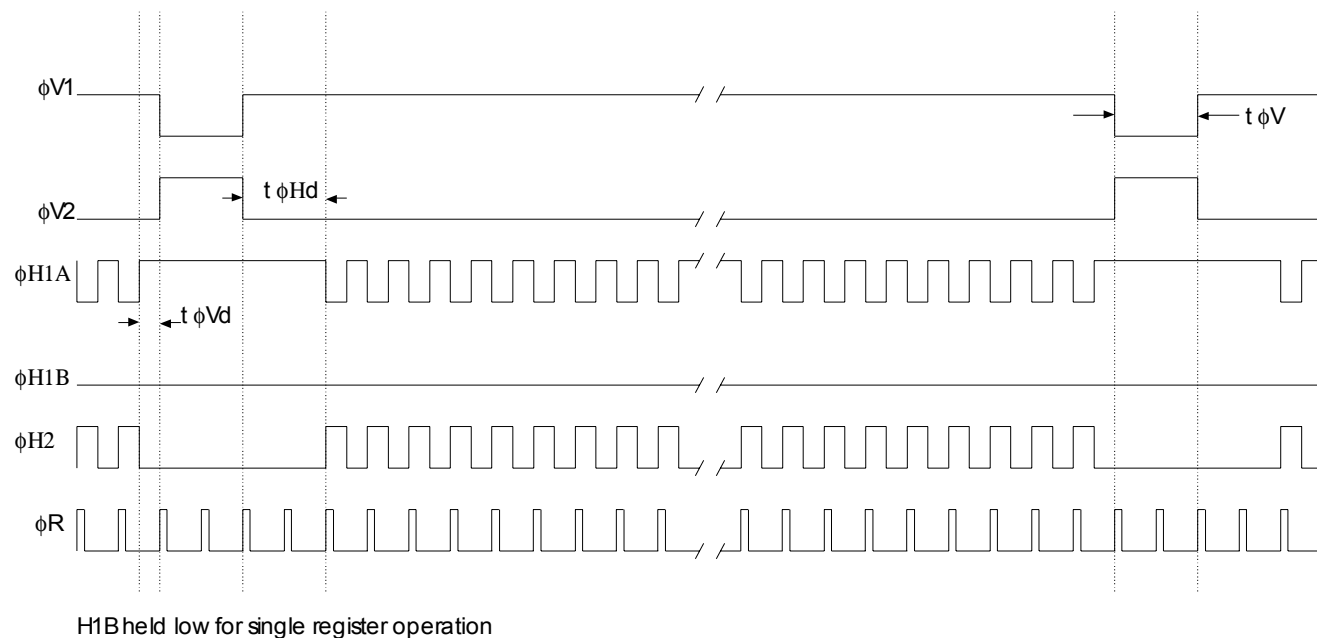


Figure 8 Line Timing - Single Register Output



## Pixel Timing - Single Register Readout

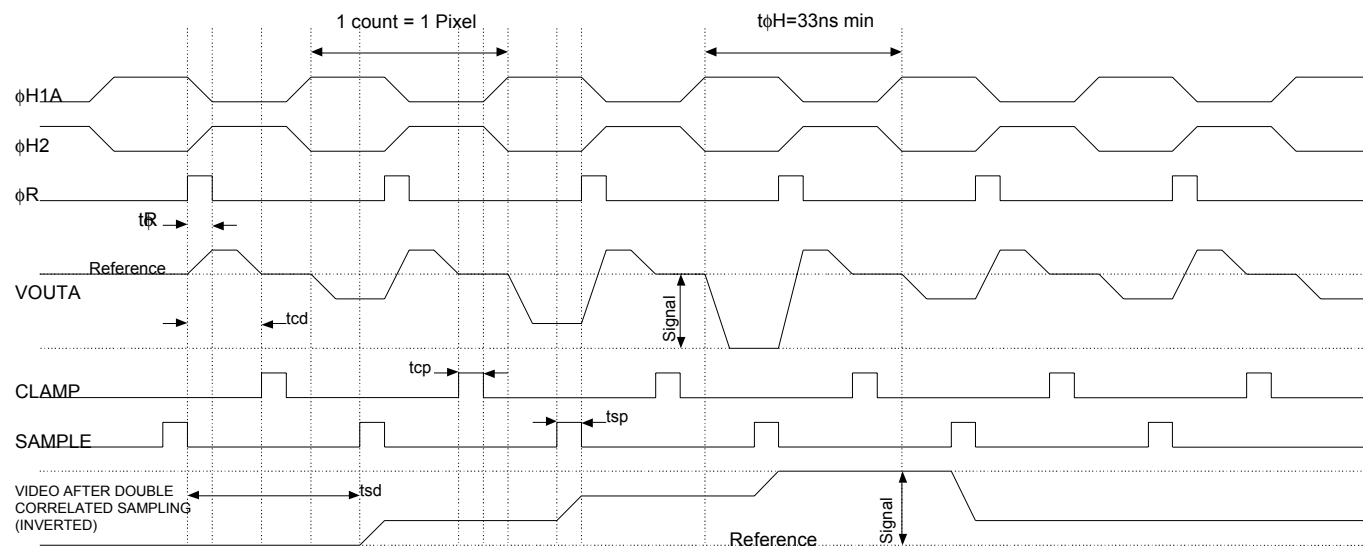
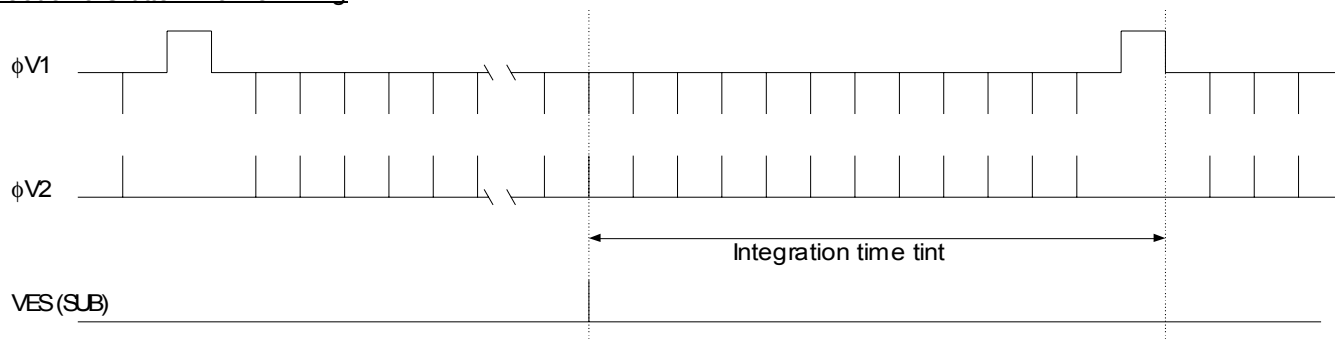


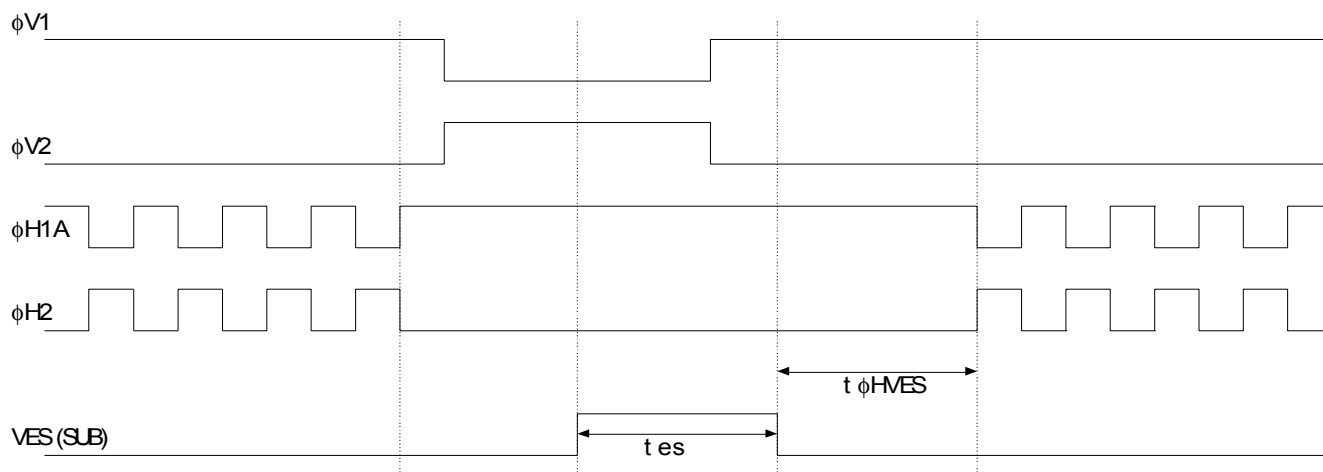
Figure 9 Pixel Timing Diagram - Single Register Readout

## Electronic Shutter Timing - Single Register Readout

### Electronic Shutter - Frame Timing



### Electronic Shutter - Placement



### Electronic Shutter - Operating Voltages

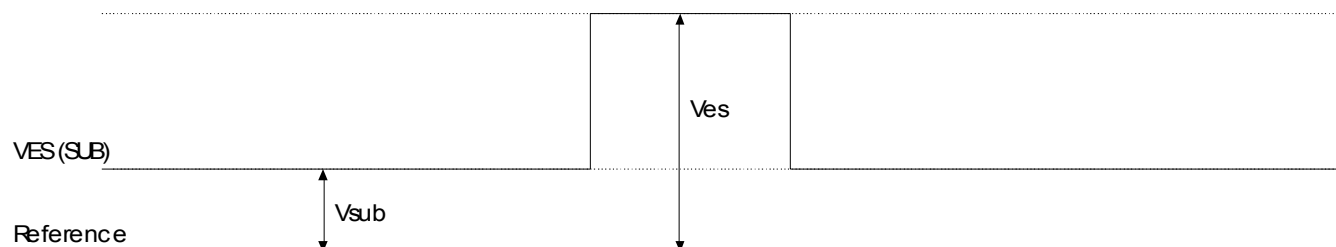


Figure 10 Electronic Shutter Timing Diagram - Single Register Readout

## Frame Timing - Dual Register Readout

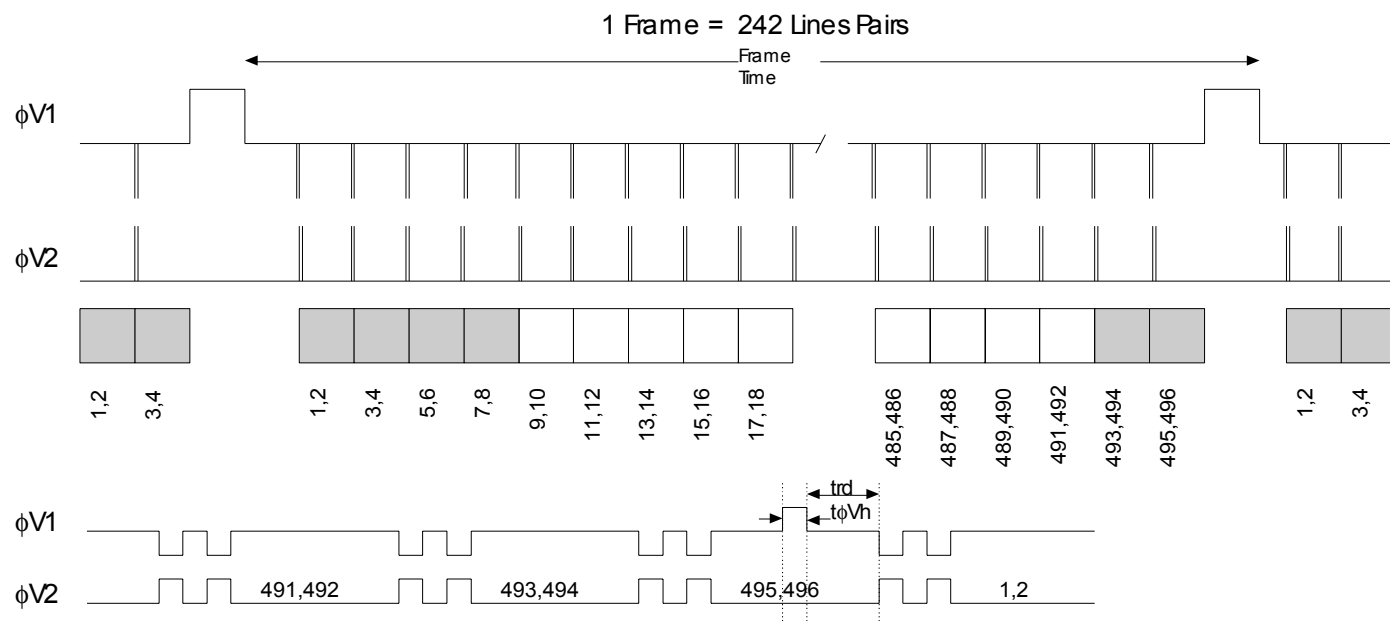


Figure 11 Frame Timing - Dual Register Readout

Note : When no electronic shutter is used, the integration time is equal to the frame time.

## Line Timing - Dual Register Readout

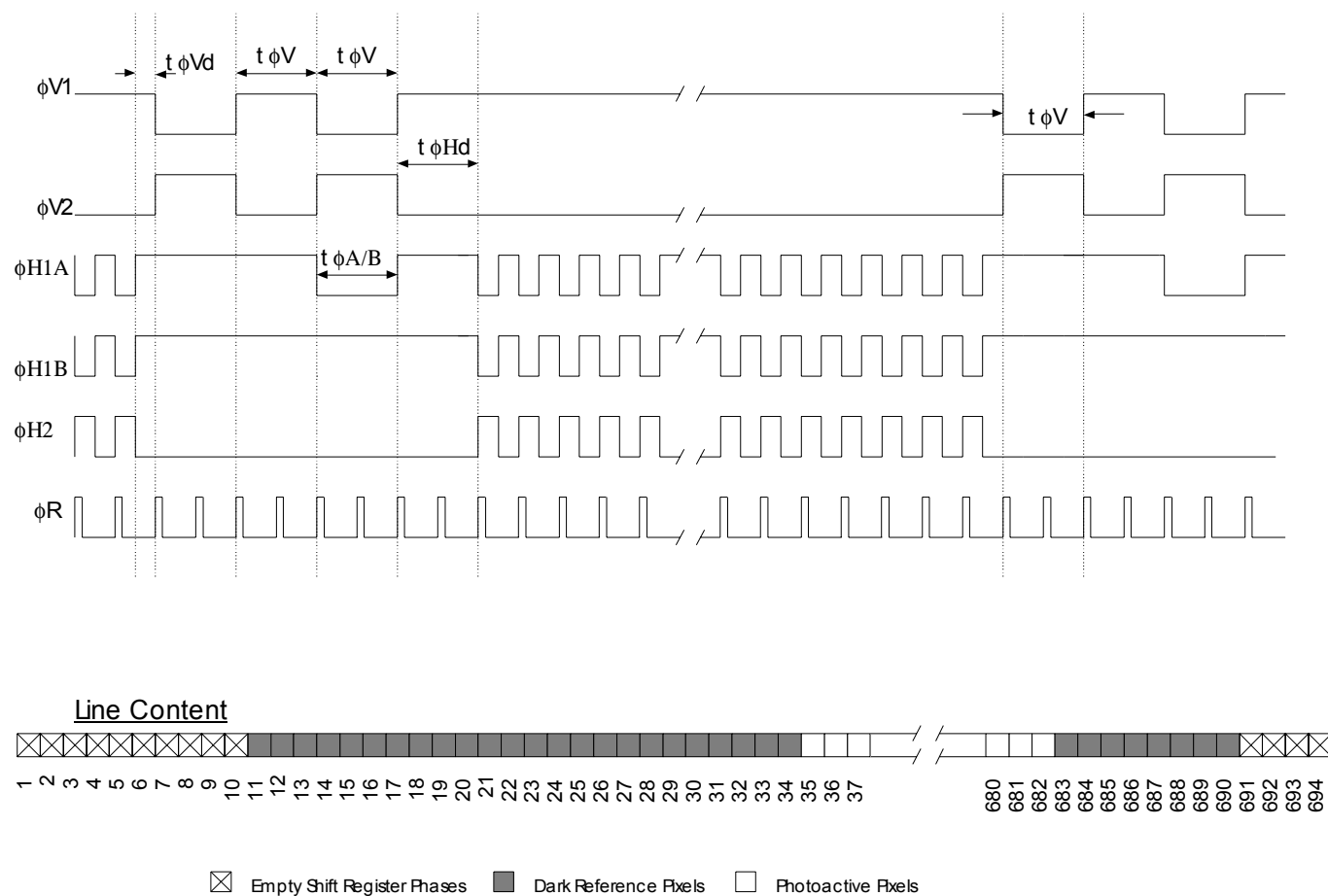


Figure 12 Line Timing - Dual Register Output

## Pixel Timing - Dual Register Readout

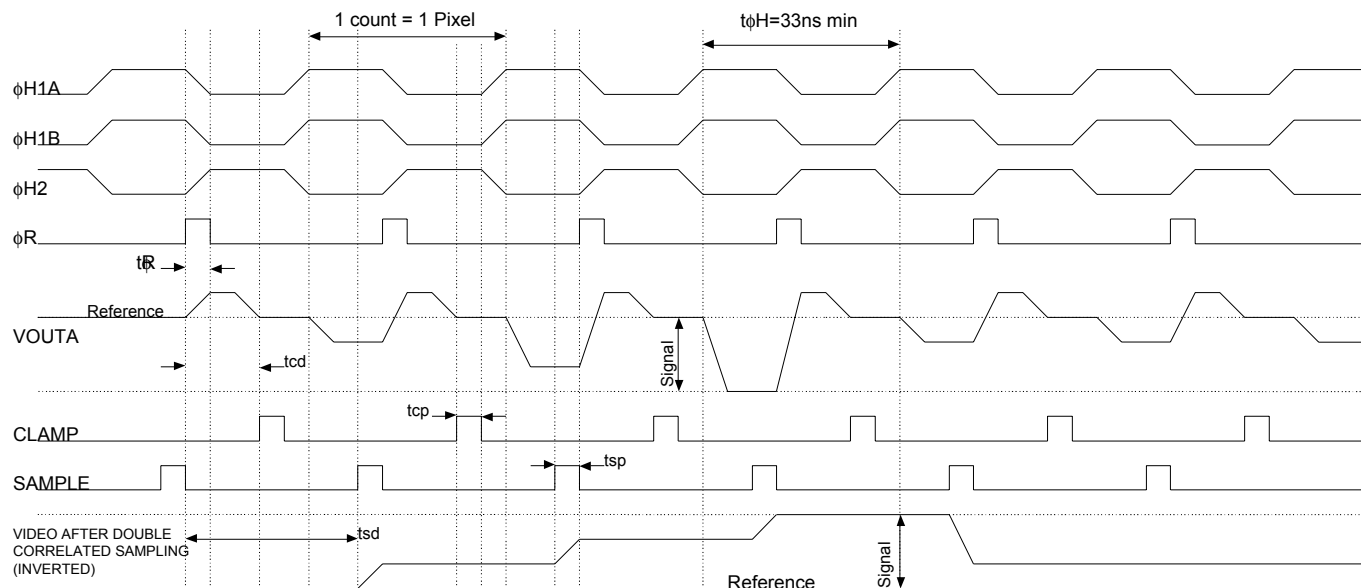


Figure 13 Pixel Timing Diagram - Dual Register Readout

## Fast Dump Timing – Removing Four Lines

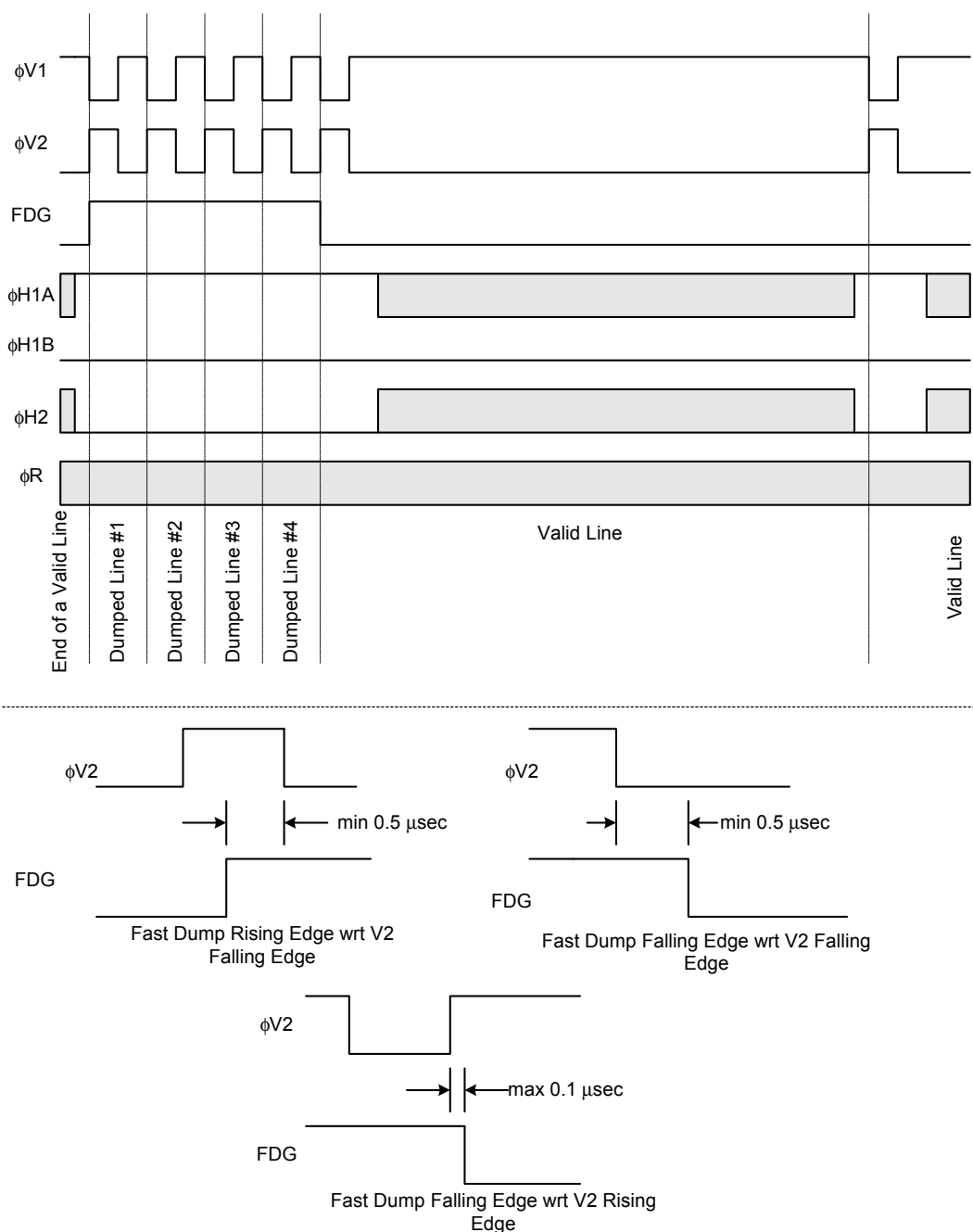


Figure 14 Fast Line Dump Timing - Removing Four Lines

# Binning – Two to One Line Binning

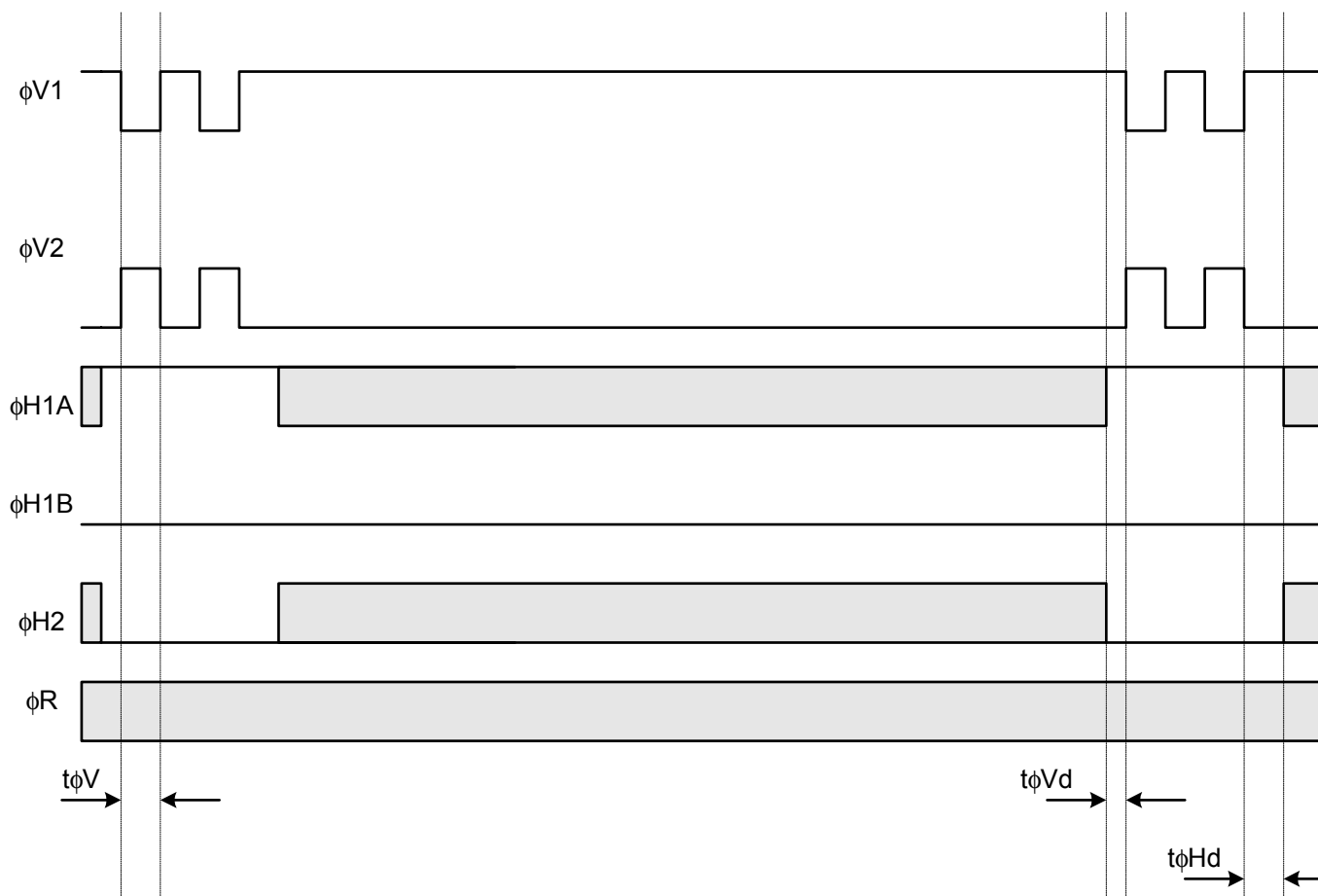


Figure 15 Binning - 2 to 1 Line Binning

# Timing – Sample Video Waveform

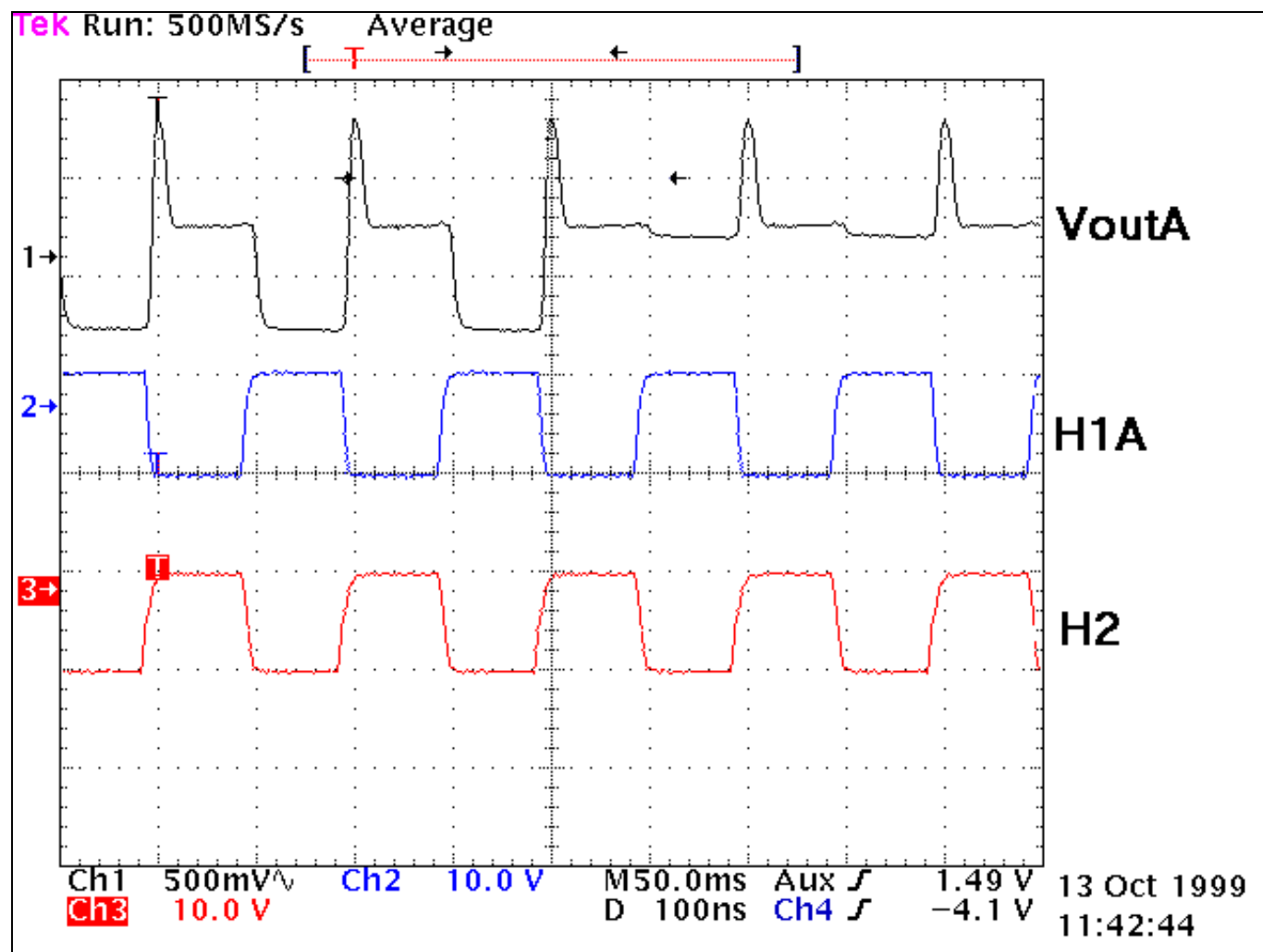


Figure 16 Sample Video Waveform at 5MHz



## Image Specifications

All the following values were derived using nominal operating conditions using the recommended timing. Unless otherwise stated, readout time = 40ms, integration time = 40ms and sensor temperature = 40°C. Correlated double sampling of the output is assumed and recommended. Many units are expressed in electrons, to convert to voltage, multiply by the amplifier sensitivity.

Defects are excluded from the following tests and the signal output is referenced to the dark pixels at the end of each line unless otherwise specified.

## Electro-Optical for KAI-0330DCM

SYMBOL	PARAMETER	MIN.	NOM.	MAX.	UNITS	NOTES
F F	Optical Fill Factor		55.0		%	
E <sub>sat</sub>	Saturation Exposure		0.046		μJ/cm <sup>2</sup>	1
QE <sub>r</sub>	Red Peak Quantum Efficiency $\lambda = 650\text{nm}$		22		%	2
QE <sub>g</sub>	Green Peak Quantum Efficiency $\lambda = 530\text{nm}$		28		%	2
QE <sub>b</sub>	Blue Peak Quantum Efficiency $\lambda = 450\text{nm}$		20		%	2
R <sub>gs</sub>	Green Photoresponse Shading		6		%	4
PRNU	Photoresponse Non-uniformity		5.0		p-p %	3
PRNL	Photoresponse Non-linearity		5.0		%	
	Amplifier Sensitivity		11.5		μV/e <sup>-</sup>	

Table 6 Electro-Optical Image Specifications KAI-0330DCM

- Notes:
1. For  $\lambda = 530\text{nm}$  wavelength, and  $V_{\text{sat}} = 350\text{mV}$ .
  2. Refer to typical values from Figure 17 Nominal KAI 0330DCM Spectral Response.
  3. Under uniform illumination with output signal equal to 280 mV.
  4. This is the global variation in chip output for green pixels across the entire chip.
  5. It is recommended to use low pass filter with  $\lambda_{\text{cut-off}}$  at  $\sim 680\text{nm}$  for high performance.

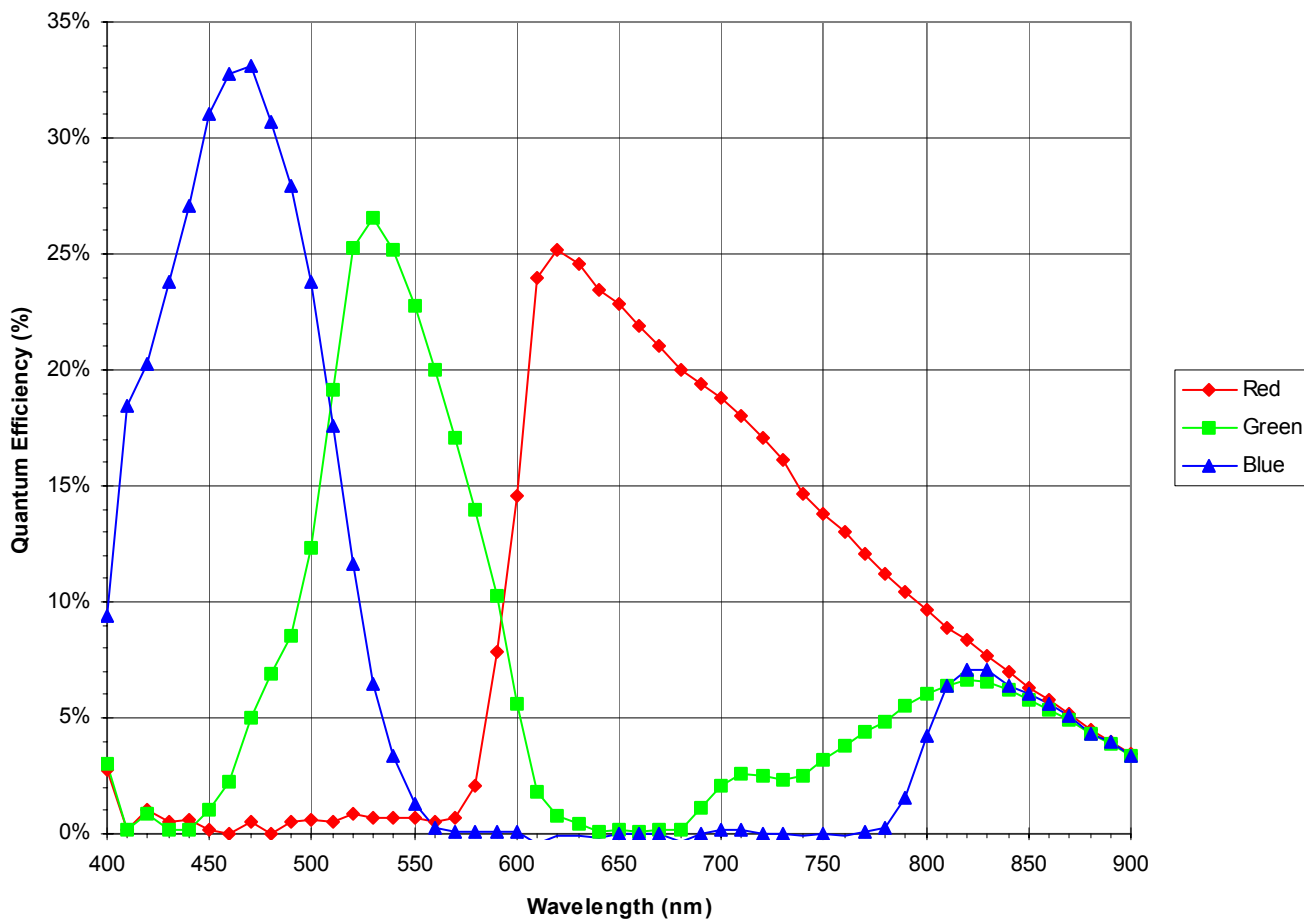


Figure 17 Nominal KAI 0330DCM Spectral Response

Electro-Optical for KAI-0330DM

SYMBOL	PARAMETER	MIN.	NOM.	MAX.	UNITS	NOTES
F F	Optical Fill Factor		55.0		%	
E <sub>sat</sub>	Saturation Exposure		0.037		μJ/cm <sup>2</sup>	1
QE	Peak Quantum Efficiency		36		%	2
PRNU	Photoresponse Non-uniformity		5.0		p-p %	3
PRNL	Photoresponse Non-linearity		5.0		%	

Table 7 Electro-Optical Image Specifications KAI-0330DM

- Notes:
- 1. For  $\lambda = 550\text{nm}$  wavelength, and  $V_{\text{sat}} = 350\text{mV}$ .
  - 2. Refer to typical values from Figure 18 Nominal KAI-0330DM Spectral Response
  - 3. Under uniform illumination with output signal equal to 280 mV.

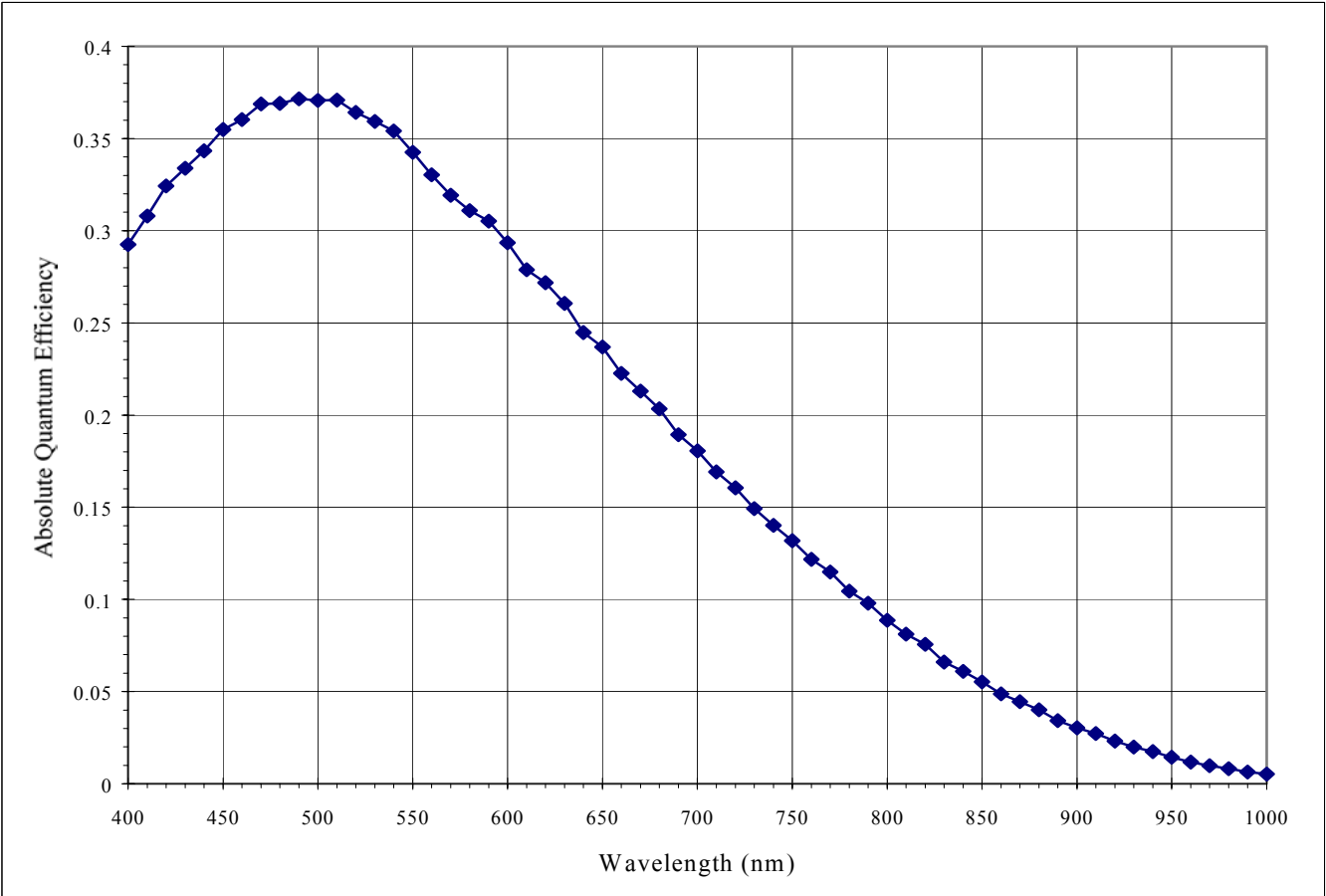


Figure 18 Nominal KAI-0330DM Spectral Response

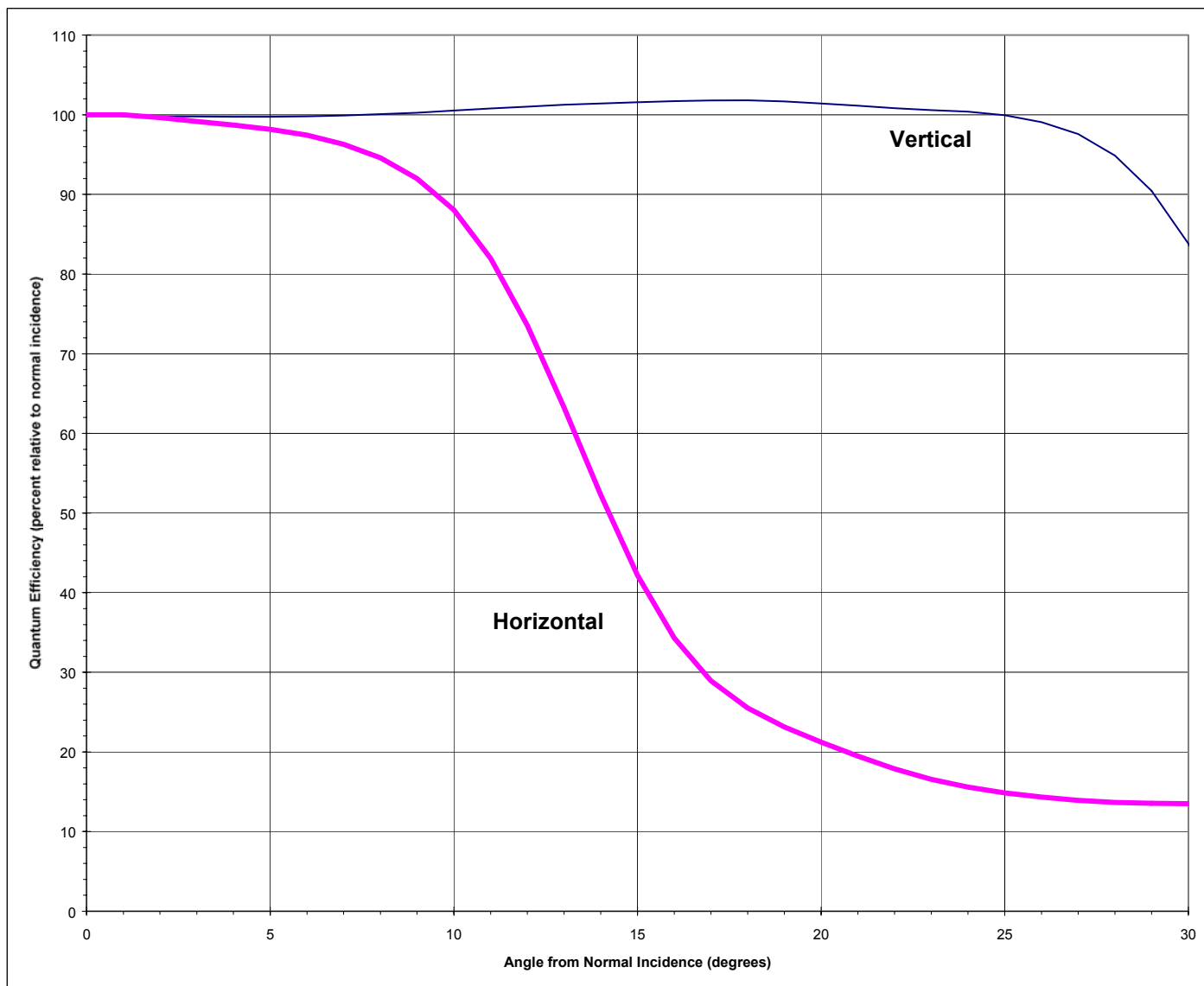


Figure 19 Angular Dependence on Quantum Efficiency

For the curve marked “Horizontal”, the incident light angle is varied in a plane parallel to the HCCD. For the curve marked “Vertical”, the incident light angle is varied in a plane parallel to the VCCD.

## CCD

SYMBOL	PARAMETER	MIN.	NOM.	MAX.	UNITS	NOTES
Vsat	Output Saturation Voltage		350		mV	1,2,8
I <sub>d</sub>	Dark Current			0.5	nA	
DCDT	Dark Current Doubling Temp	7	8	10	°C	
CTE	Charge Transfer Efficiency		0.99999			2,3
f <sub>H</sub>	Horizontal CCD Frequency			30	MHz	4
IL	Image Lag			100	e <sup>-</sup>	5
Xab	Blooming Margin		100			6,8
Smr	Vertical Smear		0.01		%	7

Table 8 CCD Image Specifications

- Notes:
1. Vsat is the green pixel mean value at saturation as measured at the output of the device with Xab=1. Vsat can be varied by adjusting Vsub.
  2. Measured at sensor output.
  3. With stray output load capacitance of C<sub>L</sub> = 10 pF between the output and AC ground.
  4. Using maximum CCD frequency and/or minimum CCD transfer times may compromise performance.
  5. This is the first field decay lag measured by strobe illuminating the device at (Hsat,Vsat), and by then measuring the subsequent frame's average pixel output in the dark.
  6. Xab represents the increase above the saturation-irradiance level (Hsat) that the device can be exposed to before blooming of the vertical shift register will occur. It should also be noted that Vout rises above Vsat for irradiance levels above Hsat, as shown in Figure 20.
  7. Measured under 10% (~ 100 lines) image height illumination with white light source and without electronic shutter operation and below Vsat.
  8. It should be noted that there is trade off between Xab and Vsat.

## Output Amplifier @ V<sub>DD</sub> = 15V, V<sub>SS</sub> = 0.0V

SYMBOL	PARAMETER	MIN.	NOM.	MAX.	UNITS	NOTES
V <sub>dc</sub>	Output DC Offset		7		V	1,2
P <sub>d</sub>	Power Dissipation	----	55	----	mW	3
f <sub>-3db</sub>	Output Amplifier Bandwidth		140		MHz	1,4
C <sub>L</sub>	Off-Chip Load			10	pF	

Table 9 Output Amplifier Image Specifications

- Notes:
1. Measured at sensor output with constant current load of I<sub>out</sub> = 5mA per output.
  2. Measured with V<sub>RD</sub> = 9v during the floating-diffusion reset interval, (φR high), at the sensor output terminals.
  3. Both channels.
  4. With stray output load capacitance of C<sub>L</sub> = 10 pF between the output and AC ground.

General

SYMBOL	PARAMETER	MIN.	NOM.	MAX.	UNITS	NOTES
Vn - total	Total Sensor Noise		0.5		mV, rms	1
DR	Dynamic Range			58	dB	2

Table 10 General Image Specifications

- Notes:
- 1. Includes amplifier noise and dark current shot noise at data rates of 10MHz. The number is based on the full bandwidth of the amplifier. It can be reduced when a low pass filter is used.
  - 2. Uses  $20\text{LOG}(V_{\text{sat}}/V_n - \text{total})$  where  $V_{\text{sat}}$  refers to the output saturation signal.

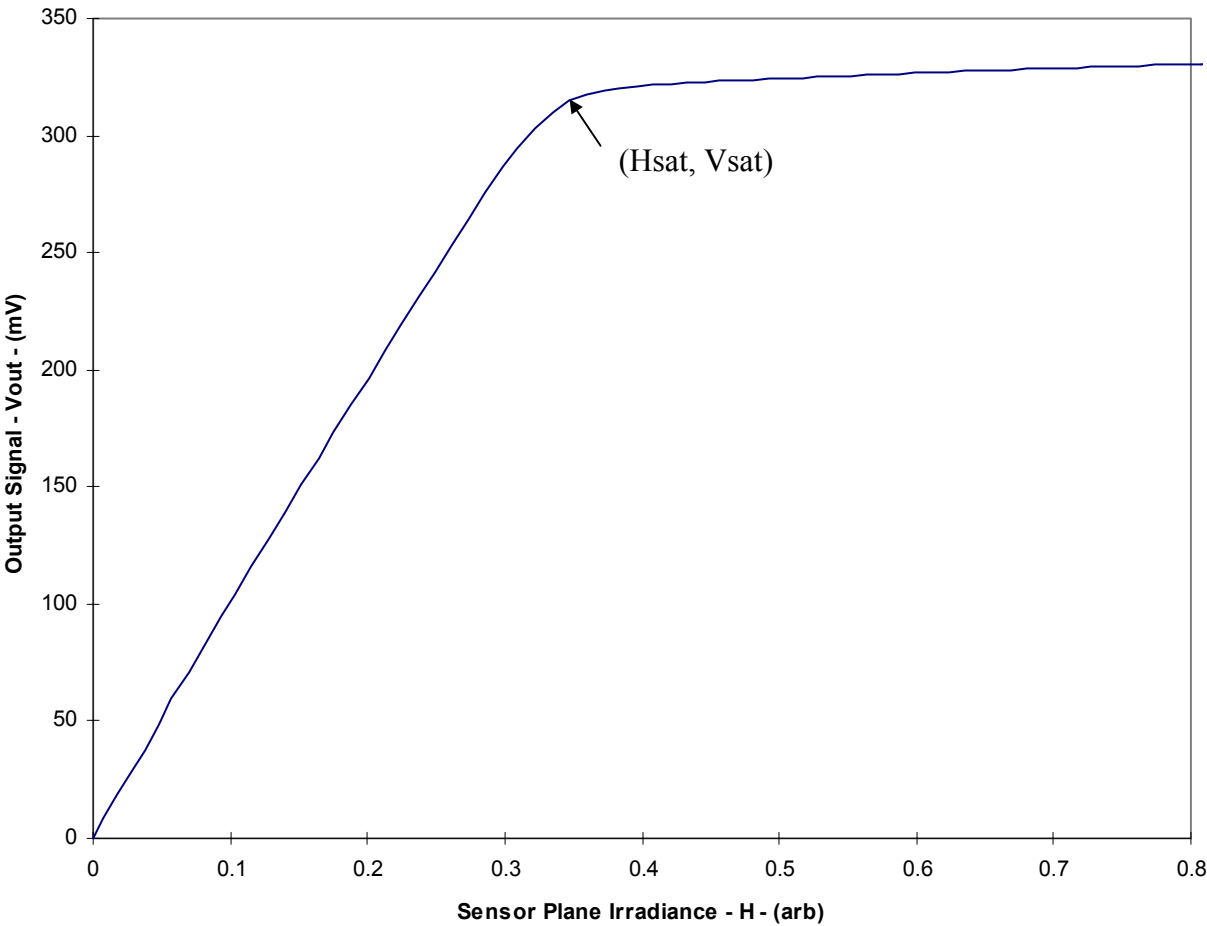


Figure 20 Typical KAI-0330D Series Photoresponse

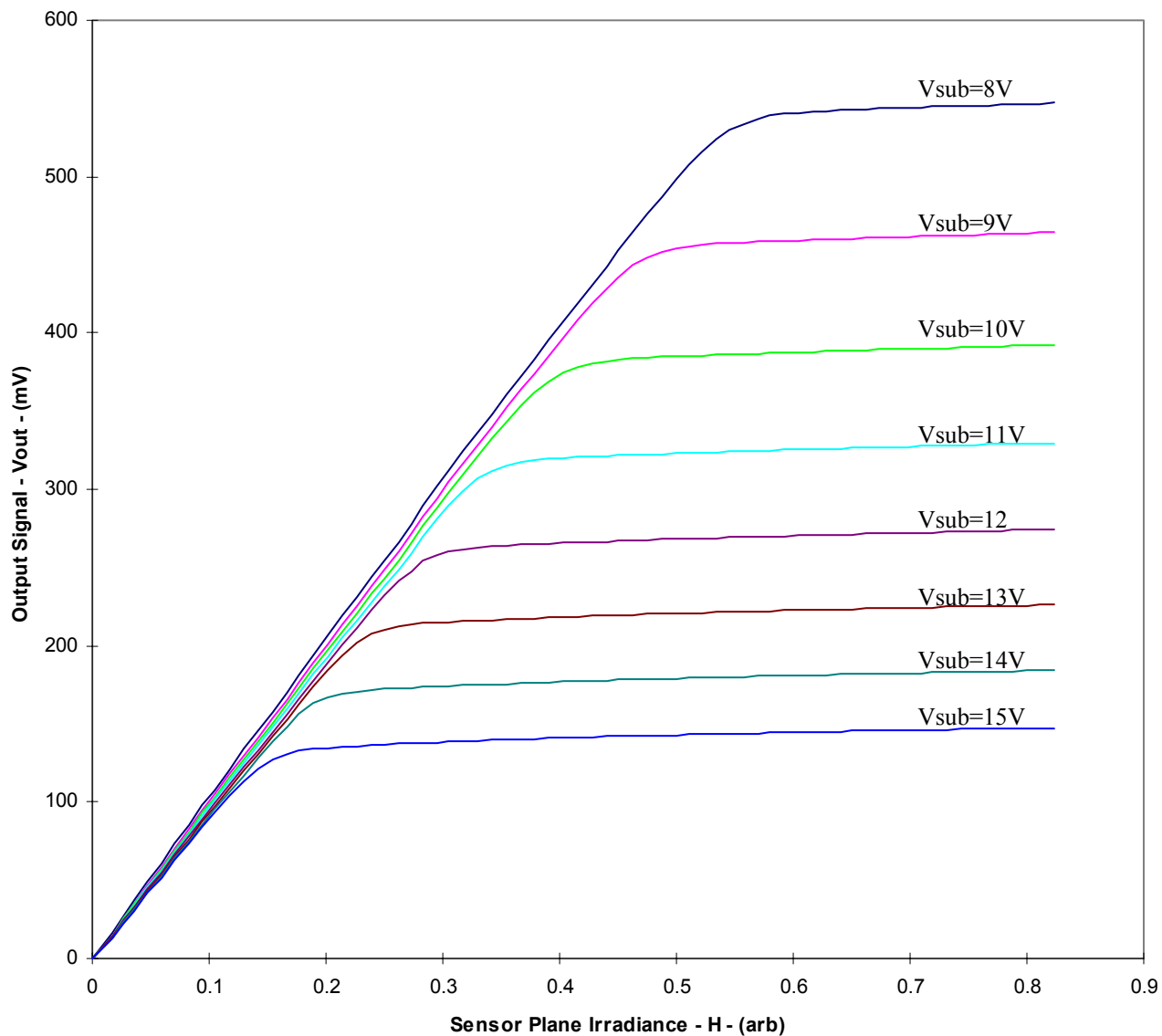


Figure 21 Example of Vsat versus Vsub

As Vsub is decreased, Vsat increases and anti-blooming protection decreases.

As Vsub is increased, Vsat decreases and anti-blooming protection increases.

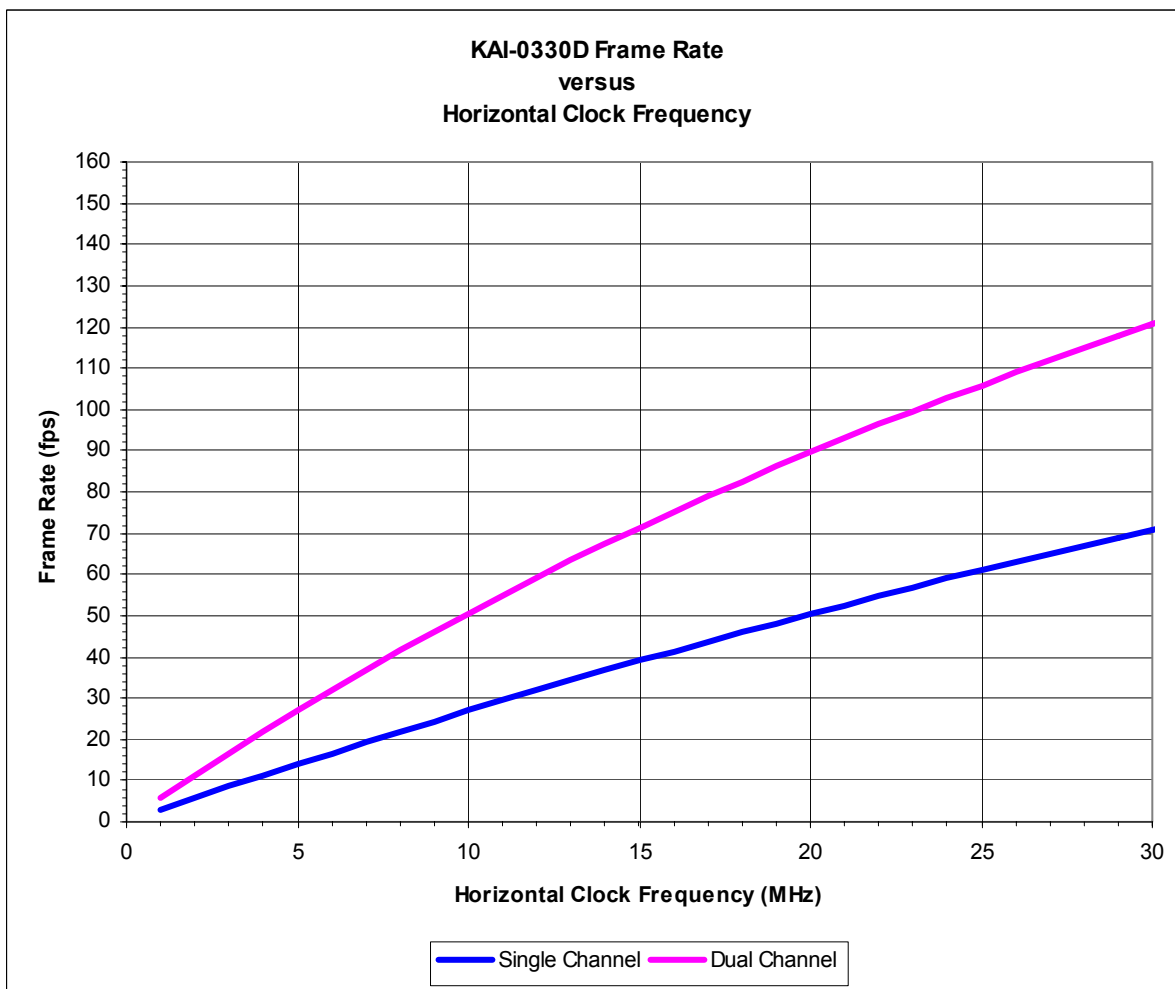


Figure 22 Frame Rate versus Horizontal Clock Frequency



## Defect Classification

All values derived under nominal operating conditions at 40°C operating temperature.

Point Defects		Cluster Defects	Column Defects Total
Major	Minor		
$\leq 2$	$\leq 15$	0	0

Major Defective Pixel	A pixel whose signal deviates by more than 25 mV from the mean value of all active pixels under dark field condition or by more than 15% from the mean value of all active pixels under uniform illumination at 80% of saturation.
Minor Defective Pixel	A pixel whose signal deviates by more than 6mV from the mean value of all active pixels under dark field condition.
Point Defect	An isolated defective pixel.
Cluster Defect	A group of 2 to 4 contiguous major defective pixels.
Column Defect	A group of more than 4 contiguous major defective pixels along a single column or row.

Note : No row defects are allowed.

### Test Conditions

Junction Temperature	$(T_j) = 40^{\circ}\text{C}$
Integration Time	$(t_{\text{int}}) = 40\text{msec}$
Readout Rate	$(t_{\text{readout}}) = 40\text{msec}$

## Climatic Requirements

ITEM	DESCRIPTION	MIN.	MAX.	UNITS	CONDITIONS	NOTES
Operation to Specification	Temperature	-25	+40	°C	@ 10% $\pm$ 5% RH	1, 2
	Humidity	10 $\pm$ 5	86 $\pm$ 5	%RH	@ 36 $\pm$ 2°C Temp.	1, 2
Operation Without Damage	Temperature	-50	+70	°C	@ 10% $\pm$ 5% RH	2, 3
Storage	Temperature	-55	+70	°C	@ 10% $\pm$ 5%RH	2, 4
	Humidity	-----	95 $\pm$ 5	%RH	@ 49 $\pm$ 2°C Temp.	2, 4

Table 11 Climatic Requirements

- Notes:
1. The image sensor shall meet the specifications of this document while operating at these conditions.
  2. The tolerance on all relative humidity values is provided due to limitations in measurement instrument accuracy.
  3. The image sensor shall continue to function but not necessarily meet the specifications of this document while operating at the specified conditions.
  4. The image sensor shall meet the specifications of this document after storage for 15 days at the specified conditions.

## Quality Assurance and Reliability

- 4.2.1 Quality Strategy: All devices will conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and inspection at key points of the production process. Typical specification limits are not guaranteed but provided as a design target. For further information refer to ISS application Note MTD/PS-0292, Quality and Reliability.
- 4.2.2 Replacement: All devices are warranted against failures in accordance with the Terms of Sale. This does not include failure due to mechanical and electrical causes defined as the liability of the customer below.
- 4.2.3 Liability of the Supplier: A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer.
- 4.2.4 Liability of the Customer: Damage from mechanical (scratches or breakage), electrostatic discharge (ESD) damage, or other electrical misuse of the device beyond the stated absolute maximum ratings, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.
- 4.2.5 Cleanliness: Devices are shipped free of mobile contamination inside the package cavity. Immovable particles and scratches that are within the imager pixel area and the corresponding cover glass region directly above the pixel sites are also not allowed. The cover glass is highly susceptible to particles and other contamination. Touching the cover glass must be avoided. See ISS Application Note MTD/PS-0237, Cover Glass Cleaning for Image Sensors, for further information.
- 4.2.6 ESD Precautions: Devices are shipped in static-safe containers and should only be handled at static-safe workstations. See ISS Application Note MTD/PS-0224, Electrostatic Discharge Control, for handling recommendations.
- 4.2.7 Reliability: Information concerning the quality assurance and reliability testing procedures and results are available from the Image Sensor Solutions and can be supplied upon request. For further information refer to ISS Application Note MTD/PS-0292 Quality and Reliability.
- 4.2.8 Test Data Retention: Image sensors shall have an identifying number traceable to a test file. Test data shall be kept for a period of 2 years after date of delivery.
- 4.2.9 Mechanical: The device assembly drawing is provided as a reference. The device will conform to the published package tolerances.

## Ordering Information

### Available Part Configurations

Type	Description	Glass Configuration
KAI-0330D	Monochrome	Taped On Glass
KAI-0330DM	Monochrome with microlens	Sealed Clear Glass
KAI-0330DCM	Color with microlens	Sealed Clear Glass

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E-mail: [imagers@kodak.com](mailto:imagers@kodak.com)

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### **WARNING: LIFE SUPPORT APPLICATIONS POLICY**

Kodak image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company. Product warranty is limited to replacement of defective components and does not cover injury to persons or property or other consequential damages.

**Revision Changes**

No.	Description of Revision
1	<ul style="list-style-type: none"><li>Initial release of document</li></ul>
2.0	<ul style="list-style-type: none"><li>Correction to Table 1 Package Pin Assignments. V2E and V2O were incorrectly labeled. Pins were labeled: Pin 17 V2O Vertical CCD Clock – Phase 2, odd field Pin 18 V2E Vertical CCD Clock – Phase 2, even field Correct pin assignments: Pin 17 V2E Vertical CCD Clock – Phase 2, even field Pin 18 V2O Vertical CCD Clock – Phase 2, odd field</li><li>Corrected t<math>\phi</math>H in: Figure 9: Pixel Timing Diagram - Single Register Readout and Figure 13: Pixel Timing Diagram - Dual Register Readout Incorrect t<math>\phi</math>H was 50 ns (20 MHz) Correct t<math>\phi</math>H value is 33 ns (30 MHz)</li></ul>