

Features

- Performance of Greater than 100MHz (200 DDR)
- Interfaces to JEDEC Standard DDR SDRAMs
- Supports DDR SDRAM Data Widths of 16, 32 and 64 Bits
- Supports up to 8 External Memory Banks
- Programmable Burst Lengths of 2, 4, or 8
- Programmable CAS Latency of 1.5, 2.0, 2.5 or 3.0
- Byte-level Writing Supported
- Increased Throughput Using Command Pipelining and Bank Management
- Supports Power-down and Self Refresh Modes
- Automatic Initialization
- Automatic Refresh During Nomal and Power-down Modes
- Timing and Settings Parameters Implemented as Programmable Registers

- Bus Interfaces to PCI Target, PowerPC and AMBA (AHB) Buses Available
- Complete Synchronous Implementation

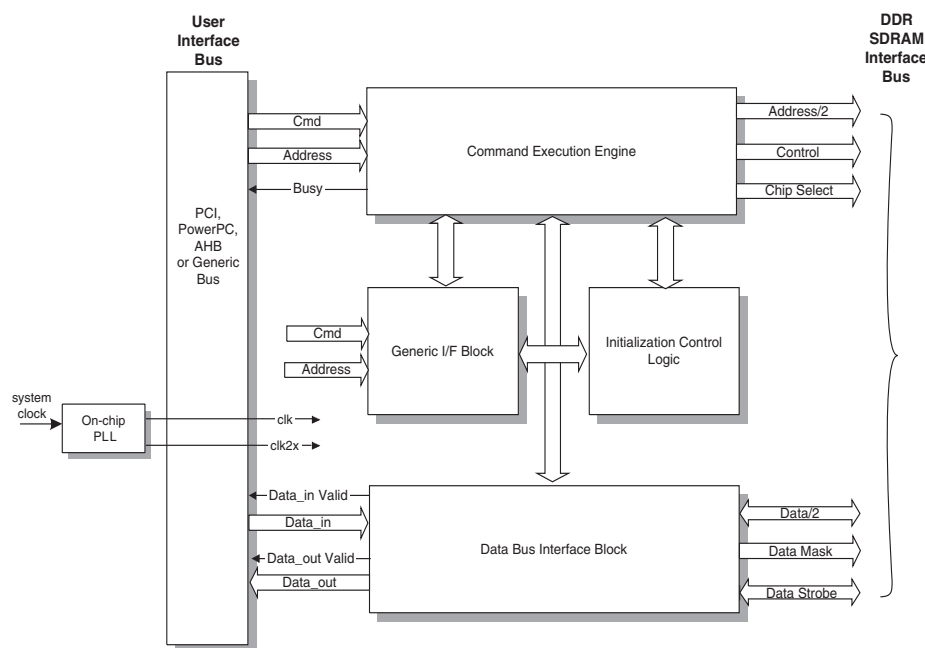
General Description

DDR (Double Data Rate) SDRAM was introduced as a replacement for SDRAM memory running at bus speeds over 75MHz. DDR SDRAM is similar in function to the regular SDRAM but doubles the bandwidth of the memory by transferring data twice per cycle on both edges of the clock signal, implementing burst mode data transfer.

The DDR SDRAM Controller is a parameterized core giving user the flexibility for modifying the data widths, burst transfer rates, and CAS latency settings of the design. In addition, the DDR core supports intelligent bank management, which is done by maintaining a database of "all banks activated" and the "rows activated" in each bank. With this information, the DDR SDRAM Controller decides if an active or pre-charge command is needed. This effectively reduces the latency of read/write commands issued to the DDR SDRAM.

Block Diagram

Figure 1. DDR SDRAM Controller Block Diagram



Since the DDR SDRAM Controller takes care of activating/pre-charging the banks, user only needs to issue simple read/write commands.

Functional Description

The DDR SDRAM Controller block diagram, illustrated in Figure 1, consists of four functional modules: the Generic Interface block, Command Execution Engine, Data Bus Interface block and the Initialization Control Logic.

Generic Interface Block

The Generic interface block contains the configuration registers: CFG0, CFG1, CFG2, and CFG3. These registers are updated when a `Load_CFG` command is received from the user. These registers contain the programmable DDR SDRAM timing parameters and can be changed by the user to suit the DDR SDRAM memory timings being used thus giving the flexibility to use any DDR SDRAM memory.

Command Execution Engine

The command execution engine is the main component of the DDR SDRAM controller. This block accepts commands from the “User Interface Bus” and keeps a record of bank open/close status. It accepts up to two commands at any time (pipelined). Once a command is received, it decides whether to open the bank, close the bank or directly execute the READ/WRITE commands and apply the appropriate DDR SDRAM commands to the DDR SDRAM Memory. Table 1 shows the different user interface commands supported.

To maintain throughput of data this block uses two state machines to process READ/WRITE commands received from the user interface. When the commands are continuously received, one state machine works in master mode and the other state machine works in slave mode. The state machine that receives the command first becomes the master and the other becomes the slave on receiving the second command. Once the master state machine completes the command execution, the slave state machine execution is enabled.

This block also maintains an auto refresh counter, which refreshes the DDR SDRAM memory at the predetermined programmed intervals even during power down.

Table 1. DDR SDRAM Controller Generic I/F Commands

Command Name	Cmd[2:0]	Description
NOP	000	No operation.
READ	001	Initiate a burst read.
WRITE	010	Initiate a burst write.
LOAD CONFIG REG (Load_CFG)	011	Load controller configuration values. The controller uses this command to load the CFG0/CFG1/CFG2/CFG3 registers.
LOAD MODE REG (Load_MR)	100	Load the Mode and Extended Mode registers.
POWER_DOWN	101	Put the DDR SDRAM into power-down or wake up from POWER DOWN.
SELF_REFRESH	110	To enter into self refresh mode or get out of self refresh mode

Data Bus Interface

The Data Bus Interface block controls the data flow between the User Interface bus and DDR SDRAM Memory interface bus. The data received from the Memory during a read operation is converted from a double data rate to single data rate; similarly the data to be written into the memory is converted from a single data rate to a double data rate.

During a write operation, depending on the data mask signals, the data is written or masked by the DDR SDRAM-memory.

Initialization Control Logic

When the User sets the initialization bit (Bit 7 in the configuration register CFG0) using the LOAD_CFG command, this block starts initialization as specified in the DDR SDRAM specification. The DDR controller initialization can only be performed after the system power is applied and the clock is running for at least 200 μ s. An initialization is required before any read/write command is issued to the DDR SDRAM memory.

User Interface Bus

In order to connect this controller to different bus standards Lattice provides the following “Bus Interface blocks”:

1. PCI Target Interface
2. Power PC Interface
3. AMBA-AHB Interface
4. Generic Bus Interface

The main function of these “Bus Interface blocks” is to trap all transactions on the respective bus addressed to the DDR SDRAM and translate them into Generic Interface commands.

Since all the buses have burst addressing which is greater than the burst supported by the DDR SDRAM memory, all the interfaces have an address generator block which generates the appropriate address depending on the requested burst.

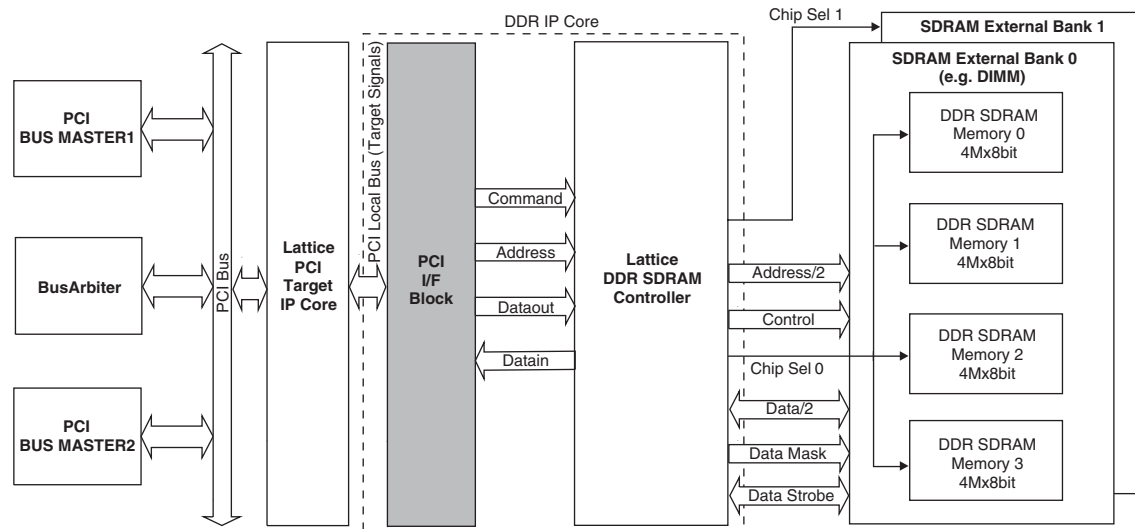
In all the interfaces the data going in and out of the bus is stored in a sync FIFO block, which is used as a storage buffer for read/write commands. During a read from the DDR SDRAM the data is sent to FIFO and is read by Bus Interface block. During a write the data is first written into the FIFO before actually writing this data into the DDR SDRAM.

PCI Target Interface Block

The PCI Target Interface Block is used to interface the Lattice DDR Controller IP core with a Lattice PCI Target core, which simplifies the usage in a PCI Bus environment. Figure 2 shows the system with a PCI Target core.

The following are the features of the PCI Target interface block:

- Parameterized data path width of 32- or 64-bit on the PCI Local Bus and the User interface bus of DDR controller.
- Read/Write of configurable registers through PCI memory space.
- Read/Write to DDR through PCI memory space.
- Supports Power down and self refresh commands for low power applications.
- Programmable burst length.
- Programmable FIFO Depth
- Automatic wake up from power down/self refresh by a Read/Write command.

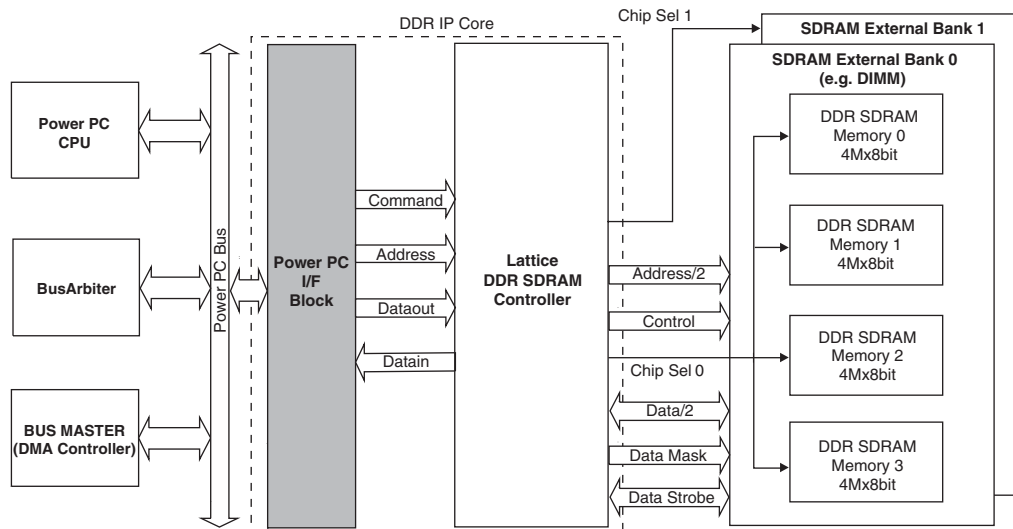
Figure 2. Typical PCI System with Lattice DDR SDRAM Controller

PowerPC BUS Interface Block

The Power PC Bus Interface block is used to interface with the Lattice DDR SDRAM Controller IP Core with the Power PC 60x Bus. This interface allows easy usage of the Lattice DDR SDRAM Controller in a Power PC Bus environment. Figure 3 shows the system with a Power PC Bus interface block.

The following are the features of the Power PC Bus interface block

- Supports PowerPC 601,603, 604 and processors supporting 60x bus.
- Parameterized data path widths of 32 or 64 bits.
- Supports both burst and single-beat data transfers (DDR Burst Length is 4).
- Programmable FIFO Depth
- Supports pipeline of two requests (write).
- Supports Address retry
- Supports separate address and data bus tenure.

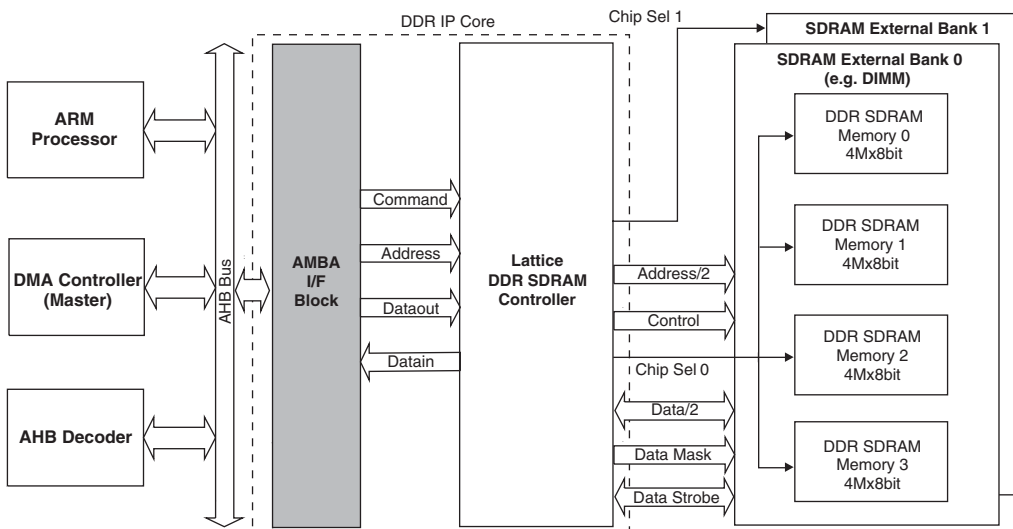
Figure 3. Typical PowerPC System with Lattice DDR Controller

AHB Bus Interface Block

The AHB Bus Interface Block interfaces between AMBA Bus and Lattice DDR SDRAM Controller IP Core. This interface allows easy usage of the Lattice DDR SDRAM Controller on an ARM AHB bus environment. Figure 4 shows the system with an AHB Bus interface block.

The following are the features of the AHB Bus interface block

- Parameterized data path widths of 32, 64 and 128 bits on the AMBA Bus and the User Interface Bus.
- Supports INCR4/INCR8/INCR16/WRAP4/WRAP8/WRAP16/INCR Bursts (DDR side Burst Length is 4)
- Supports Byte/Half word/Word/Double Word transfers (with 64bit AHB-Bus)
- Programmable FIFO Depth

Figure 4. Typical AHB System with Lattice DDR Controller IP Cores

Parameter Descriptions

The static parameters are set before the design is synthesized to a gate-level netlist. The dynamic parameters can also be set in this way, or they can be changed after the core is programmed onto a device by writing the values into the Configuration Registers. The user should consult the DDR SDRAM specifications before choosing the dynamic parameters, which are dependent on the DDR SDRAM device being used.

Table 2. Static DDR Core Parameters

Parameter	Description	Default Value
DSIZE	Defines the bus width for the data input/output port.	32 bits
RSIZE	Defines row address width.	12 bits
CSIZE	Defines column width.	11 bits
BSIZE	Defines bank width for internal chip banks. This version of the DDR SDRAM Controller is designed to work with memory chips containing four internal banks (sometimes called a quad memory array). The default value for BSIZE cannot be changed in this version of the core.	2 bits
RANK_SIZE	Defines the number of external Banks (RANKS). NOTE: an external bank is a memory chip or group of chips (such as on a DIMM) that can be accessed using the same chip select signal. RANK_SIZE = 0 (External Banks = 1) RANK_SIZE = 1 (External Banks = 2) RANK_SIZE = 2 (External Banks = 4) RANK_SIZE = 3 (External Banks = 8)	0
Interface Type	The following Bus Interface Blocks are available for connecting this controller to different bus standards: PCI Target Interface, PowerPC Interface, AMBA_AHB Interface, Generic Bus Interface.	Generic

Table 3. Dynamic DDR Core Parameters

Parameter	Description	Default Value
INIT	Initialize DDR. Initializes the DDR SDRAM when bit is set. Set by command in register.	0
TRCD Delay	RAS to CAS Delay. This is the delay from /RAS to /CAS in number of clock cycles and is calculated using this formula $\text{INT}(t_{\text{RCD(MIN)}} / t_{\text{CK}})^*$.	2
TRRD Delay	Row ACTIVE to Row ACTIVE Delay. This delay is in clock cycles and is calculated using this formula $\text{INT}(t_{\text{RRD(MIN)}} / t_{\text{CK}})^*$.	2
TRFC Delay	AUTO REFRESH command period. This delay is in clock cycles and is calculated using this formula $\text{INT}(t_{\text{RFC(MIN)}} / t_{\text{CK}})^*$.	9
TRP Delay	PRECHARGE command period. This is calculated by the formula $\text{INT}(t_{\text{RP(MIN)}} / t_{\text{CK}})^*$.	2
TMRD Delay	LOAD MODE REGISTER command cycle time. This is calculated by the formula $\text{INT}(t_{\text{MRD(MIN)}} / t_{\text{CK}})^*$.	2
TWR Delay	Write recovery time. This is calculated by the formula $\text{INT}(t_{\text{WR(MIN)}} / t_{\text{CK}})^*$.	2
TRAS Delay	ACTIVE to PRECHARGE delay. Defines the delay between the ACTIVE and PRECHARGE commands (maximum value = 15 clock cycles).	6
TWTR Delay	WRITE to READ command delay. Defines internal write to read command delay (maximum value = 7 clock cycles).	1
TRC Delay	ACTIVE to ACTIVE /AUTOREFRESH command delay. Defines ACTIVE to ACTIVE /auto refresh command period delay (maximum value = 15 clock cycles).	8
CAS Latency	CAS Latency. Delay in clock cycles between the registration of a READ command and the first bit of output data. Valid values are 1.5, 2.0, 2.5 and 3.0.	2 (2.0 clock cycles)
Burst Length	Burst Length. This number determines the maximum number of columns that can be accessed for a given READ/WRITE and is equal to Burst Length programmed in the Mode register. Valid values are 2, 4 and 8.	2

Table 3. Dynamic DDR Core Parameters (Continued)

Parameter	Description	Default Value
Burst Type	Burst Type. Specifies whether an interleaved or sequential burst is required. 0 represents a sequential and 1 represents an interleaved burst type.	0
DSTRENGTH	Drive Strength. Defines bit 1 in the Extended mode register. 0 represents normal drive strength, 1 represents a reduced drive strength (required by some memory devices).	0
QFCFUNC	Defines bit 2 of the extended mode register which enables or disables the QFC function (required by some memory devices).	0
Refresh Period	Refresh Period. Defines maximum time period between AUTOREFRESH commands. Calculate as follows: $\text{INT}(t_{\text{REF}} / t_{\text{CK}})^*$.	2228

***Notes:** t_{CK} = Clock cycle time $t_{\text{RCD(MIN)}}$ = ACTIVE to READ or WRITE delay $t_{\text{RRD(MIN)}}$ = ACTIVE (bank A) to ACTIVE (bank B) command period $t_{\text{RFC(MIN)}}$ = AUTOREFRESH command period (min.) $t_{\text{RP(MIN)}}$ = PRECHARGE command period $t_{\text{MRD(MIN)}}$ = LOAD_MR command cycle time $t_{\text{WR(MIN)}}$ = Write recovery time t_{REF} = AUTOREFRESH command interval (max.)

Signal Descriptions

The following tables show the different interface signals for the DDR SDRAM controller. The DDR SDRAM Interface signals are the same for all core configurations.

Table 4. DDR SDRAM Interface Bus Signals

Signal Name	Direction	Active State	Description
ddr_clk	Output	N/A	DDR SDRAM Clock, derived from the system clock.
ddr_clk_n	Output	N/A	Inverted DDR SDRAM Clock, derived from the system clock.
ddr_cke	Output	High	Clock enable.
ddr_cs_n [(2 ^{RANK_SIZE}) - 1:0]	Output	N/A	Active Low Chip Select. Selects and deselects the DDR SDRAM external bank.
ddr_we_n	Output	Low	Write Enable. Defines the part of the command being entered.
ddr_cas_n	Output	Low	Column Select. Defines the part of the command being entered.
ddr_ras_n	Output	Low	Row select. Defines the part of the command being entered.
ddr_ad[RSIZE-1:0]	Output	N/A	Row or column address lines depending whether the /RAS or /CAS is active.
ddr_ba[BSIZE-1:0]	Output	N/A	Bank Address Select.
ddr_dq[DSIZE/2-1:0]	In/Out	N/A	Bi-directional Data Bus.
ddr_dqm[DSIZE/16-1:0]	Output	N/A	Data mask signals used to mask the byte lanes for byte level write control.
ddr_dqs[DSIZE/16-1:0]	In/Out	N/A	Data strobe signals used by memory to latch the write data.

Table 5. User Generic Interface Bus interface Signals

Signal Name	Direction	Active State	Description
clk	Input	N/A	System clock.
reset_n	Input	Low	System reset.
cmd[2:0]	Input	N/A	Command for controller.
datain[DSIZE-1:0]	Input	N/A	Data input. DSIZE is a programmable parameter of 32, 64, or 128.
addr[ASIZE-1:0]	Input	N/A	Address for read/write. ASIZE is based on size of memory, which is derived by the following formula: ASIZE = RANK_SIZE + RSIZE + BSIZE + CSIZE.
dmsel[DSIZE/8-1:0]	Input	N/A	Data Mask select.
busy	Output	High	Busy signal indicates the controller will not accept any more commands.
dataout[DSIZE-1:0]	Output	N/A	Data out.
dataout_valid	Output	High	During a read, this signal indicates when the dataout bus from the controller contains valid data.
datain_valid	Output	High	This signal indicates when the user can start sending in data through datain bus during a write.
clk2x	Input	N/A	This is the doubled clock signal coming from the on-chip PLL.

Table 6. Power PC Bus Interface Signals

Signal Name	Direction	Active State	Description
clk	In	N/A	System Clock.
reset_n	In	LOW	System Reset.
ppc_aack_n	Out	LOW	Address Acknowledge. When asserted, this signal indicates the address phase of the transaction is complete.
ppc_addr[0:ASIZE_BIM]	In	N/A	Address Bus. Address received from a bus master after receiving a bus grant.
ppc_data_l[0:31]	I/O	N/A	Low Data Bus.
ppc_data_h[0:31]	I/O	N/A	High Data Bus.
ppc_artry_n	In	LOW	Address Retry. This signal indicates the current cycle is aborted and the bus master will issue a request at a later time.
ppc_dbb_n	In	LOW	Data Bus Busy. The bus master that has received a data bus grant issues this signal. This signal indicates the length the data bus will be used for a memory access.
ppc_ta_n	Out	LOW	Transfer Acknowledge. This signal indicates the data transfer on the PowerPC bus has been completed.
ppc_tbst_n	In	LOW	Transfer Burst. This signal indicates a burst transfer is in progress.
ppc_tea_n	Out	LOW	Transfer Error Acknowledge. This signal indicates an error has occurred during a data transfer.
ppc_ts_n	In	LOW	Transfer Start. This signal indicates the master has begun a memory bus transaction, and the address and transfer attributes are valid.
ppc_tsiz[0:2]	In	LOW	Transfer Size.
ppc_tt[0:4]	In	LOW	Transfer Type.
clk2x	In	N/A	This the doubled clock signal coming from the on-chip PLL.

Table 7. PCI Local Bus Interface Signals

Signal Name	Direction	Active	Description
clk	In	N/A	PCI System Clock.
reset_n	In	LOW	Asynchronous PCI Reset.
l_data_in[DSIZE-1:0]	Out	N/A	Local Address/Burst Length/Data Input. The address/burst length input is used in master transactions. The data input is used for a master write or for a target read.
l_data_out[DSIZE-1:0]	In	N/A	Local data output for a master read or a target write.
lt_address_out[ASIZE_BIM-1:0]	In	N/A	Local starting address output for target reads and writes.
lt_ben_out[DSIZE_BIM/8-1:0]	In	N/A	Local target byte enables.
lt_command_out[3:0]	In	N/A	Local command for target reads and writes.
lt_abortn	Out	LOW	Local target abort request.
lt_disconnectn	Out	LOW	Local target disconnect or retry.
l_interruptn	Out	LOW	Local side interrupt request (multi-function device may need additional IRQ signals).
lt_rdyn	Out	LOW	Local target ready to receive data (write) or send data (read).
lt_r_nw	In	HIGH	Read/Write# (read/not write). Signals whether the current transaction is a read or write.

Table 7. PCI Local Bus Interface Signals (Continued)

Signal Name	Direction	Active	Description
cache[7:0]	In	N/A	Local target controller cache register output.
status[5:0]	In	N/A	Local target controller status register.
lt_hdata_xfern	In	LOW	Memory or I/O high DWORD read or write data phase complete. The address counter can be incremented in combination with the lt_ldataxfern.
lt_ldata_xfern	In	LOW	Memory or I/O low DWORD read or write data phase complete. The address counter can be incremented in combination with the lt_hdataxfern.
exprom_hit	In	HIGH	Expansion ROM register hit.
bar_hit[5:0]	In	N/A	Signals that the current address is within one of the base address register ranges, and access is requested until the current cycle is done (multi-function devices will need an additional set of registers for each function).
lt_64bit_transn	In	LOW	Signals the local target that a 64-bit read or write transaction is underway.
clk2x	In	N/A	This is the doubled clock signal coming from the on-chip PLL.

Table 8. AMBA Bus Interface Signals

Signal Name	Direction	Active State	Description
clk	In	N/A	Bus Clock. This clock times all bus transfers. All signal timings are related to the rising edge of clk.
reset_n	In	LOW	The bus reset signal is active LOW and is used to reset the system and the bus. This is the only active LOW signal.
HADDR[HASIZE:0]	In	N/A	The 32-bit system address bus.
HTRANS[1:0]	In	N/A	Transfer type. This indicates the type of the current transfer, which can be NONSEQUENTIAL, SEQUENTIAL, IDLE or BUSY.
HWRITE	In	HIGH	Transfer direction. When HIGH, this signal indicates a write transfer. When LOW, it indicates a read transfer.
HSIZE[2:0]	In	N/A	Transfer size. Indicates the size of the transfer, which is typically byte (8-bit), half word (16-bit), word (32-bit) or double word (64-bit) for a 64-bit AHB Bus.
HBURST[2:0]	In	N/A	Burst type. Indicates if the transfer forms part of a burst. Four, eight and sixteen beat bursts are supported. The burst may be either incremental or wrapping.
HWDATA[HDSIZE-1:0]	In	HIGH	Write data bus. The write data bus is used to transfer data from the master to the bus slaves during write operations.
HSELx	In	HIGH	Slave select. This signal indicates that the current transfer is intended for the slave. This signal is a combinatorial decode of the address bus.
HSELregx	In	HIGH	This signal indicates the current transfer is meant for internal registers of the Bus Interface Block. This is valid only when HSELx is asserted.
HSELmemx	In	HIGH	This signal indicates the current transfer is meant for DDR memory data. This is valid only when HSELx is asserted.
HREADY	In	HIGH	Transfer done. When HIGH, the HREADY signal indicates that a transfer has finished on the bus.
HRDATA[HDSIZE-1:0]	Out	N/A	Read data bus. The read data bus is used to transfer data from bus slaves to the bus master during read operations.
HREADY_out	Out	HIGH	Transfer done. When high, the HREADY_out signal indicates that a transfer has finished on the bus. This signal may be driven LOW to extend a transfer.

Table 8. AMBA Bus Interface Signals (Continued)

Signal Name	Direction	Active State	Description
HRESP[1:0]	Out	N/A	Transfer response. The transfer response provides additional information on the status of a transfer. Four different responses are possible: OKAY, ERROR, RETRY and SPLIT. RETRY and SPLIT are not supported.
clk2x	In	N/A	This is the doubled clock signal coming from the on-chip PLL.

Custom Core Configurations

For DDR SDRAM core configurations that are not available in the Evaluation Package, please contact your Lattice sales office to request a custom configuration.

Related Information

For more information regarding core usage and design verification, refer to the *DDR SDRAM Controller IP Core User's Guide*, available on the Lattice web site at www.latticesemi.com.

Appendix for Series 4 ORCA[®] FPGAs or FPSCs

Table 9. Performance and Resource Utilization¹

Parameter File	Core Configuration	ORCA 4 PFUs ²	LUTs	Registers	Dist. RAM ³	f _{MAX} (MHz)	External Pins	sysMEM™ EBRs
ddrct_gen_o4_1_008.lpc	Generic I/F	344	1359	1559	N/A	100	239	N/A
ddrct_ahb_o4_1_008.lpc	AHB I/F	560	2322	2451	18	100	242	N/A
ddrct_pci_o4_1_008.lpc	PCI I/F	510	2024	2070	16	66 ⁴	246	N/A
ddrct_ppc_o4_1_008.lpc	PPC I/F	492	1922	2170	18	100	181	N/A

1. Performance and utilization characteristics are generated using an OR4E022BA352 in ispLEVER™ v.3.0 software except for the AHB configuration 008 which is generated using OR4E042BM416. When using this IP core in a different density, package, speed, or grade within the ORCA Series 4 family, performance may vary.
2. PFU is a standard logic block of some Lattice devices. For more information, check the data sheet of the device.
3. Dist. RAM = distributed memory.
4. Performance for the PCI configuration of this DDR core is limited by the maximum throughput of the PCI 2.2 interface (66MHz).

Supplied Netlist Configurations

The Ordering Part Numbers (OPN) for all configurations of this core on ORCA Series 4 are DDRCT-GEN-O4-N1, DDRCT-PCI-O4-N1, DDRCT-AHB-O4-N1, and DDRCT-PPC-O4-N1. Table 10 lists the Lattice-specific netlists that are available in Evaluation Package, which can be downloaded from the Lattice web site at www.latticesemi.com.

Table 10. Parameter Files

Core Type	Config. Number	Data Size	Row Size	Bank Size	Column Size	Rank Size	Burst Length	Burst Type	CAS Latency
Generic I/F	008	64	12	2	10	3	4	0	2.0
AHB I/F	008	64	12	2	10	3	4	0	2.0
PPC I/F	008	64	12	2	10	3	4	0	2.0
PCI I/F	008	64	12	2	10	3	4	0	2.0

Appendix for ispXPGA® FPGAs

Table 11. Performance and Resource Utilization¹

Parameter File	Device	Core Config.	ispXPGA PFUs ²	LUTs	Registers	f _{MAX}	External Pins	sysMEM EBRs
ddrct_gen_xp_1_002.lpc	LFX125B-4FH516CES/2X	Generic I/F	393	1116	910	100	142	N/A
ddrct_ahb_xp_1_002.lpc	LFX500B-4FH516CES/2X	AHB I/F	751	1928	1599	100	145	N/A
ddrct_pci_xp_1_002.lpc	LFX500C-4FH516CES/2X	PCI I/F	688	1867	1333	66 ³	170	N/A
ddrct_ppc_xp_1_002.lpc	LFX500B-4FH516CES/2X	PPC I/F	647	1670	1392	100	154	N/A

1. Performance and utilization characteristics are generated using the ispXPGA device shown above in ispLEVER v.3.1 software. The evaluation version of this IP core only works on this specific device density, package and speed grade.
2. PFU is a standard logic block of some Lattice devices. For more information, check the data sheet of the device.
3. Performance for the PCI configuration of this DDR core is limited by the maximum throughput of the PCI 2.2 interface (66MHz).

Supplied Netlist Configurations

The Ordering Part Numbers (OPN) for all configurations of this core on ispXPGA are DDRCT-GEN-XP-N1, DDRCT-PCI-XP-N1, DDRCT-AHB-XP-N1, and DDRCT-PPC-XP-N1. Table 12 lists the Lattice-specific netlists that are available in Evaluation Package, which can be downloaded from the Lattice web site at www.latticesemi.com.

Table 12. Parameter Files

Core Type	Config. Number	Data Size	Row Size	Bank Size	Column Size	Rank Size	Burst Length	Burst Type	CAS Latency
Generic I/F	002	32	12	2	10	1	4	0	2.0
AHB I/F	002	32	12	2	10	1	4	0	2.0
PPC I/F	002	32	12	2	10	1	4	0	2.0
PCI I/F	002	32	12	2	10	1	4	0	2.0