

## Features

### ■ High Performance Bus Switching

- High bandwidth
  - Up to 13.6 Gbps (SERDES)
  - Up to 38 Gbps (without SERDES)
- Up to 16 (15x10) FIFOs for data buffering
- High speed performance
  - $f_{MAX} = 330\text{MHz}$
  - $t_{PD} = 3.0\text{ns}$
  - $t_{CO} = 3.1\text{ns}$
  - $t_S = 2.0\text{ns}$
- Built-in programmable control logic capability
- I/O intensive: 64 to 256 I/Os
- Expanded MUX capability up to 188:1 MUX

### ■ sysCLOCK™ PLL

- Frequency synthesis and skew management
- Clock multiply and divide capability
- Clock shifting up to  $\pm 2.35\text{ns}$  in 335ps steps
- Up to four PLLs

### ■ sysIO™ Interfacing

- LVCMOS 1.8, 2.5, 3.3 and LVTTTL support for standard board interfaces
- SSTL 2/3 Class I and II support
- HSTL Class I, III and IV support
- GTL+, PCI-X for bus interfaces
- LVPECL, LVDS and Bus LVDS differential support
- Hot socketing

- Programmable drive strength
- sysHSI Blocks Provide up to 16 High-Speed Channels
  - Serializer/de-serializer (SERDES) included
  - Clock Data Recovery (CDR) built in
  - 850 Mbps per channel
  - LVDS differential support
  - 10B/12B support
    - Encoding / decoding
    - Bit alignment
    - Symbol alignment
  - 8B/10B support
    - Bit alignment
    - Symbol alignment
  - Source Synchronous support

### ■ Flexible Programming and Testing

- IEEE 1532 compliant In-System Programmability (ISP™)
- Boundary scan test through IEEE 1149.1 interface
- 3.3V, 2.5V or 1.8V power supplies
- 5V tolerant I/O for LVCMOS 3.3 and LVTTTL interfaces

## Introduction

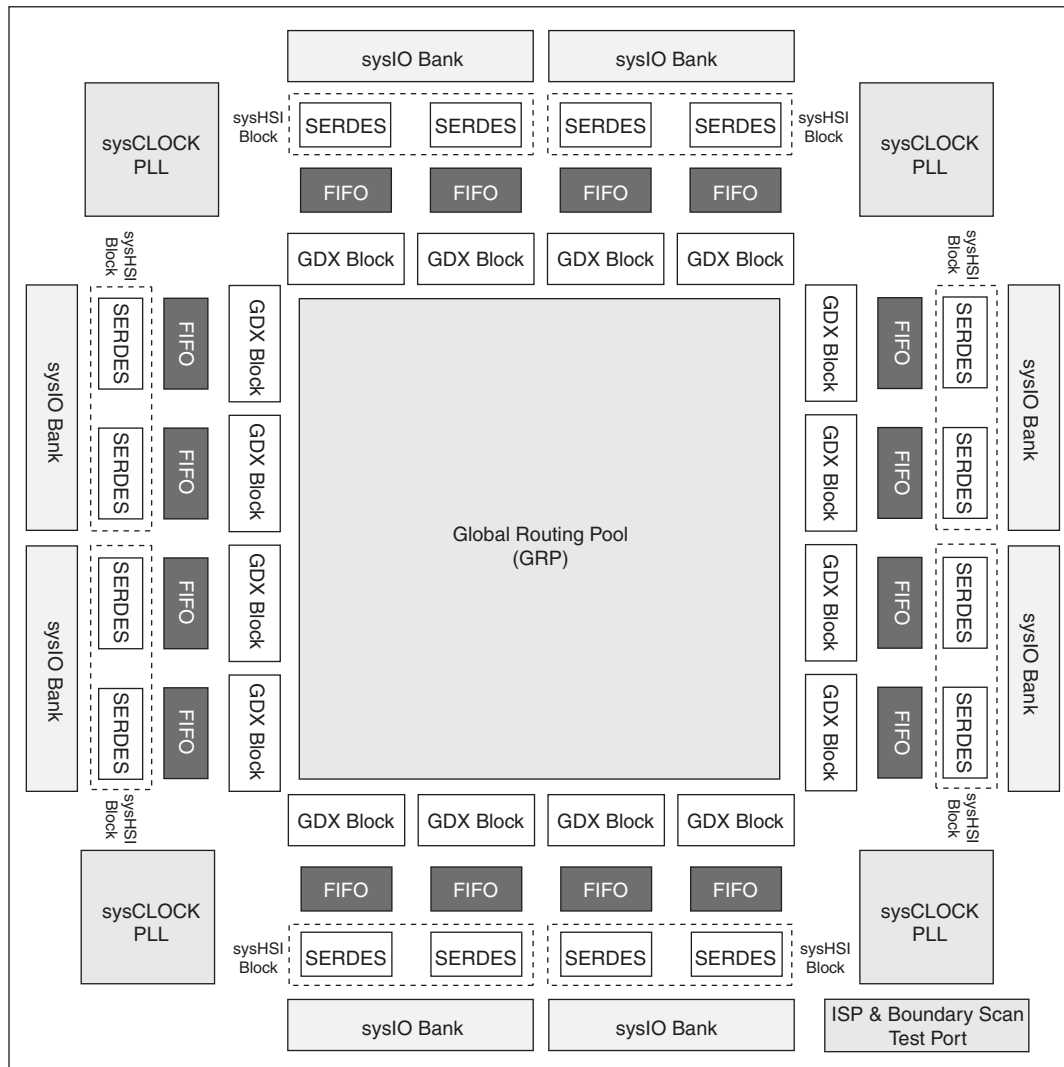
The ispGDX2™ family is Lattice's second generation in-system programmable generic digital crosspoint switch for high speed bus switching and interface applications.

**Table 1. ispGDX2 Family Selection Guide**

		ispGDX2-64	ispGDX2-128	ispGDX2-256
I/Os		64	128	256
GDX Blocks		4	8	16
$t_{PD}$		3.0ns	3.0ns	3.5ns
$t_S$		2.0ns	2.0ns	2.0ns
$t_{CO}$		3.1ns	3.1ns	3.2ns
$f_{MAX}$ (Toggle)		330MHz	330MHz	300MHz
Max bandwidth	SERDES <sup>2</sup>	3.5Gbps	7Gbps	13.6Gbps
	Without SERDES <sup>1</sup>	11Gbps	21Gbps	38Gbps
850 Mbps Duplex Channels		4	8	16
LVDS/Bus LVDS (Pairs)		32	64	128
PLLs		2	2	4
Package		100-ball fpBGA	208-ball fpBGA	484-ball fpBGA

1.  $f_{MAX}$  (Toggle) \* maximum I/Os divided by 2.

2. Max number of SERDES channels per device \* 850Mbps

**Figure 1. ispGDX2 Block Diagram (256-I/O Device)**

This family of switches combines a flexible switching architecture with advanced sysIO interfaces including 850 Mbps sysHSI Blocks, and sysCLOCK PLLs to meet the needs of the today's high-speed systems. Through a multiplexer-intensive architecture, the ispGDX2 facilitates a variety of common switching functions.

The availability of on-chip control logic further enhances the power of these devices. A high-performance solution, the family supports bandwidth up to 38Gbps.

Every device in the family has a number of PLLs to provide the system designer with the ability to generate multiple clocks and manage clock skews in their systems.

The sysIO interfaces provide system-level performance and integration. These I/Os support various modes of LVCMOS/LVTTL and support popular high-speed standard interfaces such as GTL+, PCI-X, HSTL, SSTL, LVDS and Bus-LVDS. The sysHSI Blocks further extend this capability by providing high speed serial data transfer capability.

Devices in the family can operate at 3.3V, 2.5V or 1.8V core voltages and can be programmed in-system via an IEEE 1149.1 interface that is compliant with the IEEE 1532 standard. Voltages required for the I/O buffers are independent of the core voltage supply. This further enhances the flexibility of this family in system designs.

Typical applications for the ispGDX2 include multi-port multi-processor interfaces, wide data and address bus multiplexing, programmable control signal routing and programmable bus interfaces. Table 1 shows the members of the ispGDX2 family and their key features.

## Architecture

The ispGDX2 devices consist of GDX Blocks interconnected by a Global Routing Pool (GRP). Signals interface with the external system via sysIO banks. In addition, each GDX Block is associated with a FIFO and a sysHSI Block to facilitate the transfer of data on- and off-chip. Figure 1 shows the ispGDX2 block diagram. Each GDX Block can be individually configured in one of four modes:

- Basic (No FIFO or SERDES)
- FIFO Only
- SERDES Only
- SERDES and FIFO

Each sysIO bank has its own I/O power supply and reference voltage. Designers can use any output standard within a bank that is compatible with the power supply. Any input standard may be used, providing it is compatible with the reference voltage. The banks are independent.

### Global Routing Pool (GRP)

The ispGDX2 architecture is organized into GDX Blocks, which are connected via a Global Routing Pool. The innovative GRP is optimized for routability, flexibility and speed. All the signals enter via the GDX Block. The block supplies these either directly or in registered form to the GRP. The GRP routes the signals to different blocks, and provides separate data and control routing. The data path is optimized to achieve faster speed and routing flexibility for nibble oriented signals. The control routing is optimized to provide high-speed bit oriented routing of control signals.

There are some restrictions on the allocation of pins for optimal bus routing. These restrictions are considered by the software in the allocation of pins.

### GDX Block

The blocks are organized in a “block” (nibble) manner, with each GDX Block providing data flow and control logic for 16 I/O buffers. The data flow is organized as four nibbles, each nibble containing four Multiplexer Register Blocks (MRBs). Data for the MRBs is provided from 64 lines from the GRP. Figure 2 illustrates the groups of signals going into and out of a GDX Block.

Control signals for the MRBs are provided from the Control Array. The Control Array receives the 32 signals from the GRP and generates 16 control signals: eight MUX Select, four Clock/Clock Enable, two Set/Reset and two Output Enable. Each nibble is controlled via two MUX select signals. The remaining control signals go to all the MRBs.

Besides the control signals from the Control Array, the following global signals are available to the MRBs in each GDX Block: four Clock/Clock Enable, one reset/preset, one power-on reset, two of four MUX select (two of two in 64 I/O), four Output Enable (two in 64 I/O) and Test Out Enable (TOE).

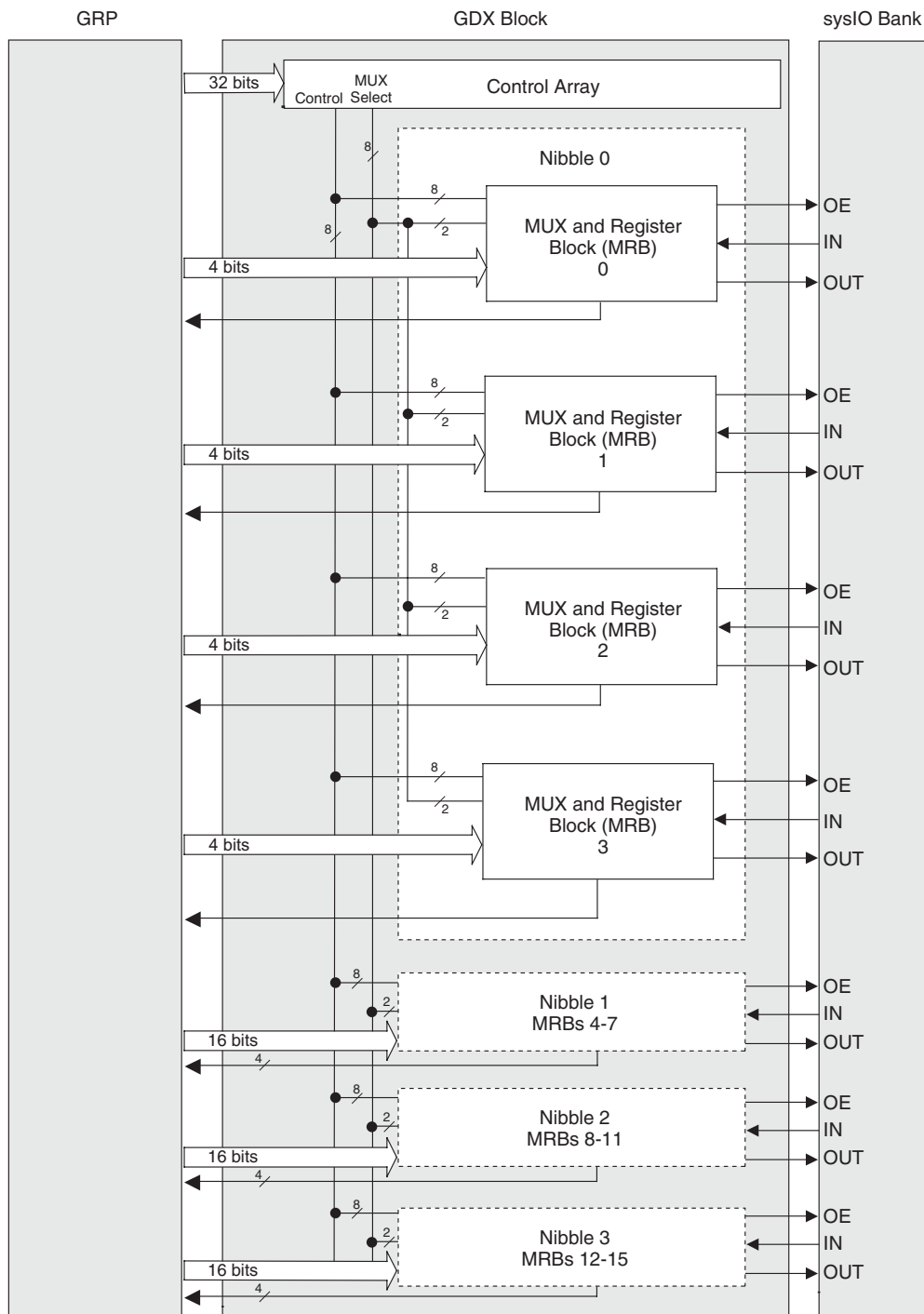
### MUX and Register Block (MRB)

Every MRB Block has a 4:1 MUX (I/O MUX) and a set of three registers which are connected to the I/O buffers, FIFO and sysHSI Blocks. Multiple MRBs can be combined to form large multiplexers as described below. Figure 3 shows the structure of the MRB.

Each of the three registers in the MRB can be configured as edge-triggered D-type flip-flop or as a level sensitive latch. One register operates on the input data, the other output data and the last register synchronizes the output enable function. The input and output data signals can bypass each of their registers. The polarity of the data out and output enable signals can be selected.

The Output and OE register share the same clock and clock enable signals. The Input register has a separate clock and clock enable. The initialization signals of each register can be independently configured as Set or Reset. These registers have programmable polarity control for Clock, Clock Enable and Set/Reset. The output enable register input can be set either by one of the two output enables generated locally from the Control Array or from one of the four (two in 64 I/O) Global OE enable pins. In addition to the local clock and clock enable signals, each MRB has access to Global Clock, Clock Enable, Reset and TOE nets.

**Figure 2. GDX Block**



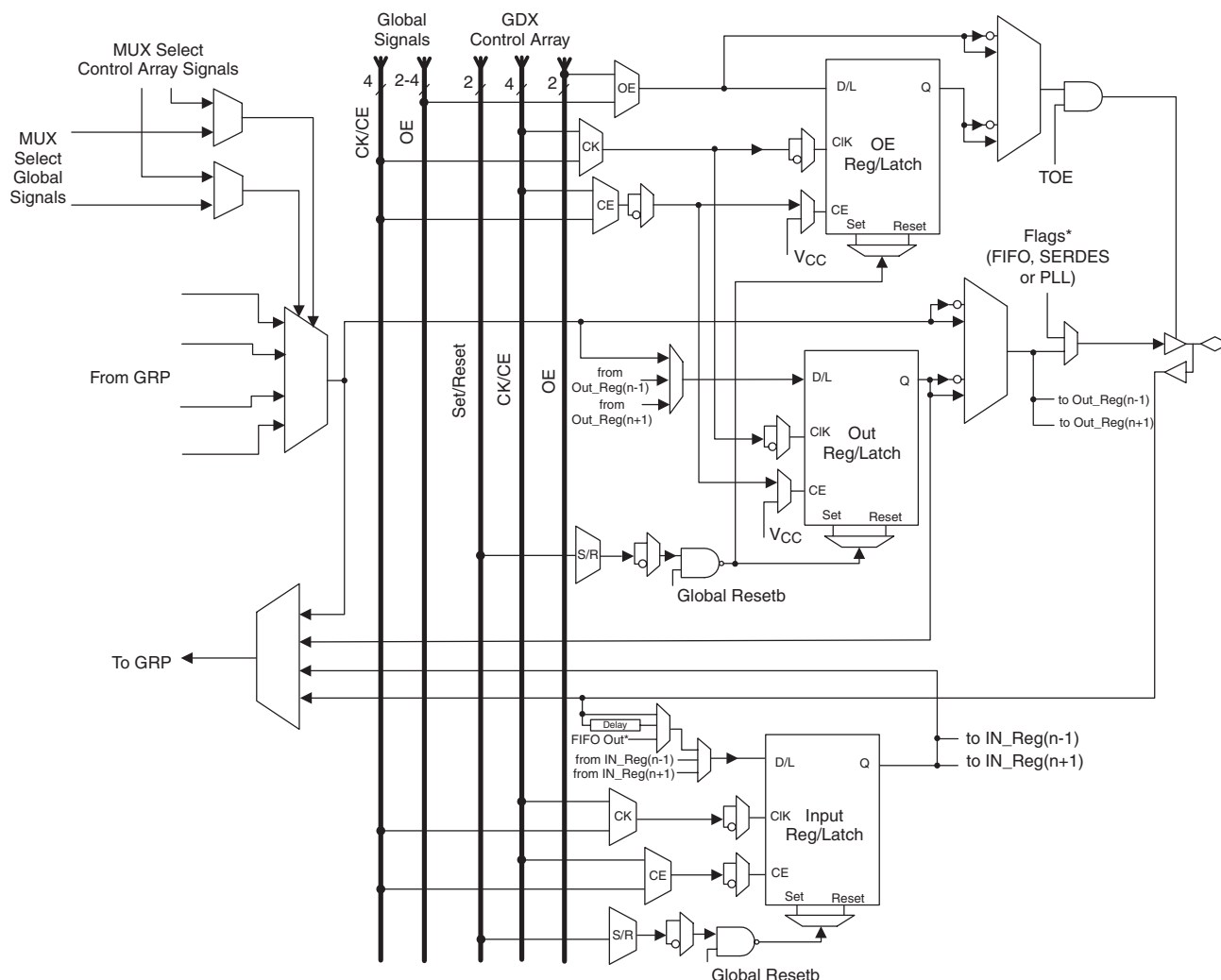
The output register of the MRB has a built-in bi-directional shift register capability. Each output register corresponding to MRB “n”, receives data output from its two adjacent MRBs, MRB (n-1) and MRB (n+1), to provide shift register capability. Like the output register, each input register of the MRB has built-in shift register capability. Each input register can receive data from its two adjacent MRB input registers, to provide bi-directional shift register capability. The chaining crosses GDX Block boundaries. The chain of input registers and the chain of output registers can be combined as one shift register via the GRP.

The four data inputs to the 4:1 MUX come from the GRP. The output of this MUX connects to the output register. A fast feedback path from the MUX to the GRP allows wider MUXes to be built. Table 2 summarizes the various MUX sizes and delay levels.

**Table 2. MUX Size Versus Internal Delay**

MUX Sizes	Levels of Internal GRP Delays
4:1	One Level
Up to 16:1	Two Levels
Up to 64:1	Three Levels
Up to 188:1 (with ispGDX2-256)	Four Levels

**Figure 3. ispGDX2 Family MRB**

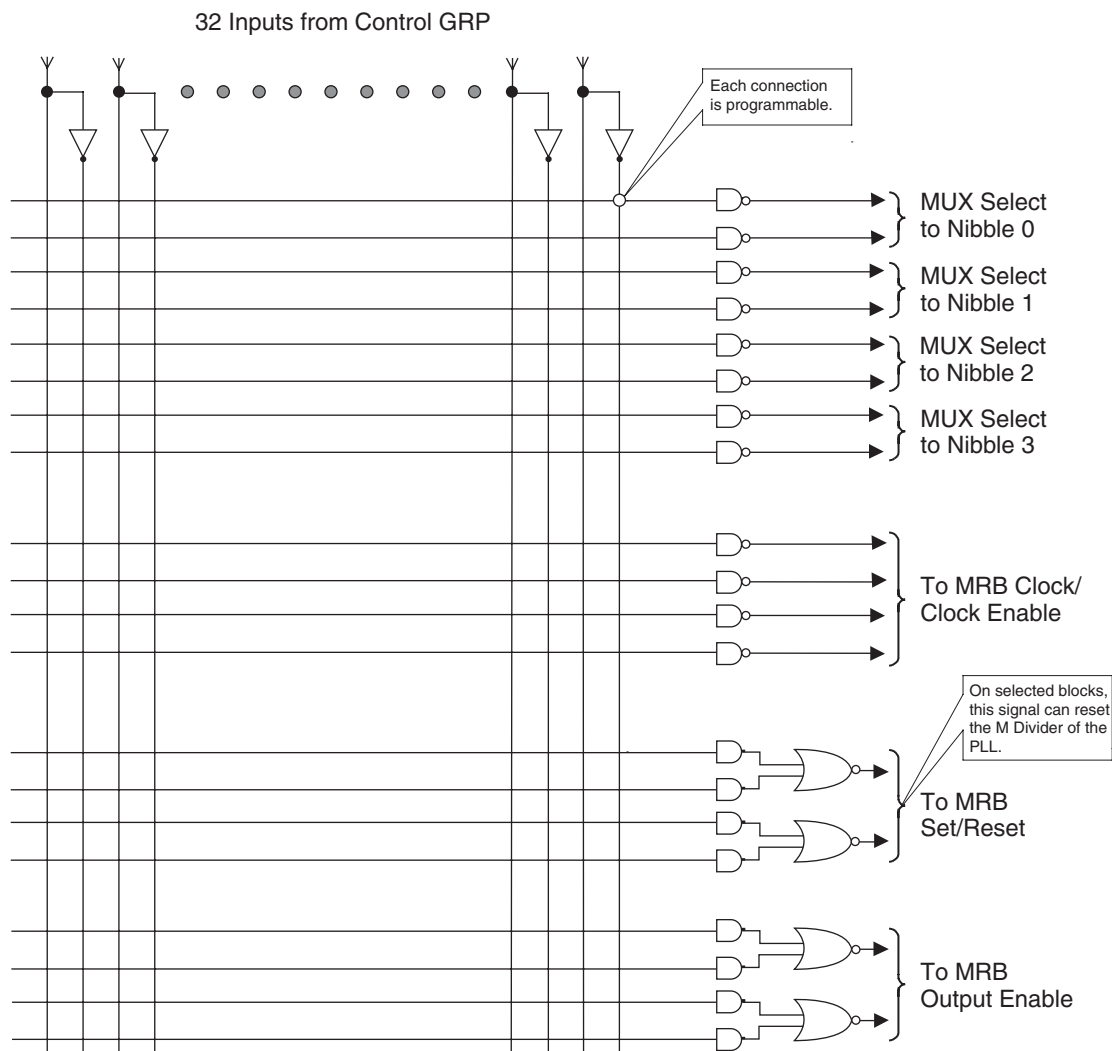


\*Selected MRBs see Logic Signal Connection Table for details

## Control Array

The control array generates control signals for the 16 MRBs within a GDX Block. The true and complement forms of 32 inputs from the GRP are available in the control array. The 20 NAND terms can use any or all of these inputs to form the control array outputs. Two AND terms are combined with a NOR term to form Set/Reset and OE signals. Figure 4 illustrates the control array.

**Figure 4. ispGDX2 Family Control Array**

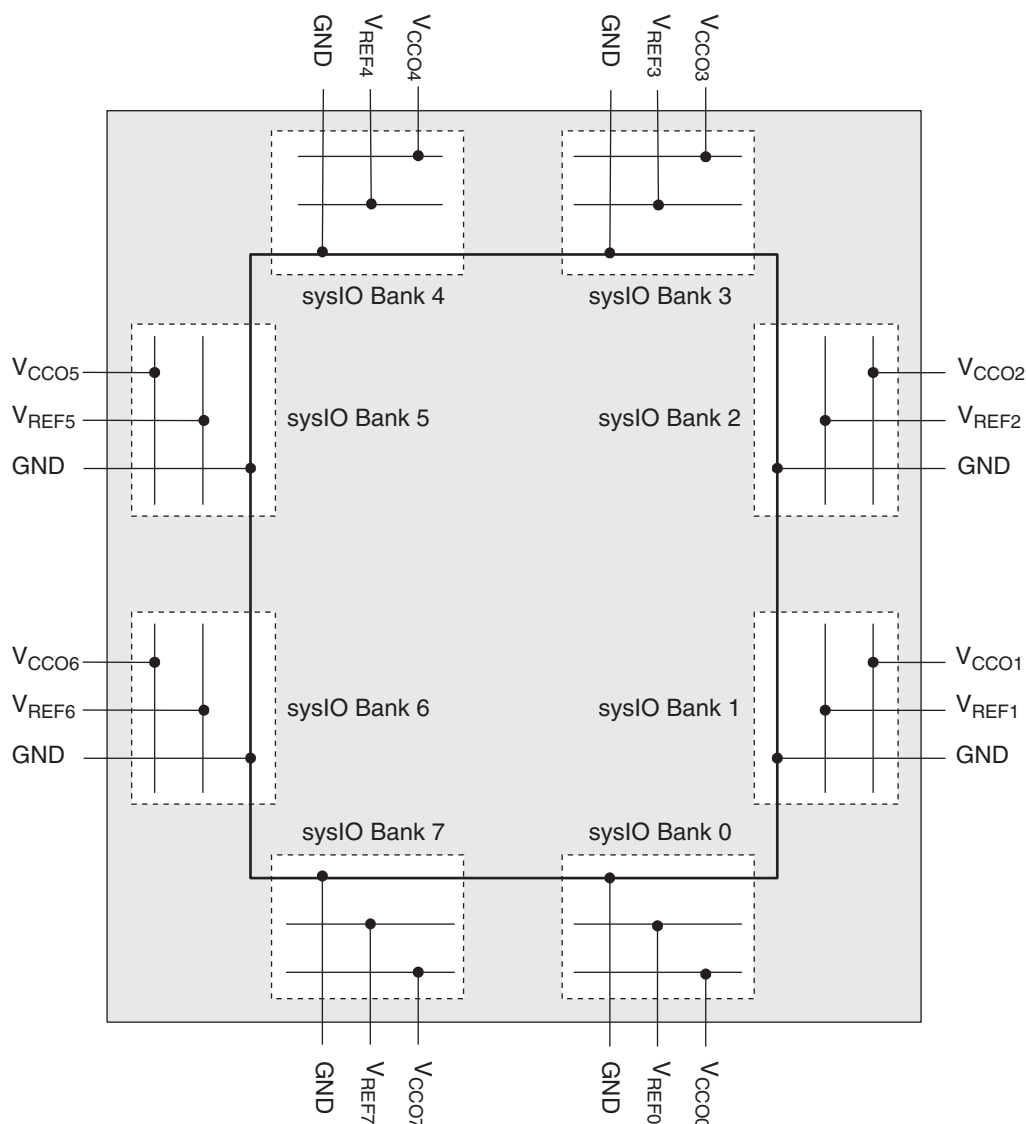


## sysIO Banks

The inputs and outputs of ispGDX2 devices are divided into eight sysIO banks, where each bank is capable of supporting different I/O standards. The number of I/Os per bank is 32, 16 and 8 for the 256-, 128- and 64-I/O devices respectively. Each sysIO bank has its own I/O supply voltage ( $V_{CCO}$ ) and reference voltage ( $V_{REF}$ ), allowing each bank complete independence from the other banks. Each I/O within a bank can be individually configured to any standard consistent with the  $V_{CCO}$  and  $V_{REF}$  settings. Figure 5 shows the I/O banks for the ispGDX2-256 device.

The I/O of the ispGDX2 devices contain a programmable strength and slew rate tri-state output buffer, a programmable input buffer, a programmable pull-up resistor, a programmable pull-down resistor and a programmable bus-keeper latch. These programmable capabilities allow the support of a wide range of I/O standards.

Figure 5. ispGDX2-256 sysIO Banks



There are three classes of I/O interface standards implemented in the ispGDX2 devices. The first is the non-terminated, single-ended interface; it includes the 3.3V LVTTTL standard along with the 1.8V, 2.5V and 3.3V LVCMOS interface standards. The slew rate and strength of these output buffers can be controlled individually. Additionally, PCI 3.3, PCI-X and AGP-1X are all subsets of this interface type. The second interface class implemented is the terminated, single-ended interface standard. This group of interfaces includes different versions of SSTL and HSTL interfaces along with CTT and GTL+. Use of these I/O interfaces requires an additional  $V_{REF}$  signal. At the system level, a termination voltage,  $V_{TT}$ , is also required. Typically, an output will be terminated to  $V_{TT}$  at the receiving end of the transmission line it is driving. The final types of interfaces implemented are the differential standards LVPECL, LVDS and Bus LVDS. Table 3 shows the I/O standards supported by the ispGDX2 devices along with nominal  $V_{CCO}$ ,  $V_{REF}$  and  $V_{TT}$ .

The ispGDX2 family also features 5V tolerant I/O. I/O banks with  $V_{CCO} = 3.3V$  may have inputs driven to a maximum of 5.5V for easy interfacing with legacy systems. Up to 64 I/O pins per device may be driven by 5V inputs.

**Table 3. ispGDX2 Supported I/O Standards**

sysIO Standard	Nominal $V_{CCO}$	Nominal $V_{REF}$	Nominal $V_{TT}$
LVC MOS 3.3	3.3V	—	—
LVC MOS 2.5	2.5V	—	—
LVC MOS 1.8	1.8V	—	—
LV TTL	3.3V	—	—
PCI 3.3	3.3V	—	—
PCI -X	3.3V	—	—
AGP-1X	3.3V	—	—
SSTL3 class I & II	3.3V	1.5V	1.5V
SSTL2 class I & II	2.5V	1.25V	1.25V
CTT 3.3	3.3V	1.5V	1.5V
CTT 2.5	2.5V	1.25V	1.25V
HSTL class I	1.5V	0.75V	0.75V
HSTL class III	1.5V	0.9V	0.75V
HSTL class IV	1.5V	0.9V	1.5V
GTL+	1.8/2.5/3.3V	1.0V	1.5V
LVPECL <sup>1, 2, 3</sup>	3.3V	—	—
LVDS	2.5/3.3V	—	—
Bus-LVDS	2.5/3.3V	—	—

1. LVPECL drivers require three resistor pack (see Figure 15).

2. Depending on the driving LVPECL output specification, GDX2 LVPECL input driver may require terminating resistors.

3. For additional information on LVPECL refer to Lattice technical note number TN1000, *sysIO Design and Usage Guidelines*.

The dedicated inputs support a subset of the sysIO standards indicated in Table 4. These inputs are associated with a bank consistent with their location.

**Table 4. I/O Standards Supported by Dedicated Inputs**

	LVC MOS	LVDS	All other ASIC I/Os
Global OE Pins	Yes	No	Yes <sup>2</sup>
Global MUX Select Pins	Yes	No	Yes <sup>2</sup>
Resetb	Yes	No	Yes <sup>2</sup>
Global Clock/Clock Enables	Yes	Yes	Yes <sup>2</sup>
ispJTAG™ Port	Yes <sup>1</sup>	No	No
TOE	Yes	No	No

1. LVC MOS as defined by the  $V_{CCJ}$  pin voltage.

2. No PCI clamp.

For more information on the sysIO capability, please refer to Lattice technical note number TN1000, *sysIO Design and Usage Guidelines*.

## sysCLOCK PLL

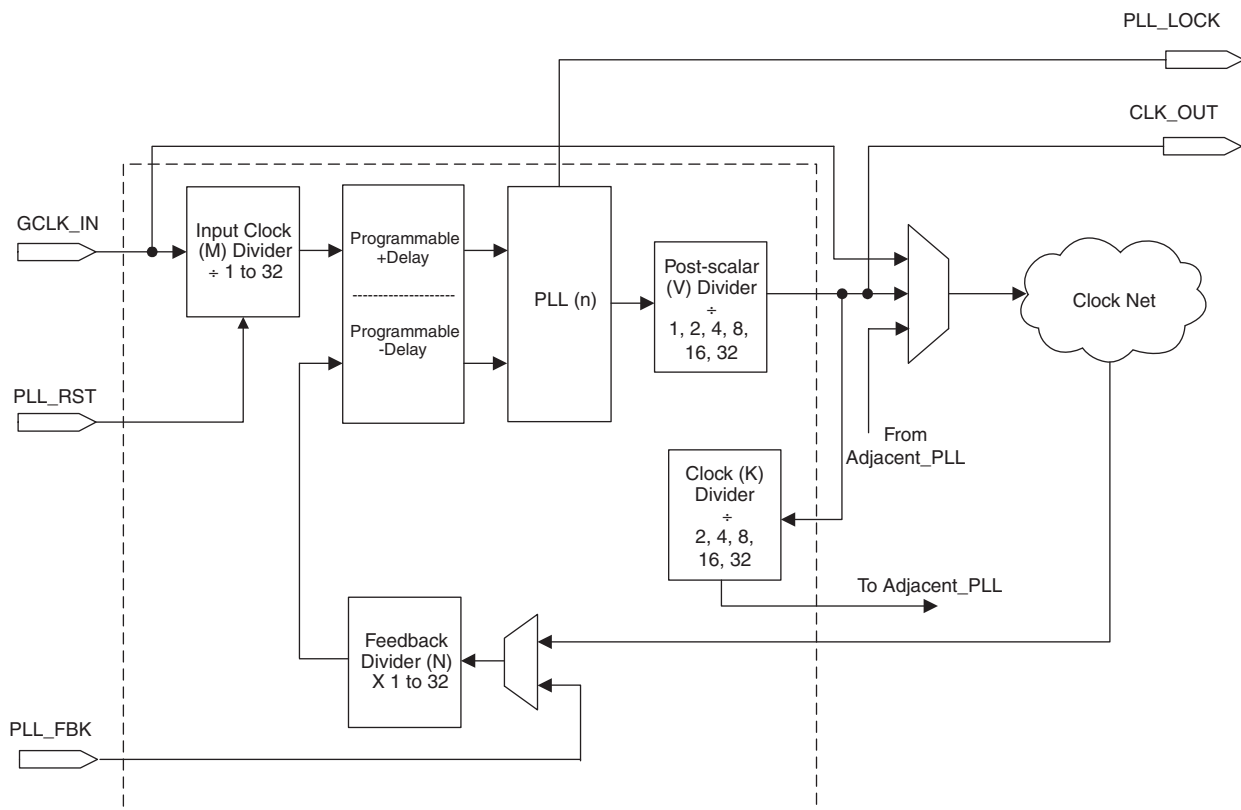
The sysCLOCK PLL circuitry consists of Phase-Lock Loops (PLLs) along the various dividers and reset and feedback signals associated with the PLLs. This feature gives the user the ability to synthesize clock frequencies and generate multiple clock signals for routing within the device. Furthermore, it can generate clock signals that are deskewed either at the board level or the device level. Figure 6 shows the ispGDX2 PLL block diagram.

Each PLL has a set of PLL\_RST, PLL\_FBK and PLL\_LOCK signals. In order to facilitate the multiply and divide capabilities of the PLL, each PLL has associated dividers. The M divider is used to divide the clock signal, while the



N divider is used to multiply the clock signal. The K divider is used to provide a divided clock frequency of the adjacent PLL. This output can be routed to the global clock net. The V divider is used to provide lower frequency output clocks, while maintaining a stable, high frequency output from the PLL's VCO circuit. The PLL also has a delay feature that allows the output clock to be advanced or delayed to improve set-up and clock-to-out times for better performance. For more information on the PLL, please refer to Lattice technical note number TN1003, *sysCLOCK PLL Design and Usage Guidelines*.

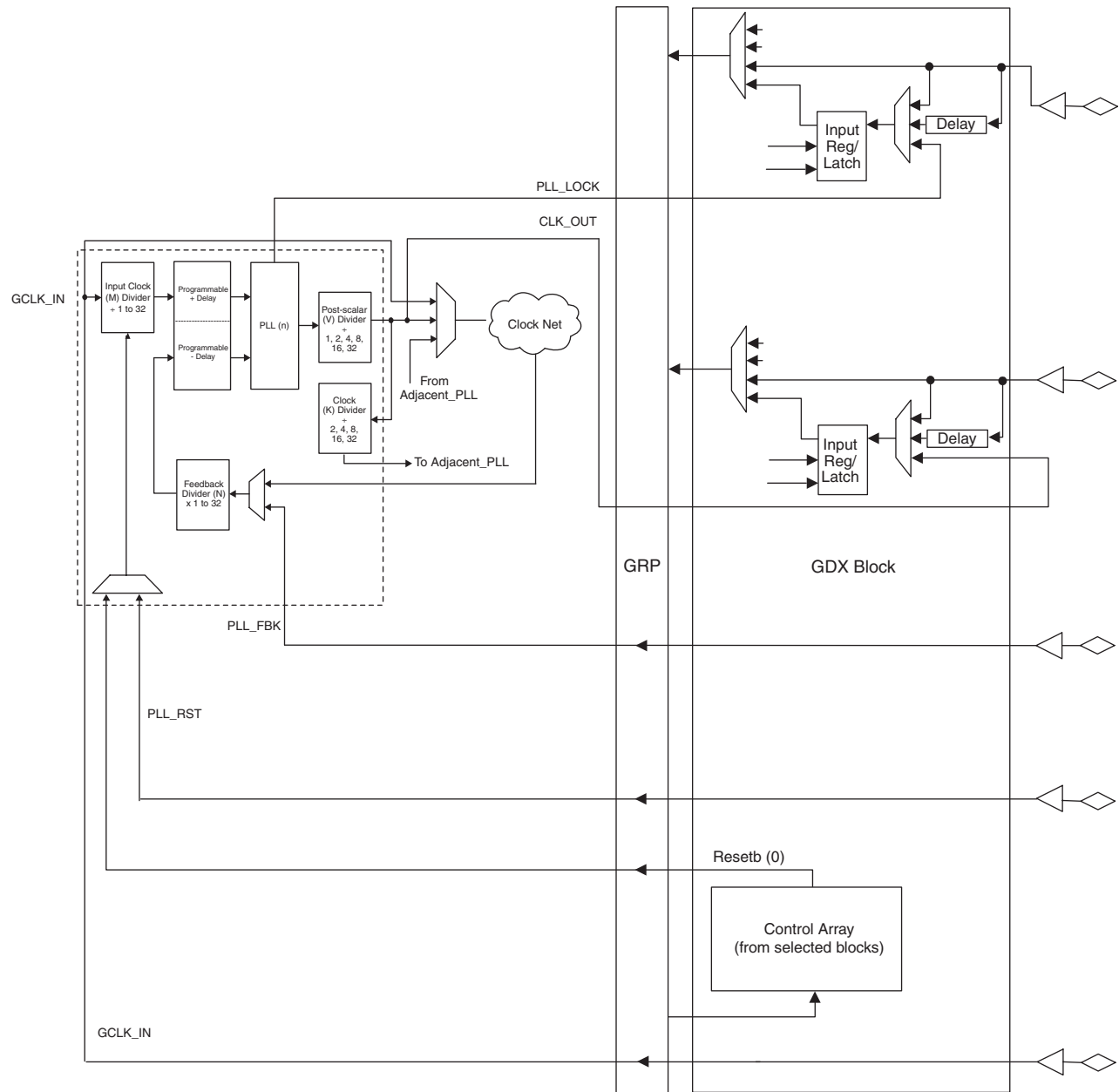
**Figure 6. sysCLOCK PLL**



There are four global clock networks routed to each MRB block. These global clocks, CLK0-3, can either be generated by the PLL circuits or supplied externally. External clock pins can be configured as single-ended or differential (LVDS) input. Figure 7 illustrates how the sysCLOCK PLL inputs and outputs can be routed to the I/O pins or general routing. Figure 8 shows the clock network for the ispGDX2-256 and Figure 9 shows the clock networks for ispGDX2-128 and ispGDX2-64. The Reset (0) pin from the Control Array of selected GDX Blocks can be programmed to reset the M Divider of the PLLs. This provides a means for generating the reset signal internally. Table 5 details which GDX Block provides reset to the PLLs.

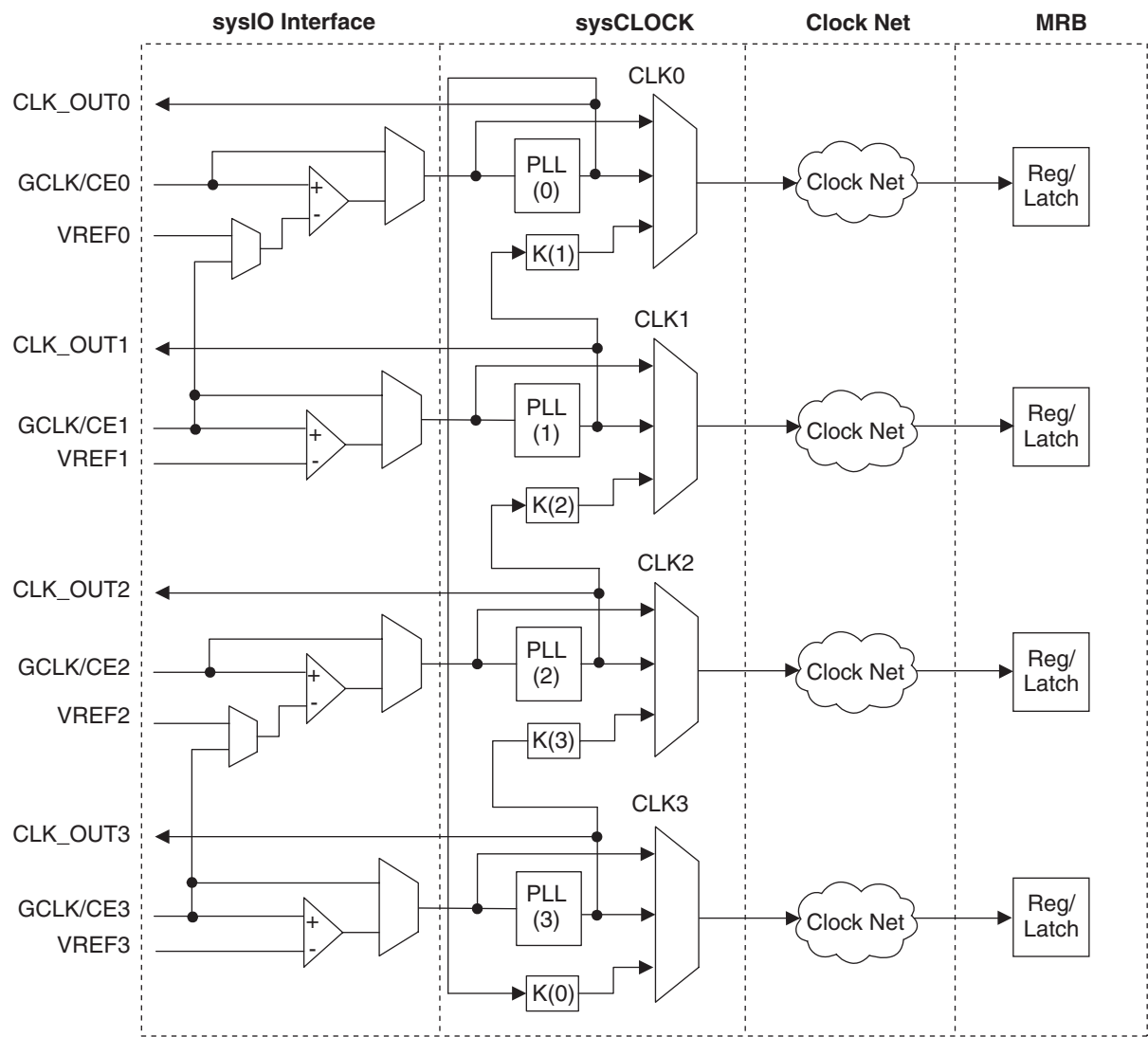
**Table 5. Internal Reset Input of the PLL (M Divider)**

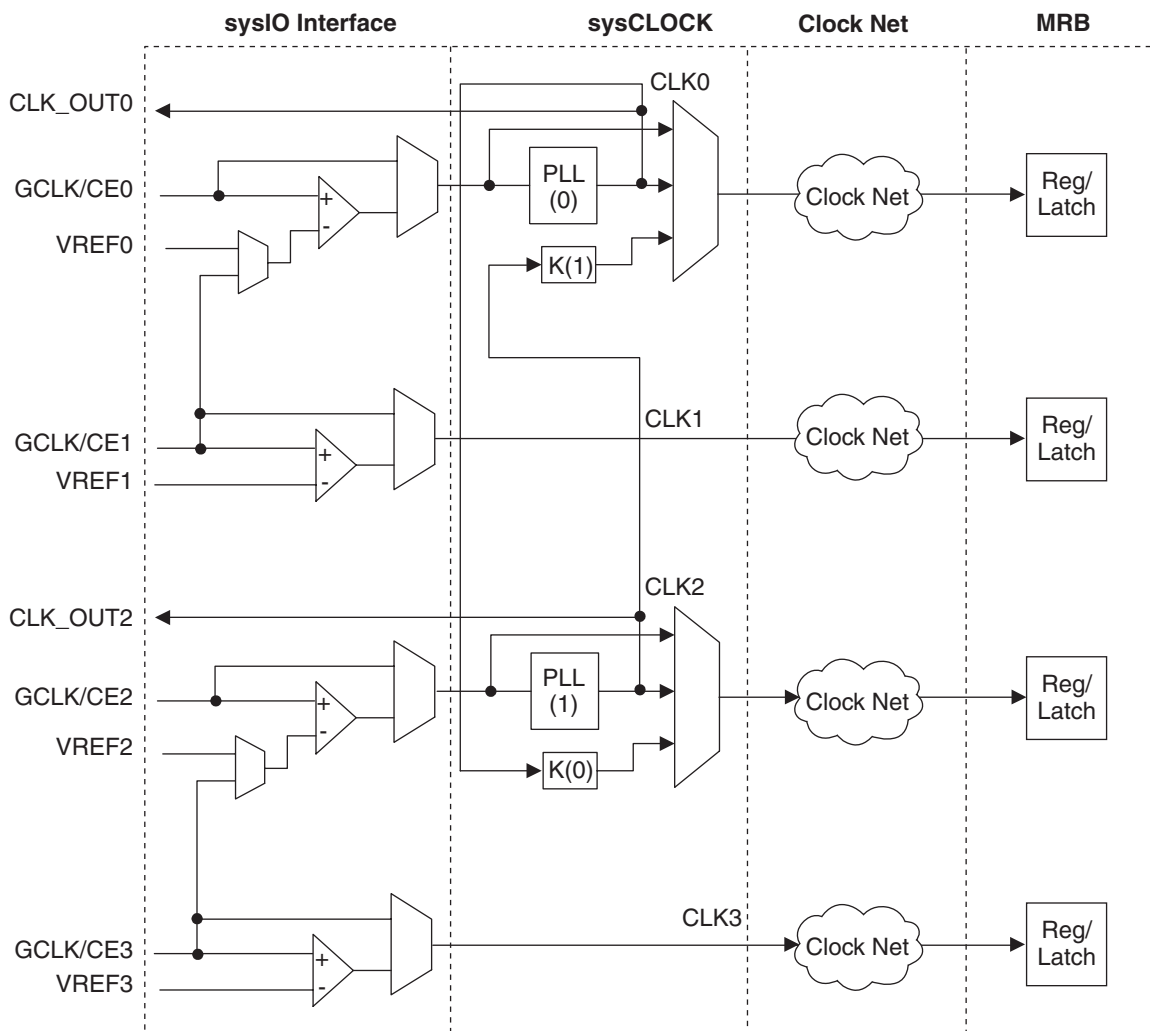
	PLL0	PLL1	PLL2	PLL3
ispGDX2-256	GDX Block 5A	GDX Block 7B	GDX Block 1A	GDX Block 3B
ispGDX2-128	GDX Block 2A	GDX Block 0A	—	—
ispGDX2-64	GDX Block 0A	GDX Block 1B	—	—

**Figure 7. I/O Pin Connection to the sysCLOCK PLL<sup>1</sup>**

1. Some pins are shared. See Logic Signal Connections Table for details.

Figure 8. ispGDX2-256 CLOCK Network

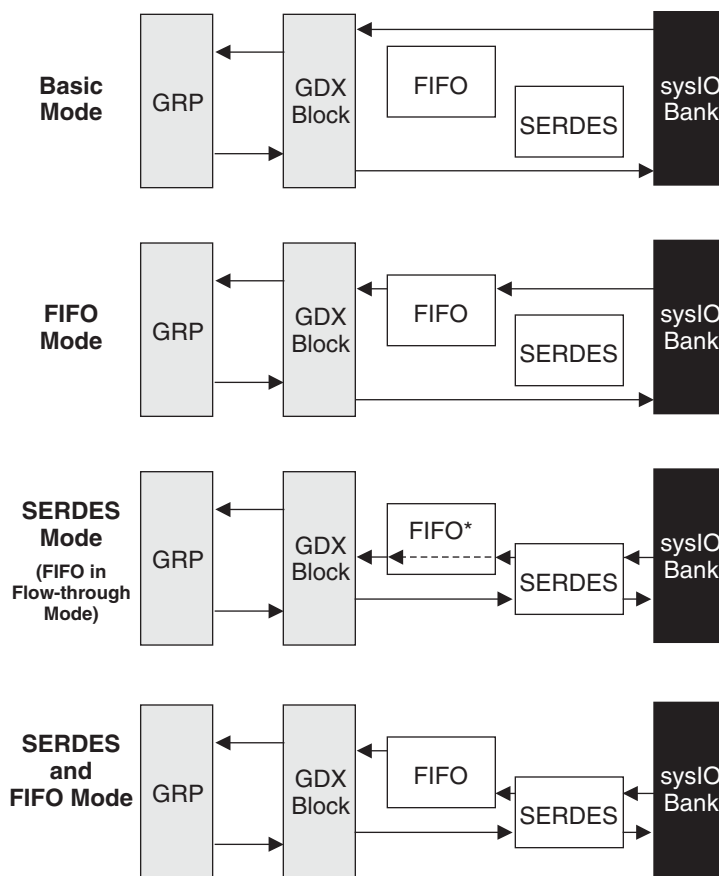


**Figure 9. ispGDX2-128 and 64 CLOCK Network**

## Operating Modes

All the GDX Blocks in the ispGDX2 family can be programmed in four modes: Basic, FIFO only, SERDES only, and FIFO with SERDES mode. In basic mode, the SERDES and FIFO are disabled and the MUX output of the MRB connects to the output register. Inputs are connected to the GRP via the MRB.

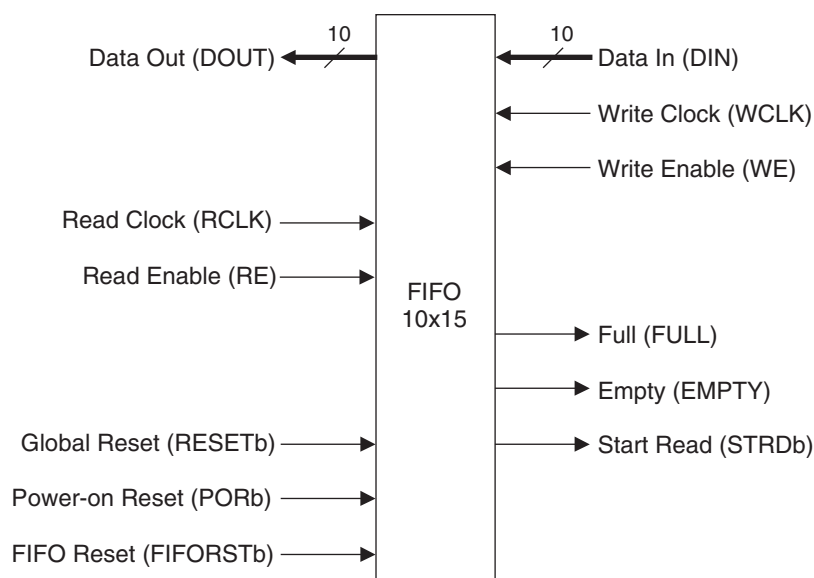
Figure 10 shows the four different operating modes. Precise detail of the FIFO and SERDES connections is provided in their respective sections.

**Figure 10. Four Operating Modes of ispGDX2 Devices**

\*FIFO held in RESET for SERDES-only mode.

## FIFO Operations

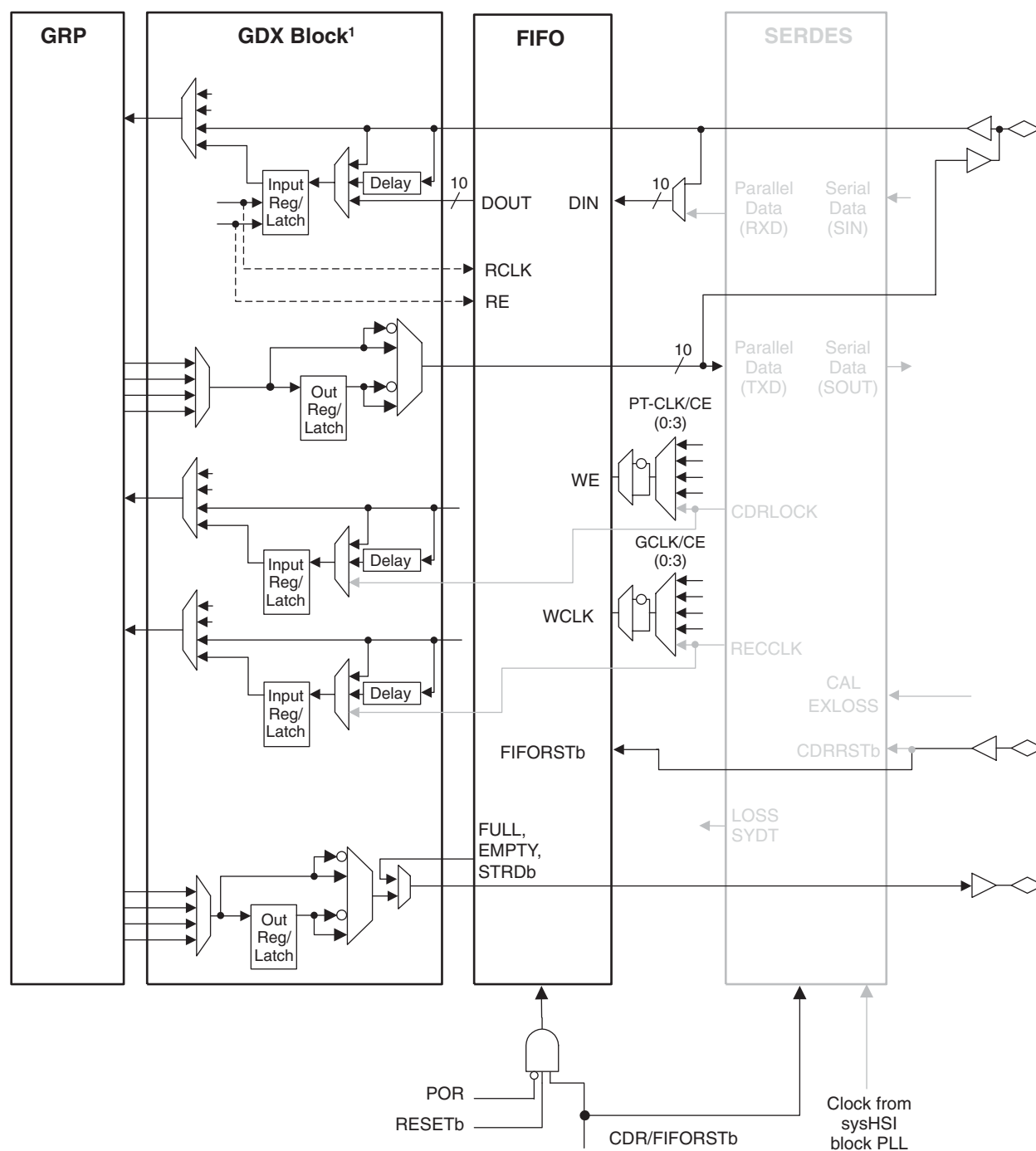
Each GDX Block is associated with a 10-bit wide and 15-word deep (10x15) RAM. This RAM, combined with two address counters and two comparators, is used to implement a FIFO as a “circular queue”. The FIFO has separate clocks, the Read Clock (RCLK) and Write Clock (WCLK), for asynchronous operation. The FIFO has three additional control signals Write Enable, Read Enable and FIFO Reset. Three flags show the status of the FIFO: Empty, Full and Start Read. Each FIFO receives the global Power-on Reset and Reset signals. Figure 11 shows the connections to the FIFO.

**Figure 11. ispGDX2 FIFO Signals**

Read Clock and Read Enable are the same as the Clock and Clock Enable signals of the input registers of the associated MRB. These registers are used to register the FIFO outputs, and in modes that utilize the FIFO are configured to use the same clock and clock enable signals. The Write Clock is selected from one of the GCLK/CE signals or the RECCLK (Recovered Clock) signal from the associated SERDES. The Write Enable is selected from one of the local MRB product term CLK/CE signals or the CDRLOCK (Clock/Data Recovery Lock) signal from the associated SERDES. All FIFO operations occur on the rising edge of the clock although clock polarity of these signals can be programmed.

The flags from the FIFO, FULL, EMPTY and STRDb (Start Read) are each fed via a MUX in the MRB to an I/O buffer. The STRDb (half full) signal is used in conjunction with SERDES. STRDb is an active low signal, the signal is inactive (high) on FIFO RESET. After the FIFO reset when the FIFO contains data in five memory locations, at the following write clock transition the STRDb becomes active (low). Note, if the Read Clocks arrive before writing the sixth location, it may take longer than five write clocks before the STRDb becomes active. When the FIFO has data in the first six locations, at the next write clock transition the STRDb becomes inactive (high). Again, if the Read Clocks arrive before writing the seventh location, the STRDb may stay active for longer than one write clock period, even if the FIFO contains data in less than five locations. After this event, the STRDb stays inactive until the FIFO is RESET again. STRDb does not become active again even if less than six memory locations are occupied in the FIFO. It is the user's responsibility to monitor the FULL and EMPTY signals to avoid data underflow/overflow and to take appropriate actions.

Figure 12 shows how the FIFO is connected between the I/O banks and the GDX Blocks in FIFO mode. For more information on the FIFO, please refer to Lattice technical note number TN1020, *sysHSI Usage Guidelines*.

**Figure 12. Operation in FIFO Mode<sup>2</sup>****Notes:**

1. For clarity, only a portion of the GDX Block is shown.
2. Some signals share pins. See Logic Signal Connections Table for details

## High Speed Serial Interface Block (sysHSI Block)

The High Speed Serial Interface (sysHSI) allows high speed serial data transfer over a pair of LVDS I/O. The ispGDX2 devices have multiple sysHSI Blocks.

Each sysHSI Block has two SERDES blocks which contain two main sub-blocks, Transmitter (with a serializer) and Receiver (with a deserializer) including Clock/Data Recovery Circuit (CDR). Each SERDES can be used as a full duplex channel. The two SERDES in a given sysHSI Block share a common clock and must operate at the same nominal frequency. Figure 13 shows the sysHSI Block.

Device features support two data coding modes: 10B/12B and 8B/10B (for use with other encoding schemes, see Lattice's sysHSI application notes). The encoding and decoding of the 10B/12B standard are performed within the device in dedicated logic. For the 8B/10B standard, the symbol boundaries are aligned internally but the encoding and decoding are performed outside the device.

Each SERDES block receives a single high speed serial data input stream (with embedded clock) from an input, and provide a low speed 10-bit wide data stream and a recovered clock to the device. For transmitting, the SERDES converts a 10-bit wide low-speed data stream to a single high-speed data stream with embedded clock for output.

Additionally, multiple sysHSI Blocks can be grouped together to form a source synchronous interface of between 1-8 channels.

Figure 14 shows the connections of the SERDES block with the FIFO, sysIO block and the MRB. Table 6 provides the descriptions of the SERDES.

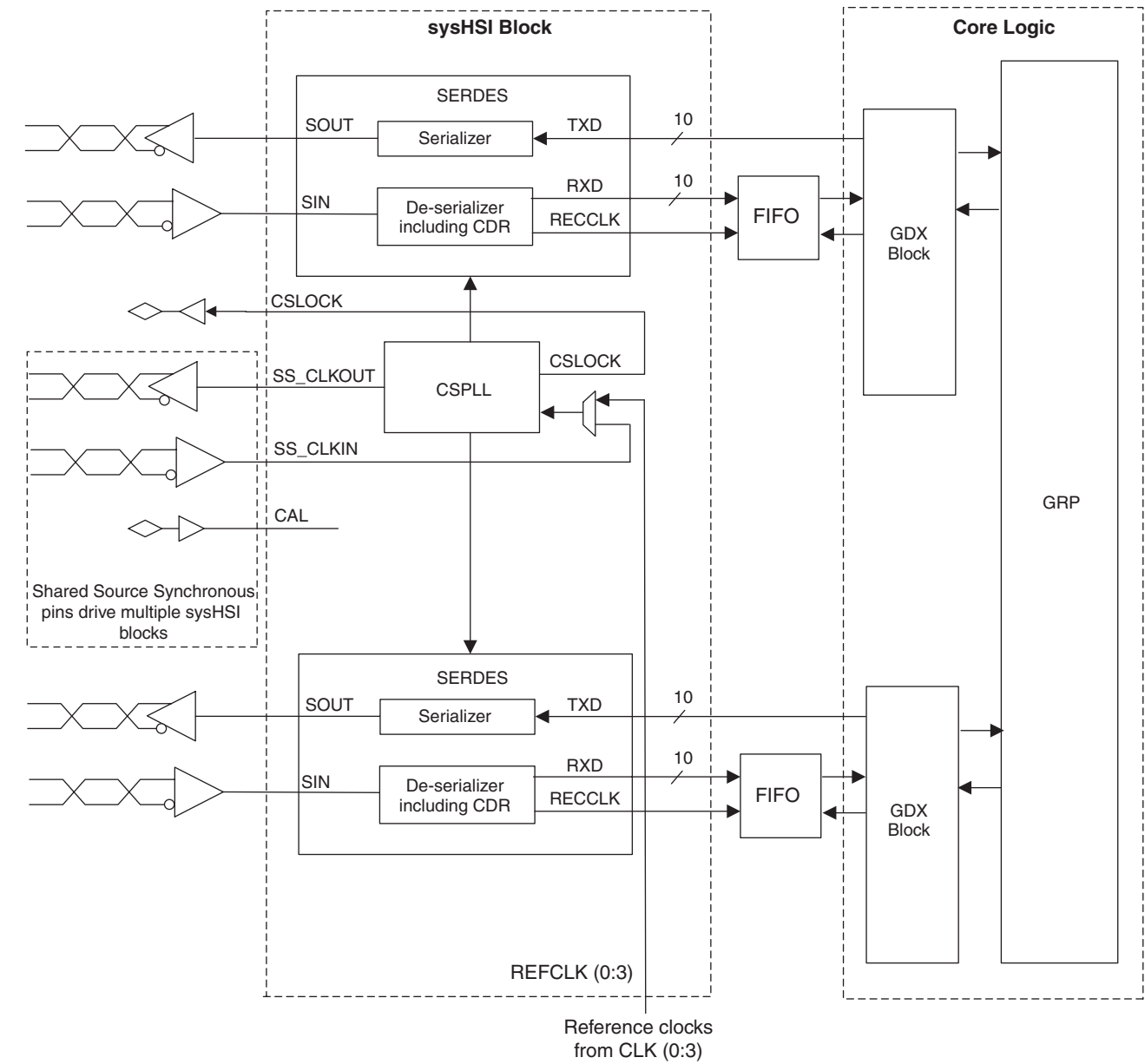
For more information on the SERDES/CDR, refer to Lattice technical note number TN1020, *sysHSI Usage Guidelines*.

**Table 6. SERDES Signal Descriptions**

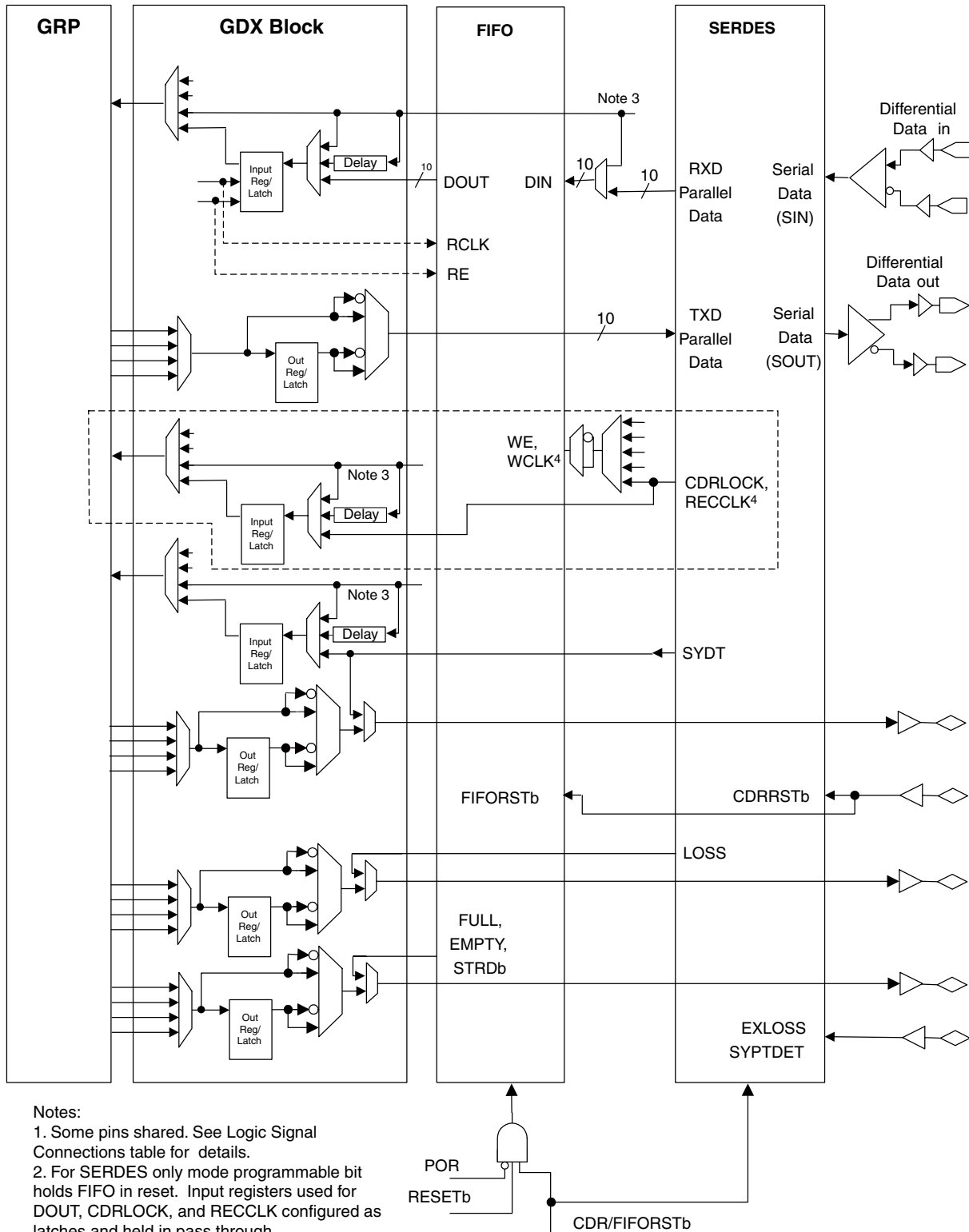
Signal	I/O	Description
CDRRST	I	Resets the CDR circuit of sysHSI block
LOSS	O	Loss of signal flag for sysHSI block
SYDT	O	Symbol alignment detect for sysHSI block
EXLOSS	I	Forces LOSS signal for sysHSI block
CAL	I	Initiates source synchronous calibration sequence
CDRLOCK	Internal	CDR lock output for sysHSI block
RXD	Internal	Parallel data in for sysHSI block
TXD	Internal	Parallel data out for sysHSI block
REFCLK	Internal	Reference clock received from the clock tree
SIN	I	Serial data input for sysHSI block
SOUT	O	Serial data output for sysHSI block
SS_CLKIN	I	Clock input for source synchronous group
SS_CLKOUT	O	Clock output for source synchronous group
RECCLK	Internal	Recovered clock from encoded data by CDR of sysHSI block
CSLOCK	Internal	Lock output of the PLL associated with sysHSI block



Figure 13. sysHSI Block with SERDES and FIFO



Note: Some pins are shared. See Logic Signal Connections table for details

Figure 14. Operation in SERDES Only and SERDES with FIFO Modes<sup>1, 2</sup>

## IEEE 1149.1-Compliant Boundary Scan Testability

All ispGDX2 devices have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more board-level testing. The test access port has its own supply voltage that can operate with LVCMOS3.3, 2.5 and 1.8 standards.

## sysIO Quick Configuration

To facilitate the most efficient board test, the physical nature of the I/O cells must be set before running any continuity tests. As these tests are fast, by nature, the overhead and time that is required for configuration of the I/Os' physical nature should be minimal so that board test time is minimized. The ispGDX2 family of devices allows this by offering the user the ability to quickly configure the physical nature of the sysIO cells. This quick configuration takes milliseconds to complete, whereas it takes seconds for the entire device to be programmed. Lattice's ispVM™ System programming software can either perform the quick configuration through the PC parallel port, or can generate the ATE or test vectors necessary for a third-party test system.

## IEEE 1532-Compliant In-System Programming

In-system programming of devices provides a number of significant benefits including rapid prototyping, lower inventory levels, higher quality and the ability to make in-field modifications. All ispGDX2 devices provide In-System Programming (ISP) capability through their Boundary Scan Test Access Port. This capability has been implemented in a manner that ensures that the port remains compliant to the IEEE 1532 standard. By using IEEE 1532 as the communication interface through which ISP is achieved, designers get the benefit of a standard, well defined interface.

The ispGDX2 devices can be programmed across the commercial temperature and voltage range. The PC-based Lattice software facilitates in-system programming of ispGDX2 devices. The software takes the JEDEC file output produced by the design implementation software, along with information about the scan chain, and creates a set of vectors used to drive the scan chain. The software can use these vectors to drive a scan chain via the parallel port of a PC. Alternatively, the software can output files in formats understood by common automated test equipment. This equipment can then be used to program ispGDX2 devices during the testing of a circuit board.

## Security Scheme

A programmable security scheme is provided on the ispGDX2 devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this scheme prevents readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. The security scheme also prevents programming and verification. The entire device must be erased in order to reset the security scheme.

## Hot Socketing

The ispGDX2 devices are well suited for those applications that require hot socketing capability. Hot socketing a device requires that the device, when powered down, can tolerate active signals on the I/Os and inputs without being damaged. Additionally, it requires that the effects of the powered-down device be minimal on active signals.

## Absolute Maximum Ratings<sup>1, 2, 3</sup>

	ispGDX2C (1.8V)	ispGDX2B/V (2.5/3.3V)
Supply Voltage $V_{CC}$ . . . . .	0.5 to 2.5V . . . . .	-0.5 to 5.5V
PLL Supply Voltage $V_{CCP}$ . . . . .	-0.5 to 2.5V . . . . .	-0.5 to 5.5V
Output Supply Voltage $V_{CCO}$ . . . . .	-0.5 to 4.5V . . . . .	-0.5 to 4.5V
JTAG Supply Voltage ( $V_{CCJ}$ ) . . . . .	-0.5 to 4.5V . . . . .	-0.5 to 4.5V
Input or I/O Tristate Voltage Applied <sup>4, 5</sup> . . . . .	-0.5 to 5.5V . . . . .	-0.5 to 5.5V
Storage Temperature . . . . .	-65 to 150°C . . . . .	-65 to 150°C
Junction Temp. ( $T_J$ ) with Power Applied . . . . .	-55 to 150°C . . . . .	-55 to 150°C

1. Stress above those listed under the Absolute Maximum Ratings may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied (while programming, following the programming specifications).
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of -2V to ( $V_{IH}$  (MAX)+2) volts is permitted for a duration of <20ns.
5. A maximum of 64 I/Os per device with  $V_{IN} > 3.6V$  is allowed.

## Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
$V_{CC}$	Supply Voltage for 1.8V Devices	1.65	1.95	V
	Supply Voltage for 2.5V Devices	2.3	2.7	V
	Supply Voltage for 3.3V Devices	3	3.6	V
$V_{CCP}$	Supply Voltage for PLL and sysHSI Blocks, 1.8V Devices	1.65	1.95	V
	Supply Voltage for PLL and sysHSI Blocks, 2.5V Devices	2.3	2.7	V
	Supply Voltage for PLL and sysHSI Blocks, 3.3V Devices	3	3.6	V
$V_{CCJ}$	Power Supply Voltage for JTAG Programming 1.8V Operation	1.65	1.95	V
	Power Supply Voltage for JTAG Programming 2.5V Operation	2.3	2.7	V
	Power Supply Voltage for JTAG Programming 3.3V Operation	3	3.6	V
$T_J$ (COM)	Junction Commercial Operation	0	90	°C
$T_J$ (IND)	Junction Industrial Operation	-40	105	°C

## Erase Reprogram Specifications

Parameter	Min	Max	Units
Erase/Reprogram Cycle	1,000	—	Cycles

Note: Valid over commercial temperature range.

## Hot Socketing Specifications<sup>1, 2, 3</sup>

Symbol	Parameter	Condition	Min	Typ	Max	Units
$I_{DK}$ <sup>4</sup>	Input or Tristated I/O Leakage Current	$0 \leq V_{IN} \leq 3.0V$	—	+/-50	+/-800	μA

1. Insensitive to sequence of  $V_{CC}$  and  $V_{CCO}$ . However, assumes monotonic rise/fall rates for  $V_{CC}$  and  $V_{CCO}$ , provided  $(V_{IN} - V_{CCO}) \leq 3.6V$ .
2. LVTTTL, LVCMOS only.
3.  $0 < V_{CC} \leq V_{CC} (MAX)$ ,  $0 < V_{CCO} \leq V_{CCO} (MAX)$ .
4.  $I_{DK}$  is additive to  $I_{PU}$ ,  $I_{PD}$  or  $I_{BH}$ . Device defaults to pull-up until fuse circuitry is active.

## DC Electrical Characteristics

### Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$I_{IL}, I_{IH}^1$	Input or I/O Low Leakage	$0 \leq V_{IN} \leq (V_{CCO} - 0.2V)$	—	—	10	$\mu A$
		$(V_{CCO} - 0.2V) < V_{IN} \leq 3.6V$	—	—	30	$\mu A$
$I_{IH}^3$	Input High Leakage Current	$3.6V < V_{IN} \leq 5.5V$ and $3.0V \leq V_{CCO} \leq 3.6V$	—	—	3	mA
$I_{PU}$	I/O Active Pull-up Current	$0 \leq V_{IN} \leq 0.7 V_{CCO}$	-30	—	-150	$\mu A$
$I_{PD}$	I/O Active Pull-down Current	$V_{IL} (MAX) \leq V_{IN} \leq V_{IH} (MAX)$	30	—	150	$\mu A$
$I_{BHLS}$	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL} (MAX)$	30	—	—	$\mu A$
$I_{BHHS}$	Bus Hold High Sustaining Current	$V_{IN} = 0.7 V_{CCO}$	-30	—	—	$\mu A$
$I_{BHLO}$	Bus Hold Low Overdrive Current	$0 \leq V_{IN} \leq V_{IH} (MAX)$	—	—	150	$\mu A$
$I_{BHLH}$	Bus Hold High Overdrive Current	$0 \leq V_{IN} \leq V_{IH} (MAX)$	—	—	-150	$\mu A$
$V_{BHT}$	Bus Hold Trip Points		$V_{CCO} * 0.35$	—	$V_{CCO} * 0.65$	V
$C_1$	I/O Capacitance <sup>2</sup>	$V_{CCO} = 3.3V, 2.5V, 1.8V$	—	8	—	pf
		$V_{CC} = 1.8V, V_{IO} = 0$ to $V_{IH} (MAX)$	—		—	
$C_2$	Clock Capacitance <sup>2</sup>	$V_{CCO} = 3.3V, 2.5V, 1.8V$	—	6	—	pf
		$V_{CC} = 1.8V, V_{IO} = 0$ to $V_{IH} (MAX)$	—		—	
$C_3$	Global Input Capacitance <sup>2</sup>	$V_{CCO} = 3.3V, 2.5V, 1.8V$	—	6	—	pf
		$V_{CC} = 1.8V, V_{IO} = 0$ to $V_{IH} (MAX)$	—		—	

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.

2.  $T_A = 25^\circ C$ ,  $f = 1.0MHz$ .

3. 5V tolerant inputs and I/Os should be placed in banks where  $3.0V \leq V_{CCO} \leq 3.6V$ . The JTAG ports are not included for the 5V tolerant interface.

## Supply Current

### Over Recommended Operating Conditions (ispGDX2-256)<sup>4</sup>

Symbol	Description	Power Pins	Vcc (V)	Min.	Typ.	Max.	Units
I <sub>CC</sub> <sup>1,2</sup>	Core Logic Power Supply Current	V <sub>CC</sub>	3.3	-	49.0	-	mA
			2.5	-	49.0	-	mA
			1.8	-	46.7	-	mA
	GPLL/sysHSI Logic Power Supply Current		3.3	-	118.7	-	mA
			2.5	-	118.7	-	mA
			1.8	-	117.5	-	mA
I <sub>CCP</sub> <sup>2</sup>	GPLL/sysHSI CSPLL Power Supply Current	V <sub>CCP</sub>	3.3	-	14.7	-	mA
			2.5	-	14.7	-	mA
			1.8	-	17.4	-	mA
I <sub>CCO</sub> <sup>3</sup>	Bank Power Supply Current	V <sub>CCO</sub>	3.3	-	35	-	mA
			2.5	-	35	-	mA
			1.8	-	25	-	mA
I <sub>CCJ</sub>	JTAG Programming Current	V <sub>CCJ</sub>	3.3	-	1.5	-	mA
			2.5	-	1.0	-	mA
			1.8	-	800	-	μA

1. 64-input switching frequency at 20 MHz, with one GRP fanout.

2. One GPLL with  $f_{VCO} = 400$  MHz and one sysHSI Block (two receivers and two transmitters) at 622 MHz data rate.

3. All 8-bank reference circuit currents, all I/Os in tristate, inputs held at valid logic levels, and bus maintenance circuits disabled.

4.  $T_A = 25^\circ C$

## sysIO Recommended Operating Conditions

Standard	V <sub>CCO</sub> (V) <sup>1</sup>			V <sub>REF</sub> (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVC MOS 3.3	3.0	3.3	3.6	-	-	-
LVC MOS 2.5	2.3	2.5	2.7	-	-	-
LVC MOS 1.8 <sup>2</sup>	1.65	1.8	1.95	-	-	-
LVTTL	3.0	3.3	3.6	-	-	-
PCI 3.3	3.0	3.3	3.6	-	-	-
PCI-X	3.0	3.3	3.6	-	-	-
AGP-1X	3.15	3.3	3.45	-	-	-
SSTL 2	2.3	2.5	2.7	1.15	1.25	1.35
SSTL 3	3.0	3.3	3.6	1.3	1.5	1.7
CTT 3.3	3.0	3.3	3.6	1.35	1.5	1.65
CTT 2.5	2.3	2.5	2.7	1.35	1.5	1.65
HSTL Class I	1.4	1.5	1.6	0.68	0.75	0.9
HSTL Class III	1.4	1.5	1.6	-	0.9	-
HSTL Class IV	1.4	1.5	1.6	-	0.9	-
GTL+	1.4	-	3.6	0.882	1.0	1.122
LVPECL	3.0	3.3	3.6	-	-	-
LVDS	2.3	2.5/3.3	3.6	-	-	-
BLVDS	2.3	2.5/3.3	3.6	-	-	-

1. Inputs are independent of V<sub>CCO</sub> setting. However, V<sub>CCO</sub> must be set within the valid operating range for one of the supported standards.

2. Software default setting.

## sysIO Single Ended DC Electrical Characteristics

### Over Recommended Operating Conditions

Input/Output Standard	$V_{IL}$		$V_{IH}$		$V_{OL}$ Max (V)	$V_{OH}$ Min (V)	$I_{OL}^2$ (mA)	$I_{OH}^2$ (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVCMOS 3.3	-0.3	0.8	2.0	5.5	0.4	2.4	20, 16, 12, 8, 5.33, 4	-20, -16, -12, -8, -5.33, -4
					0.2	$V_{CCO} - 0.2$	0.1	-0.1
LVTTTL	-0.3	0.8	2.0	5.5	0.4	2.4	4	-4
					0.2	$V_{CCO} - 0.2$	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	$V_{CCO} - 0.4$	16, 12, 8, 5.33, 4	-16, -12, -8, -5.33, -4
					0.2	$V_{CCO} - 0.2$	0.1	-0.1
LVCMOS 1.8 <sup>1,3</sup>	-0.3	0.68	1.07	3.6	0.4	$V_{CCO} - 0.4$	8	-8
LVCMOS 1.8 <sup>3</sup>	-0.3	0.68	1.07	3.6	0.4	$V_{CCO} - 0.4$	12, 5.33, 4	-12, -5.33, -4
					0.2	$V_{CCO} - 0.2$	0.1	-0.1
PCI 3.3 <sup>4</sup>	-0.3	1.08	1.5	3.6	$0.1 V_{CCO}$	$0.9 V_{CCO}$	1.5	-0.5
PCI -X <sup>5</sup>	-0.3	1.26	1.5	3.6	$0.1 V_{CCO}$	$0.9 V_{CCO}$	1.5	-0.5
AGP-1X <sup>4</sup>	-0.3	1.08	1.5	3.6	$0.1 V_{CCO}$	$0.9 V_{CCO}$	1.5	-0.5
SSTL3 class I	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.7	$V_{CCO} - 1.1$	8	-8
SSTL3 class II	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.5	$V_{CCO} - 0.9$	16	-16
SSTL2 class I	-0.3	$V_{REF} - 0.18$	$V_{REF} + 0.18$	3.6	0.54	$V_{CCO} - 0.62$	7.6	-7.6
SSTL2 class II	-0.3	$V_{REF} - 0.18$	$V_{REF} + 0.18$	3.6	0.35	$V_{CCO} - 0.43$	15.2	-15.2
CTT 3.3	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.4$	$V_{REF} + 0.4$	8	-8
CTT 2.5	-0.3	$V_{REF} - 0.3$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.4$	$V_{REF} + 0.4$	8	-8
HSTL class I	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	8	-8
HSTL class III	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	24	-8
HSTL class IV	-0.3	$V_{REF} - 0.3$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	48	-8
GTL+	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.6	n/a	36	n/a

1. Software default setting.

2. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank, as shown in the logic signals connection table, shall not exceed  $n \cdot 8\text{mA}$ . Where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.

3. For 1.8V devices (ispGDX2C) these specifications are  $V_{IL} = 0.35 V_{CC}$  and  $V_{IH} = 0.65 V_{CC}$

4. For 1.8V power supply devices these specifications are  $V_{IL} = 0.3 \cdot V_{CC} \cdot 3.3/1.8$ ,  $V_{IH} = 0.5 \cdot V_{CC} \cdot 3.3/1.8$

5. For 1.8V power supply devices these specifications are  $V_{IL} = 0.35 \cdot V_{CC} \cdot 3.3/1.8$  and  $V_{IH} = 0.5 \cdot V_{CC} \cdot 3.3/1.8$

## sysIO Differential DC Electrical Characteristics

### Over Recommended Operating Conditions

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
<b>LVDS</b>						
$V_{INP} V_{INM}$	Input Voltage	—	0	—	2.4	V
$V_{THD}$	Differential Input Threshold	—	+/-100	—	—	mV
$V_{CM}$	Input Common Mode Voltage	Half the Sum of the Two Inputs	0.05	—	2.35	V
$I_{IN}$	Input Current	Power On or Power Off	—	—	+/-10	uA
$V_{OH}$	Output High Voltage for $V_{OP}$ or $V_{OM}$	$R_T = 100\Omega$	—	1.38	1.60	V
$V_{OL}$	Output Low Voltage for $V_{OP}$ or $V_{OM}$	$R_T = 100\Omega$	0.9	1.03	—	V
$V_{OD}$	Output Voltage Differential	$(V_{OP} - V_{OM})$ , $R_T = 100\Omega$	250	350	450	mV
$\Delta V_{OD}$	Change in $V_{OD}$ Between High and Low	—	—	—	50	mV
$V_{OS}$	Output Voltage Offset	$(V_{OP} - V_{OM})/2$ , $R_T = 100\Omega$	1.125	1.25	1.375	V
$\Delta V_{OS}$	Change in $V_{OS}$ Between H and L	—	—	—	50	mV
$I_{OSD}$	Output Short Circuit Current	$V_{OD} = 0V$ . Driver Outputs Shorted.	—	—	24	mA
<b>Bus LVDS<sup>1</sup></b>						
$V_{OH}$	Output High Voltage for $V_{OP}$ or $V_{OM}$	$R_T = 27\Omega$	—	1.4	1.80	V
$V_{OL}$	Output Low Voltage for $V_{OP}$ or $V_{OM}$	$R_T = 27\Omega$	0.95	1.1	—	V
$V_{OD}$	Output Voltage Differential	$ V_{OP} - V_{OM} $ , $R_T = 27\Omega$	240	300	460	mV
$\Delta V_{OD}$	Change in $V_{OD}$ Between H and L	—	—	—	27	mV
$V_{OS}$	Output Voltage Offset	$ V_{OP} - V_{OM} /2$ , $R_T = 27\Omega$	1.1	1.3	1.5	V
$\Delta V_{OS}$	Change in $V_{OS}$ Between H and L	—	—	—	27	mV
$I_{OSD}$	Output Short Circuit Current	$V_{OD} = 0$ . Driver Outputs Shorted.	—	36	65	mA

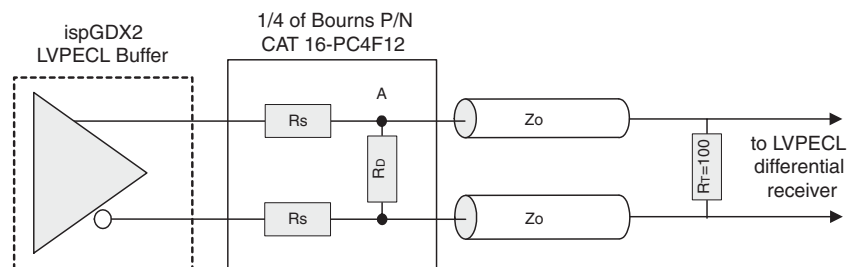
1.  $V_{OP}$  and  $V_{OM}$  are the two outputs of the LVDS output buffer.

### LVPECL<sup>1</sup>

DC Parameter	Parameter Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
$V_{CCO}$	Output Supply Voltage	3.0		3.3		3.6		V
$V_{IH}$	Input Voltage High	1.49	2.72	1.49	2.72	1.49	2.72	V
$V_{IL}$	Input Voltage Low	0.86	2.125	0.86	2.125	0.86	2.125	V
$V_{OH}$	Output Voltage High	1.7	2.11	1.92	2.28	2.03	2.41	V
$V_{OL}$	Output Voltage Low	0.96	1.27	1.06	1.43	1.25	1.57	V
$V_{DIFF}$	Differential Input voltage	0.3		0.3		0.3		V

1. These values are valid at the output of the source termination pack as shown above with 100-ohm differential load only (see Figure 15).  
The  $V_{OH}$  levels are 200mV below the standard LVPECL levels and are compatible with devices tolerant of the lower common mode ranges.

**Figure 15. LVPECL Driver with Three Resistor Pack**





## ispGDX2-256 External Switching Characteristics

### Over Recommended Operating Conditions

Parameter	Description	-3.5		-5		Units
		Min	Max	Min	Max	
Output Paths						
t <sub>PD</sub>	Data From Input Pin to Output Pin	—	3.5	—	5.0	ns
t <sub>PD_SEL</sub>	Data From Global Select Pin to Output Pin	—	3.3	—	4.7	ns
t <sub>CO</sub>	Global Clock to Output	—	3.2	—	5.4	ns
t <sub>OPS</sub>	Set-up Time Before Global Clock	2.0	—	3.0	—	ns
t <sub>OPH</sub>	Hold Time After Global Clock	0.0	—	0.0	—	ns
t <sub>OPCES</sub>	PT Clock Enable Setup time before Global Clock	4.1	—	6.9	—	ns
t <sub>OPCEH</sub>	PT Clock Enable Hold time after Global Clock	0.0	—	0.0	—	ns
t <sub>OPRSTO</sub>	External Reset Pin to Output Delay	—	6.0	—	10.0	ns
Input Paths						
t <sub>IPS</sub>	Set-up Time Before Global Clock	0.5	—	0.9	—	ns
t <sub>IPSZ</sub>	Set-up Time Before Global Clock (Zero Hold Time)	2.0	—	3.0	—	ns
t <sub>IPH</sub>	Hold Time After Global Clock	1.0	—	1.7	—	ns
t <sub>IPHZ</sub>	Hold Time After Global Clock (Zero Hold Time)	0.0	—	0.0	—	ns
t <sub>IPCES</sub>	PT Clock Enable Setup time before Global Clock	3.1	—	5.1	—	ns
t <sub>IPCEH</sub>	PT Clock Enable Hold time after Global Clock	0.0	—	0.0	—	ns
t <sub>IPRSTO</sub>	External Reset Pin to Output Delay	—	7.5	—	12.5	ns
Output Enable Paths						
t <sub>OECO</sub>	Global Clock to Output Enabled Pin	—	5.5	—	9.1	ns
t <sub>OES</sub>	Output Enable Register Set-up Time Before Global Clock	1.6	—	2.7	—	ns
t <sub>OEH</sub>	Hold Time After Global Clock	0.0	—	0.0	—	ns
t <sub>OECES</sub>	PT Clock Enable Setup time before Global Clock	4.1	—	6.9	—	ns
t <sub>OECEH</sub>	PT Clock Enable Hold time after Global Clock	0.0	—	0.0	—	ns
t <sub>GOE/DIS</sub>	Global OE Input to Output Enable/Disable	—	4.5	—	7.5	ns
t <sub>TOE/DIS</sub>	Test OE Input to Output Enable/Disable	—	6.2	—	10.3	ns
t <sub>EN/DIS</sub>	Input to Output Enable/Disable	—	6.2	—	10.3	ns
Clock and Reset Paths						
t <sub>RW</sub>	Width of Reset Pulse	—	2.5	—	4.1	ns
t <sub>CW</sub>	Clock Width	—	1.65	—	2.75	ns
t <sub>GW</sub>	Clock Width	—	1.65	—	2.75	ns
f <sub>MAX</sub> (Ext)	Clock Frequency with External Feedback 1/(t <sub>OPS</sub> + t <sub>CO</sub> )	—	190	—	115	MHz
f <sub>MAX</sub> (Tog, No PLL)	Clock Frequency Maximum Toggle (No PLL)	—	300	—	180	MHz
f <sub>MAX</sub> (Tog, PLL)	Clock Frequency Maximum Toggle (With PLL)	—	300	—	180	MHz

Timing v.1.0

## Timing Model

The task of determining the timing through the ispGDX2 family is relatively simple. The timing model provided in Figure 16 shows the specific delay paths. Once the implementation of a given function is determined either conceptually or from the software report file, the delay path of the function can easily be determined from the timing model. The Lattice design tools report the timing delays based on the same timing model for a particular design. Note that the internal timing parameters are given for reference only, and are not tested. The external timing parameters are tested and guaranteed for every device.

**Figure 16. ispGDX2 Timing Model Diagram (I/O Cell)**

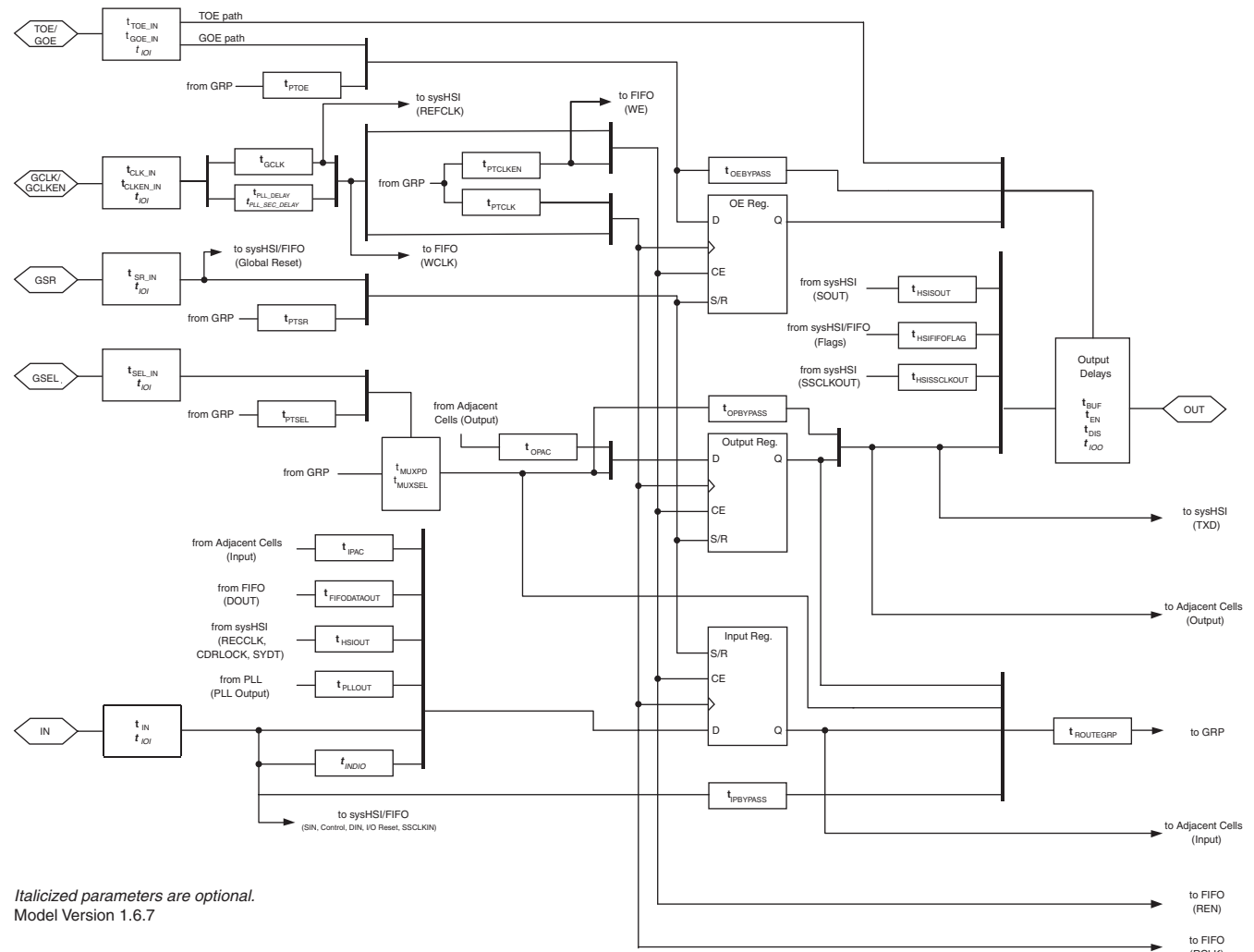


Figure 17. ispGDX2 Timing Model Diagram (with sysHSI and FIFO Receive Mode)

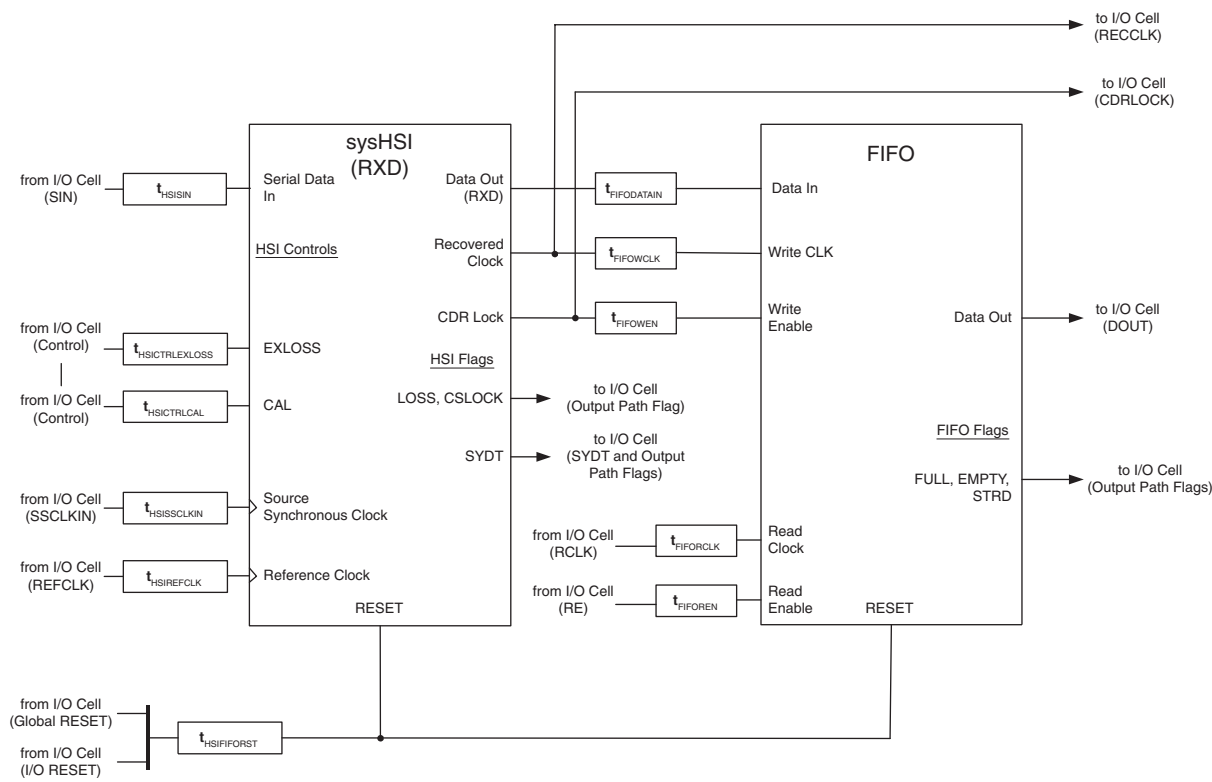


Figure 18. ispGDX2 Timing Model Diagram (with sysHSI Transmit Mode)

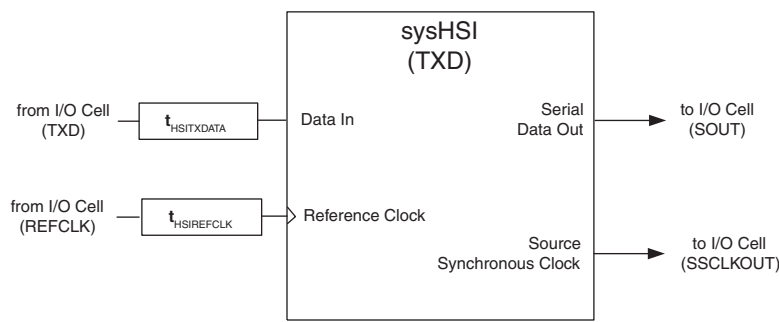
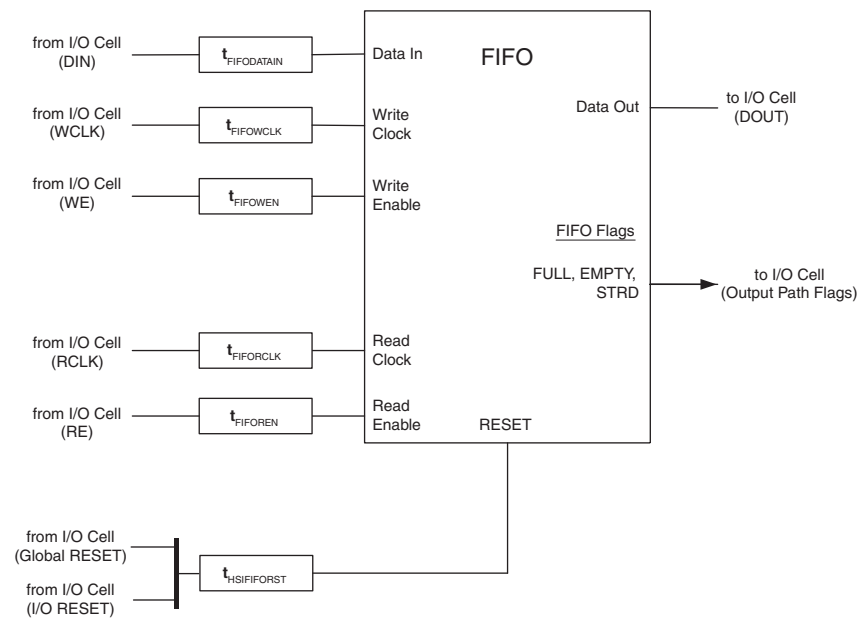


Figure 19. ispGDX2 Timing Model Diagram (in FIFO Only Mode)



## Sample External Timing Calculations

The following equations illustrate the task of determining the timing through the ispGDX2 family. These are only a sample of equations to calculate the timing through the ispGDX2.

Figure 16 shows the specific delay paths and the Internal Timing Parameters table provides the parameter values. Note that the internal timing parameters are given for reference only and are not tested. The external timing parameters are tested and guaranteed for every device.

Data from global select pin to output pin:

$$t_{PD\_SEL} = t_{SEL\_IN} + t_{MUXSEL} + t_{OPBYPASS} + t_{BUF}$$

Global clock to output:

$$t_{CO} = t_{CLK\_IN} + t_{GCLK} + t_{OPCOi} + t_{BUF}$$

Input register or latch set-up time before global clock:

$$t_{IPS} = t_{IN} + t_{IPS} - (t_{CLK} + t_{GCLK})$$

Input register or latch hold time after global clock:

$$t_{IPH} = (t_{CLK\_IN} + t_{GCLK}) + t_{IPHi} - t_{IN}$$

Data from product term select to output pin:

$$t_{PD\_PTSEL} = t_{IN} + t_{IPBYPASS} + t_{ROUTEGRP} + t_{PTSEL} + t_{MUXSEL} + t_{OPBYPASS} + t_{BUF}$$

Product term clock to output:

$$t_{CO\_PT} = t_{IN} + t_{IPBYPASS} + t_{ROUTEGRP} + t_{PTCLK} + t_{OPCOi} + t_{BUF}$$

Input register or latch set-up time before product term clock:

$$t_{IPS\_PT} = t_{IN} + t_{IPSi\_PT} - (t_{IN} + t_{IPBYPASS} + t_{ROUTEGRP} + t_{PTCLK})$$

Input register or latch hold time after product term clock:

$$t_{IPH\_PT} = (t_{IN} + t_{IPBYPASS} + t_{ROUTEGRP} + t_{PTCLK}) + t_{IPHi} - t_{IN}$$

Global OE input to output enable/disable:

$$t_{GOE/DIS} = t_{GOE\_IN} + t_{OEBYPASS} + t_{EN}$$

External reset pin to output delay:

$$t_{OPRSTO} = t_{SR\_IN} + t_{OPASROi} + t_{BUF}$$

**ispGDX2-256 Internal Timing Parameters<sup>1</sup>****Over Recommended Operating Conditions**

Parameter	Description	-3.5		-5		Units
		Min.	Max.	Min.	Max.	
Input/Output Delays						
t <sub>BUF</sub>	Output Buffer Delay	—	0.80	—	1.14	ns
t <sub>CLK_IN</sub>	Global Clock Input Delay	—	1.00	—	1.67	ns
t <sub>CLKEN_IN</sub>	Global Clock Enable Input Delay	—	1.80	—	3.00	ns
t <sub>DIS</sub>	Output Disable Delay	—	2.50	—	4.17	ns
t <sub>EN</sub>	Output Enable Delay	—	2.50	—	4.17	ns
t <sub>GOE_IN</sub>	Global Output Enable Path Delay	—	2.00	—	3.33	ns
t <sub>IN</sub>	Input Pin Delay	—	0.40	—	0.57	ns
t <sub>SEL_IN</sub>	Global MUX Select Input Delay	—	1.60	—	2.29	ns
t <sub>SR_IN</sub>	Global Set/Reset Path Delay	—	2.70	—	4.50	ns
t <sub>TOE_IN</sub>	Test Output Enable Path Delay	—	3.70	—	6.17	ns
Register Latch Delays, Output Paths						
t <sub>OPASROi</sub>	Asynchronous Set/Reset to Output	—	2.50	—	4.17	ns
t <sub>OPASRRi</sub>	Asynchronous Set/Reset Recovery	—	2.50	—	4.17	ns
t <sub>OPBYPASS</sub>	Register/Latch Bypass Delay	—	0.50	—	0.71	ns
t <sub>OPCEHi</sub>	Register Clock Enable Hold Time	1.30	—	2.17	—	ns
t <sub>OPCESi</sub>	Register Clock Enable Setup Time (Global Clock Enable)	1.10	—	1.83	—	ns
t <sub>OPCESi_PT</sub>	Register Clock Enable Setup Time (Product Term Clock Enable)	2.10	—	3.50	—	ns
t <sub>OPCOi</sub>	Register Clock to Output Delay	—	1.00	—	1.67	ns
t <sub>OPHi</sub>	Register Hold Time	0.80	—	1.33	—	ns
t <sub>OPLGOi</sub>	Latch Gate to Output Delay	—	1.00	—	1.67	ns
t <sub>OPLHi</sub>	Latch Hold Time	0.80	—	1.33	—	ns
t <sub>OPLPDi</sub>	Latch Propagation Delay (Transparent Mode)	—	0.30	—	0.50	ns
t <sub>OPLSi</sub>	Latch Setup Time (Global Gate)	1.00	—	1.67	—	ns
t <sub>OPLSi_PT</sub>	Latch Setup Time (Product Term Gate)	1.00	—	1.67	—	ns
t <sub>OPSi</sub>	Register Setup Time (Global Clock)	1.20	—	2.00	—	ns
t <sub>OPSi_PT</sub>	Register Setup Time (Product Term Clock)	1.00	—	1.67	—	ns
t <sub>OPSRPWi</sub>	Asynchronous Set/Reset Pulse Width	—	2.50	—	4.17	ns
Register Latch Delays, Input Paths						
t <sub>IPASROi</sub>	Asynchronous Set/Reset to Output	—	1.70	—	2.83	ns
t <sub>IPASRRi</sub>	Asynchronous Set/Reset Recovery	—	2.50	—	4.17	ns
t <sub>IPBYPASS</sub>	Register/Latch Bypass Delay	—	0.00	—	0.00	ns
t <sub>IPCEHi</sub>	Register Clock Enable Hold Time	1.30	—	2.17	—	ns
t <sub>IPCESi</sub>	Register Clock Enable Setup Time (Global Clock Enable)	1.10	—	1.83	—	ns
t <sub>IPCESi_PT</sub>	Register Clock Enable Setup Time (Product Term Clock Enable)	1.10	—	1.83	—	ns
t <sub>IPCOi</sub>	Register Clock to Output Delay	—	1.00	—	1.67	ns
t <sub>IPHi</sub>	Register Hold Time	0.00	—	0.00	—	ns
t <sub>IPLGOi</sub>	Latch Gate to Output Delay	—	1.00	—	1.67	ns
t <sub>IPLHi</sub>	Latch Hold Time	0.00	—	0.00	—	ns
t <sub>IPLPDi</sub>	Latch Propagation Delay (Transparent Mode)	—	0.30	—	0.50	ns
t <sub>IPLSi</sub>	Latch Setup Time (Global Term)	1.50	—	2.50	—	ns
t <sub>IPLSi_PT</sub>	Latch Setup Time (Product Term Gate)	1.50	—	2.50	—	ns

## ispGDX2-256 Internal Timing Parameters<sup>1</sup> (Continued)

Over Recommended Operating Conditions

Parameter	Description	-3.5		-5		Units
		Min.	Max.	Min.	Max.	
t <sub>IPSi</sub>	Register Setup Time (Global Clock)	1.50	—	2.50	—	ns
t <sub>IPSL_PT</sub>	Register Setup Time (Product Term Clock)	1.50	—	2.50	—	ns
t <sub>IPSRPW<sub>i</sub></sub>	Asynchronous Set/Reset Pulse Width	—	2.50	—	4.17	ns
<b>OE Path</b>						
t <sub>OEASROi</sub>	Asynchronous Set/Reset to Output	—	2.50	—	4.17	ns
t <sub>OEASRRi</sub>	Asynchronous Set/Reset Recovery	—	2.50	—	4.17	ns
t <sub>OEByPASS</sub>	Register/Latch Bypass Delay	—	0.00	—	0.00	ns
t <sub>OECEHi</sub>	Register Clock Enable Hold Time	0.80	—	1.33	—	ns
t <sub>OECESi</sub>	Register Clock Enable Setup Time (Global Clock Enable)	1.20	—	2.00	—	ns
t <sub>OECESi_PT</sub>	Register Clock Enable Setup Time (Product Term Clock Enable)	2.10	—	3.50	—	ns
t <sub>OECo<sub>i</sub></sub>	Register Clock to Output Delay	—	1.60	—	2.67	ns
t <sub>OEHi</sub>	Register Hold Time	0.40	—	0.67	—	ns
t <sub>OE<sub>LG</sub>o<sub>i</sub></sub>	Latch Gate to Output Delay	—	1.60	—	2.67	ns
t <sub>OE<sub>LH</sub>i</sub>	Latch Hold Time	0.40	—	0.67	—	ns
t <sub>OE<sub>LP</sub>Di</sub>	Latch Propagation Delay (Transparent Mode)	—	0.30	—	0.50	ns
t <sub>OE<sub>LS</sub>i</sub>	Latch Setup Time (Global Gate)	1.00	—	1.67	—	ns
t <sub>OE<sub>LS</sub>i_PT</sub>	Latch Setup Time (Product Term Gate)	1.00	—	1.67	—	ns
t <sub>OESi</sub>	Register Setup Time (Global Clock)	1.00	—	1.67	—	ns
t <sub>OESi_PT</sub>	Register Setup Time (Product Term Clock)	1.00	—	1.67	—	ns
t <sub>OESRPW<sub>i</sub></sub>	Asynchronous Set/Reset Pulse Width	—	2.50	—	4.17	ns
<b>Shift Register and MUX Delays</b>						
t <sub>IPAC</sub>	Input Path Adjacent I/O Cell Delay (Shift Register)	—	0.80	—	1.33	ns
t <sub>OPAC</sub>	Output Path Adjacent I/O Cell Delay (Shift Register)	—	1.30	—	2.17	ns
t <sub>MUXPD</sub>	MUX Data Path Delay	—	0.90	—	1.29	ns
t <sub>MUXSEL</sub>	MUX Select Path Delay	—	0.40	—	0.57	ns
<b>AND Arrays and Routing Delays</b>						
t <sub>FIFO<sub>DATA</sub>OUT</sub>	FIFO Output to I/O Block Delay	—	0.00	—	0.00	ns
t <sub>GCLK</sub>	Clock Tree Delay	—	0.40	—	0.67	ns
t <sub>HSI<sub>FIFO</sub>FLAG</sub>	HSI/FIFO Flag to I/O Block Delay	—	0.00	—	0.00	ns
t <sub>HSI<sub>OUT</sub></sub>	HSI Output to I/O Cell Block Delay	—	0.00	—	0.00	ns
t <sub>HSI<sub>SS</sub>CLK<sub>OUT</sub></sub>	HSI Source Synchronous Clock to I/O Cell Block Delay	—	0.00	—	0.00	ns
t <sub>PLLOUT</sub>	PLL Output to I/O Cell Block Delay	—	0.00	—	0.00	ns
t <sub>PLL_DELAY</sub> <sup>2</sup>	PLL Delay Increment(User Selectable)	—	0.33	—	0.90	ns
t <sub>PTCLK</sub>	Clock AND Array Delay	—	2.20	—	3.67	ns
t <sub>PTCLKEN</sub>	Clock Enable AND Array Delay	—	2.10	—	3.50	ns
t <sub>PTOE</sub>	OE AND Array Delay	—	2.40	—	4.00	ns
t <sub>PTSEL</sub>	Select AND Array Delay	—	1.70	—	2.83	ns
t <sub>PTSR</sub>	Set/Reset AND Array Delay	—	2.70	—	4.50	ns
t <sub>ROUTE<sub>GRP</sub></sub>	Global Routing Pool Delay	—	0.90	—	1.50	ns

Timing v.1.0

1. Internal timing parameters are not tested and are for reference only. Refer to the timing model in this data sheet for details.
2. t<sub>PLL\_DELAY</sub> is the unit of increment by which the clock signal can be incremented. The PLL can adjust the clock signal by up to t<sub>RANGE</sub> (as given in the sysCLOCK PLL timing section) in either direction in steps of size t<sub>PLL\_DELAY</sub>.

## ispGDX2 Family Timing Adjusters

Parameter	Description	Base Parameter	-3.5		-5		Units
			Min.	Max.	Min.	Max.	
Optional Adders							
t <sub>INDIO</sub>	Input Delay	—	—	1.50	—	2.50	ns
t <sub>PLL_SEC_DELAY</sub>	Secondary PLL Output Delay	t <sub>PLL_DELAY</sub>	—	1.30	—	1.30	ns
t <sub>IOI</sub> Input Adjusters							
LVTTTL_in	Using 3.3V TTL	t <sub>IN</sub> , t <sub>CLK_IN</sub> , t <sub>CLKEN_IN</sub> , t <sub>SEL_IN</sub> , t <sub>GOE_IN</sub> , t <sub>SR_IN</sub>	—	0.00	—	0.00	ns
LVC MOS_18_in	Using 1.8V CMOS	t <sub>IN</sub> , t <sub>CLK_IN</sub> , t <sub>CLKEN_IN</sub> , t <sub>SEL_IN</sub> , t <sub>GOE_IN</sub> , t <sub>SR_IN</sub>	—	0.00	—	0.00	ns
LVC MOS_25_in	Using 2.5V CMOS	t <sub>IN</sub> , t <sub>CLK_IN</sub> , t <sub>CLKEN_IN</sub> , t <sub>SEL_IN</sub> , t <sub>GOE_IN</sub> , t <sub>SR_IN</sub>	—	0.00	—	0.00	ns
LVC MOS_33_in	Using 3.3V CMOS	t <sub>IN</sub> , t <sub>CLK_IN</sub> , t <sub>CLKEN_IN</sub> , t <sub>SEL_IN</sub> , t <sub>GOE_IN</sub> , t <sub>SR_IN</sub>	—	0.00	—	0.00	ns
AGP_1X_in	Using AGP 1x	t <sub>IN</sub> , t <sub>CLK_IN</sub> , t <sub>CLKEN_IN</sub> , t <sub>SEL_IN</sub> , t <sub>GOE_IN</sub> , t <sub>SR_IN</sub>	—	1.00	—	1.00	ns
BLVDS_in	Using Bus Low Voltage Differential Signaling (BLVDS)	t <sub>IN</sub> , t <sub>CLK_IN</sub> , t <sub>CLKEN_IN</sub> , t <sub>SEL_IN</sub> , t <sub>GOE_IN</sub> , t <sub>SR_IN</sub>	—	0.50	—	0.50	ns
CTT25_in	Using CTT 2.5V	t <sub>IN</sub> , t <sub>CLK_IN</sub> , t <sub>CLKEN_IN</sub> , t <sub>SEL_IN</sub> , t <sub>GOE_IN</sub> , t <sub>SR_IN</sub>	—	1.00	—	1.00	ns
CTT33_in	Using CTT 3.3V	t <sub>IN</sub> , t <sub>CLK_IN</sub> , t <sub>CLKEN_IN</sub> , t <sub>SEL_IN</sub> , t <sub>GOE_IN</sub> , t <sub>SR_IN</sub>	—	1.00	—	1.00	ns
GTL+_in	Using GTL+	t <sub>IN</sub> , t <sub>CLK_IN</sub> , t <sub>CLKEN_IN</sub> , t <sub>SEL_IN</sub> , t <sub>GOE_IN</sub> , t <sub>SR_IN</sub>	—	0.50	—	0.50	ns
HSTL_I_in	Using HSTL 2.5V, Class I	t <sub>IN</sub> , t <sub>CLK_IN</sub> , t <sub>CLKEN_IN</sub> , t <sub>SEL_IN</sub> , t <sub>GOE_IN</sub> , t <sub>SR_IN</sub>	—	0.50	—	0.50	ns
HSTL_III_in	Using HSTL 2.5V, Class III	t <sub>IN</sub> , t <sub>CLK_IN</sub> , t <sub>CLKEN_IN</sub> , t <sub>SEL_IN</sub> , t <sub>GOE_IN</sub> , t <sub>SR_IN</sub>	—	0.60	—	0.60	ns
HSTL_IV_in	Using HSTL 2.5V, Class IV	t <sub>IN</sub> , t <sub>CLK_IN</sub> , t <sub>CLKEN_IN</sub> , t <sub>SEL_IN</sub> , t <sub>GOE_IN</sub> , t <sub>SR_IN</sub>	—	0.60	—	0.60	ns
LVPECL_in	Using Differential Signaling (LVPECL)	t <sub>IN</sub> , t <sub>CLK_IN</sub> , t <sub>CLKEN_IN</sub>	—	0.00	—	0.00	ns
LVDS_in	Using Low Voltage Differential Signaling (LVDS)	t <sub>IN</sub> , t <sub>CLK_IN</sub> , t <sub>CLKEN_IN</sub>	—	0.50	—	0.50	ns
PCI_in	Using PCI	t <sub>IN</sub> , t <sub>CLK_IN</sub> , t <sub>CLKEN_IN</sub> , t <sub>SEL_IN</sub> , t <sub>GOE_IN</sub> , t <sub>SR_IN</sub>	—	1.00	—	1.00	ns
PCI_X_in	Using PCI-X	t <sub>IN</sub> , t <sub>CLK_IN</sub> , t <sub>CLKEN_IN</sub> , t <sub>SEL_IN</sub> , t <sub>GOE_IN</sub> , t <sub>SR_IN</sub>	—	1.00	—	1.00	ns
SSTL2_I_in	Using SSTL 2.5V, Class I	t <sub>IN</sub> , t <sub>CLK_IN</sub> , t <sub>CLKEN_IN</sub> , t <sub>SEL_IN</sub> , t <sub>GOE_IN</sub> , t <sub>SR_IN</sub>	—	0.50	—	0.50	ns
SSTL2_II_in	Using SSTL 2.5V, Class II	t <sub>IN</sub> , t <sub>CLK_IN</sub> , t <sub>CLKEN_IN</sub> , t <sub>SEL_IN</sub> , t <sub>GOE_IN</sub> , t <sub>SR_IN</sub>	—	0.50	—	0.50	ns
SSTL3_I_in	Using SSTL 3.3V, Class I	t <sub>IN</sub> , t <sub>CLK_IN</sub> , t <sub>CLKEN_IN</sub> , t <sub>SEL_IN</sub> , t <sub>GOE_IN</sub> , t <sub>SR_IN</sub>	—	0.60	—	0.60	ns
SSTL3_II_in	Using SSTL 3.3V, Class II	t <sub>IN</sub> , t <sub>CLK_IN</sub> , t <sub>CLKEN_IN</sub> , t <sub>SEL_IN</sub> , t <sub>GOE_IN</sub> , t <sub>SR_IN</sub>	—	0.60	—	0.60	ns
t <sub>IOO</sub> Output Adjusters							
Slow Slew	Using Slow Slew (LVTTTL and LVC MOS Outputs Only)	t <sub>BUF</sub> t <sub>EN</sub>	—	0.90	—	0.90	ns
LVTTTL_out	Using 3.3V TTL Drive	t <sub>BUF</sub> t <sub>EN</sub> , t <sub>DIS</sub>	—	1.20	—	1.20	ns
LVC MOS_18_4mA_out	Using 1.8V CMOS Standard, 4mA Drive	t <sub>BUF</sub> t <sub>EN</sub> , t <sub>DIS</sub>	—	0.30	—	0.30	ns



**ispGDX2 Family Timing Adjusters (Continued)**

Parameter	Description	Base Parameter	-3.5		-5		Units
			Min.	Max.	Min.	Max.	
LVCMOS_18_5.33mA_out	Using 1.8V CMOS Standard, 5.33mA Drive	$t_{BUF}$ , $t_{EN}$ , $t_{DIS}$	—	0.30	—	0.30	ns
LVCMOS_18_8mA_out	Using 1.8V CMOS Standard, 8mA Drive	$t_{BUF}$ , $t_{EN}$ , $t_{DIS}$	—	0.00	—	0.00	ns
LVCMOS_18_12mA_out	Using 1.8V CMOS Standard, 12mA Drive	$t_{BUF}$ , $t_{EN}$ , $t_{DIS}$	—	0.00	—	0.00	ns
LVCMOS_25_4mA_out	Using 2.5V CMOS Standard, 4mA Drive	$t_{BUF}$ , $t_{EN}$ , $t_{DIS}$	—	1.20	—	1.20	ns
LVCMOS_25_5.33mA_out	Using 2.5V CMOS Standard, 5.33mA Drive	$t_{BUF}$ , $t_{EN}$ , $t_{DIS}$	—	1.00	—	1.00	ns
LVCMOS_25_8mA_out	Using 2.5V CMOS Standard, 8mA Drive	$t_{BUF}$ , $t_{EN}$ , $t_{DIS}$	—	0.40	—	0.40	ns
LVCMOS_25_12mA_out	Using 2.5V CMOS Standard, 12mA Drive	$t_{BUF}$ , $t_{EN}$ , $t_{DIS}$	—	0.40	—	0.40	ns
LVCMOS_25_16mA_out	Using 2.5V CMOS Standard, 16mA Drive	$t_{BUF}$ , $t_{EN}$ , $t_{DIS}$	—	0.40	—	0.40	ns
LVCMOS_33_4mA_out	Using 3.3V CMOS Standard, 4mA Drive	$t_{BUF}$ , $t_{EN}$ , $t_{DIS}$	—	1.20	—	1.20	ns
LVCMOS_33_5.33mA_out	Using 3.3V CMOS Standard, 5.33mA Drive	$t_{BUF}$ , $t_{EN}$ , $t_{DIS}$	—	1.20	—	1.20	ns
LVCMOS_33_8mA_out	Using 3.3V CMOS Standard, 8mA Drive	$t_{BUF}$ , $t_{EN}$ , $t_{DIS}$	—	0.80	—	0.80	ns
LVCMOS_33_12mA_out	Using 3.3V CMOS Standard, 12mA Drive	$t_{BUF}$ , $t_{EN}$ , $t_{DIS}$	—	0.60	—	0.60	ns
LVCMOS_33_16mA_out	Using 3.3V CMOS Standard, 16mA Drive	$t_{BUF}$ , $t_{EN}$ , $t_{DIS}$	—	0.60	—	0.60	ns
LVCMOS_33_20mA_out	Using 3.3V CMOS Standard, 20mA Drive	$t_{BUF}$ , $t_{EN}$ , $t_{DIS}$	—	0.30	—	0.30	ns
AGP_1X_out	Using AGP 1x Standard	$t_{BUF}$ , $t_{EN}$ , $t_{DIS}$	—	0.60	—	0.60	ns
BLVDS_out	Using Bus Low Voltage Differential Signaling (BLVDS)	$t_{BUF}$ , $t_{EN}$ , $t_{DIS}$	—	1.00	—	1.00	ns
CTT25_out	Using CTT 2.5v	$t_{BUF}$ , $t_{EN}$ , $t_{DIS}$	—	0.30	—	0.30	ns
CTT33_out	Using CTT 3.3v	$t_{BUF}$ , $t_{EN}$ , $t_{DIS}$	—	0.20	—	0.20	ns
GTL+_out	Using GTL+	$t_{BUF}$ , $t_{EN}$ , $t_{DIS}$	—	0.50	—	0.50	ns
HSTL_I_out	Using HSTL 2.5V, Class I	$t_{BUF}$ , $t_{EN}$ , $t_{DIS}$	—	0.50	—	0.50	ns
HSTL_III_out	Using HSTL 2.5V, Class III	$t_{BUF}$ , $t_{EN}$ , $t_{DIS}$	—	0.60	—	0.60	ns
HSTL_IV_out	Using HSTL 2.5V, Class IV	$t_{BUF}$ , $t_{EN}$ , $t_{DIS}$	—	0.60	—	0.60	ns
LVPECL_out	Using LVPECL Differential Signaling	$t_{BUF}$ , $t_{EN}$ , $t_{DIS}$	—	0.30	—	0.30	ns
LVDS_out	Using Low Voltage Differential Signaling (LVDS)	$t_{BUF}$ , $t_{EN}$ , $t_{DIS}$	—	0.80	—	0.80	ns
PCI_out	Using PCI Standard	$t_{BUF}$ , $t_{EN}$ , $t_{DIS}$	—	0.60	—	0.60	ns
PCI_X_out	Using PCI-X Standard	$t_{BUF}$ , $t_{EN}$ , $t_{DIS}$	—	0.60	—	0.60	ns
SSTL2_I_out	Using SSTL 2.5V, Class I	$t_{BUF}$ , $t_{EN}$ , $t_{DIS}$	—	0.30	—	0.30	ns
SSTL2_II_out	Using SSTL 2.5V, Class II	$t_{BUF}$ , $t_{EN}$ , $t_{DIS}$	—	0.50	—	0.50	ns
SSTL3_I_out	Using SSTL 3.3V, Class I	$t_{BUF}$ , $t_{EN}$ , $t_{DIS}$	—	0.20	—	0.20	ns
SSTL3_II_out	Using SSTL 3.3V, Class II	$t_{BUF}$ , $t_{EN}$ , $t_{DIS}$	—	0.40	—	0.40	ns

Timing v.1.0

## FIFO Internal Timing

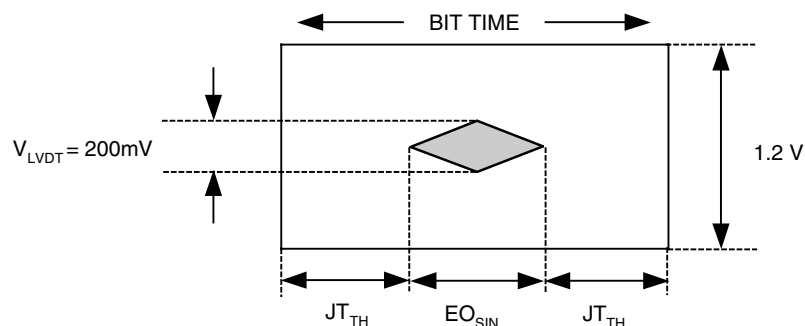
Parameter	Description	-3.5		-5		Units
		Min.	Max.	Min.	Max.	
Routing Delays						
$t_{FIFODATAIN}$	FIFO Input Delay	—	0.00	—	0.00	ns
$t_{FIFODATAOUT}$	FIFO Output to I/O Core Delay	—	0.00	—	0.00	ns
$t_{FIFORCLK}$	Read Clock Input Delay	—	0.00	—	0.00	ns
$t_{FIFOREN}$	Read Clock Enable Input Delay	—	0.00	—	0.00	ns
$t_{FIFOWCLK}$	Write Clock Input Delay	—	0.00	—	0.00	ns
$t_{FIFOWEN}$	Write Clock Enable Input Delay	—	0.00	—	0.00	ns
Core Delays						
$t_{FIFOCLKSKEW}$	Opposite Clock Cycle Time	—	2.00	—	3.33	ns
$t_{FIFOEMPTY}$	Read Clock to Empty Flag Delay	—	1.80	—	3.00	ns
$t_{FIFOFULL}$	Write Clock to Full Flag Delay	—	1.80	—	3.00	ns
$t_{FIFORCEH}$	Read Clock Hold after Read Clock Enable Time	—	0.00	—	0.00	ns
$t_{FIFORCES}$	Read Clock Setup before Read Clock Enable Time	—	1.50	—	2.50	ns
$t_{FIFORCLKO}$	Read Clock to FIFO Out Delay	—	0.50	—	0.83	ns
$t_{FIFORSTO}$	Reset to Output Delay	—	0.70	—	1.17	ns
$t_{FIFORSTPW}$	Reset Pulse Width	—	2.00	—	3.33	ns
$t_{FIFORSTR}$	Reset Recovery Time	—	2.00	—	3.33	ns
$t_{FIFOSTRD}$	Write Clock to Start Read Flag Delay	—	0.00	—	0.00	ns
$t_{FIFOTHRU}$	Flow Through Delay	—	0.00	—	0.00	ns
$t_{FIFOWCEH}$	Write Clock hold after Write Clock Enable Time	—	2.00	—	3.33	ns
$t_{FIFOWCES}$	Write Clock Setup before Write Clock Enable Time	—	0.00	—	0.00	ns
$t_{FIFOWCLKH}$	Write Data Hold after Write Clock Time	—	0.70	—	1.17	ns
$t_{FIFOWCLKS}$	Write Data Setup before Write Clock Time	—	1.00	—	1.67	ns

Timing v.1.0

## sysHSI Block Timing

Figure 20 provides a graphical representation of the SERDES receiver input requirements. It provides guidance on a number of input parameters, including signal amplitude and rise time limits, noise and jitter limits, and P and N input skew tolerance.

**Figure 20. Receive Data Eye Diagram Template (Differential)**



$JT_{TH}$  : Optimum Threshold Crossing Jitter

The data pattern eye opening at the receive end of a link is considered the ultimate measure of received signal quality. Almost all detrimental characteristics of a transmit signal and the interconnection link design result in eye closure. This combined with the eye-opening limitations of the line receiver can provide a good indication of a link's ability to transfer error-free data.

Signal jitter is of special interest to system designers. It is often the primary limiting characteristic of long digital links and of systems with high noise level environments. An interesting characteristic of the clock and data recovery (CDR) portion of the ispGDX2 SERDES receiver is its ability to filter incoming signal jitter that is below the clock recovery PLL bandwidth. For signals with high levels of low frequency jitter, the receiver can detect incoming data error free, with eye openings significantly less than that shown in Figure 20.

## sysHSI Block AC Specifications

### Operating Frequency Ranges

Symbol	Description	Mode	Test Condition	Min	Max	Unit
$f_{CLK}$	REFCLK, SS_CLKIN, SS_CLKOUT	All		40	250	MHz
$f_{SIN}$	Serial Input	SS: no CAL	with $eo_{SIN}$	400	750	Mbps
		SS: CAL	with $eo_{SIN}$	400	800	Mbps
		10B12B	with $eo_{SIN}$	400	850 <sup>1</sup>	Mbps
		8B10B	with $eo_{SIN}$	400	850 <sup>1</sup>	Mbps
$f_{SOUT}$	Serial Out	LVDS	$C_L=5\text{ pF}$ , $R_L=100\text{ Ohm}$	400	850	Mbps

1.  $f_{SIN}$  (8B/10B and 10B/12B) 850Mbps limit applicable only to 3.5ns part. Limit is 800 Mbps for 5ns and 7ns parts.

**LOCKIN Time**

Symbol	Description	Mode	Condition	Min	Max	Unit
$t_{\text{SCLOCK}}$	CSPLL Lock Time	All	After Input is Stabilized		25	$\mu\text{S}$
$t_{\text{CDRLOCK}}$	CDRPLL Lock-in Time	SS	With SS mode Sync Pattern		1024	$t_{\text{RCP}}^1$
		10B12B	With 10B12B Sync Pattern		1024	$t_{\text{RCP}}$
		8B10B	With 8B10B Idle Pattern		480	$t_{\text{RCP}}$
$t_{\text{SYNC}}$	SyncPat Length	SS		1200		$t_{\text{RCP}}$
$t_{\text{CAL}}$	CAL Duration	SS		1100		$t_{\text{RCP}}$
$t_{\text{SUSYNC}}$	SyncPat Set-up Time to CAL	SS		50		$t_{\text{RCP}}$
$t_{\text{HDSYNC}}$	SyncPat Hold Time from CAL	SS		50		$t_{\text{RCP}}$

1. REFCLK clock period.

**REFCLK and SS\_CLKIN Timing**

Symbol	Description	Mode	Condition	Min	Max	Unit
$f_{\text{DREFCLK}}$	Frequency Deviation Between TX REFCLK and CDRX REFCLK on one link.	8B10B, 10B12B		-100	100	ppm
$t_{\text{JPPREFCLK}}$	REFCLK, SS_CLKIN Peak-to-Peak Period Jitter	All	40-250 (MHz)	-0.005	0.005	UIPP
$t_{\text{PWREFCLK}}$	REFCLK, SS_CLKIN Pulse Width, (80% to 80% or 20 % to 20%).	All		1		ns
$t_{\text{RFREFCLK}}$	REFCLK, SS_CLKIN Rise/Fall Time. (20% to 80% or 80% to 20%)	All			2	ns

**Serializer Timing<sup>2</sup>**

Symbol	Description	Mode	Condition	Min	Max	Unit
$t_{\text{JPPSOUT}}$	SOUT Peak-to-Peak Output Data Jitter	All			0.25	UIPP
$t_{\text{JPP8B10B}}$	SOUT Peak-to-Peak Random Jitter	8B10B	900 Mbps w/K28.7-		130	ps
	SOUT Peak-to-Peak Deterministic Jitter	8B10B	900 Mbps w/K28.5+		110	ps
$t_{\text{RFSOUT}}$	SOUT Output Data Rise/Fall Time (20%, 80%)	LVDS			700	ps
		BLVDS			900	ps
$t_{\text{COSOUT}}$	REFCLK to SOUT Delay	SS/8B10B		$2Bt^1 + 2$	$2Bt^1 + 10$	ns
		10B12B		$1Bt^1 + 2$	$1Bt^1 + 10$	ns
$t_{\text{SKTX}}$	Skew of SOUT with Respect to SS_CLKOUT	SS			250	ps
$t_{\text{CKOSOUT}}$	SS_CLKOUT to bit0 of SOUT	SS		$2Bt^1 - t_{\text{SKTX}}$	$2Bt^1 + t_{\text{SKTX}}$	ns
$t_{\text{HSITXDDATAS}}$	TXD Data Setup Time	All	Note 3	1.5		ns
$t_{\text{HSITXDDATAH}}$	TXD Data Hold Time	All	Note 3		1.0	ns

1. Bt: Bit Time Period. High Speed Serial Bit Time.

2. The SIN and SOUT jitter specifications listed above are under the condition that the clock tree that drives the REFCLK to sysHSI Block is in sysCLOCK PLL BYPASS mode.

3. Internal timing for reference only.

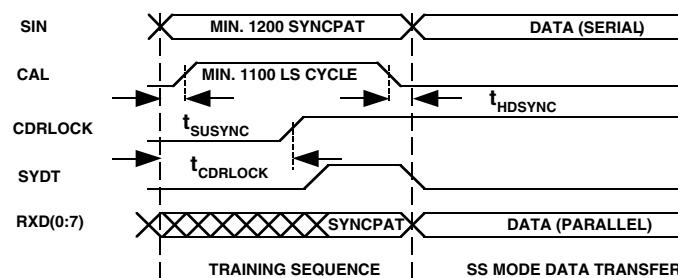
## Deserializer Timing

Symbol	Description	Mode	Conditions	Min	Max	Units
$f_{DSIN}$	SIN Frequency Deviation from REFCLK	8B10B/ 10B12B		-100	+100	ppm
$eo_{SIN}$	SIN Eye Opening Tolerance	All CDR		0.4		UIPP
		SS (Note 1)		0.65		UIPP
ber	Bit Error Rate	All			$10^{-12}$	Bits
$t_{SKRX}$	Skew Margin Between SIN and SS_CLKIN	SS	Note 1		0.125	UIPP
$t_{CKISIN}$	SS_CLKIN to bit0 of SIN	SS	Note 1	$2Bt - t_{SKRX}$	$2Bt + t_{SKRX}$	ns
$t_{HSIOUTVALIDPRE}$	RXD, LOSS, CDRLOCK, SYDT Valid Time Before RECCLK Falling Edge	All	Note 3	$t_{RCP}/2 - 0.7$		ns
$t_{HSIOUTVALIDPOST}$	RXD, LOSS, CDRLOCK, SYDT Valid Time After RECCLK Falling Edge	All	Note 3	$t_{RCP}/2 - 0.7$		ns
$t_{DSIN}$	Bit 0 of SIN Delay to RXD Valid at RECCLK Falling edge	All CDR		$1.5 t_{RCP} + 4.5Bt + 2$	$1.5 t_{RCP} + 4.5Bt + 10$	ns
		SS	Note 1	$1.5 t_{RCP} + 1.5Bt + 3$	$1.5 t_{RCP} + 1.5Bt + 15$	ns

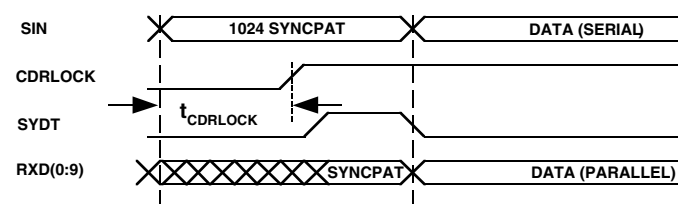
1. SS Normal Receive Mode (no de-skew option).
2. ispGDX2 only. RX\_SS mode only. This limit is increased if EO is increased.
3. Internal timing for reference only.

## Lock-in Timing

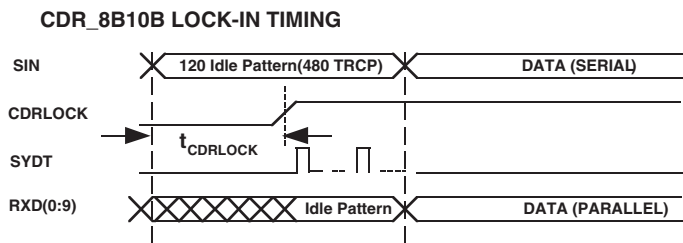
## CDRX\_SS LOCK-IN (DE-SKEW) TIMING



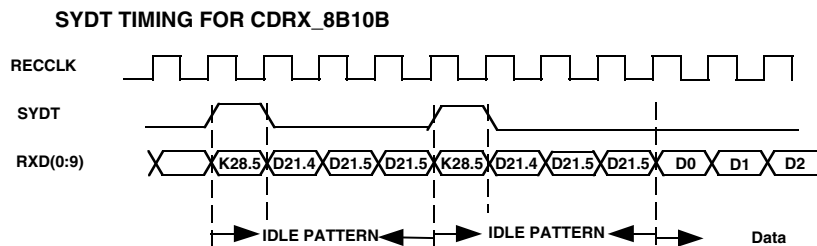
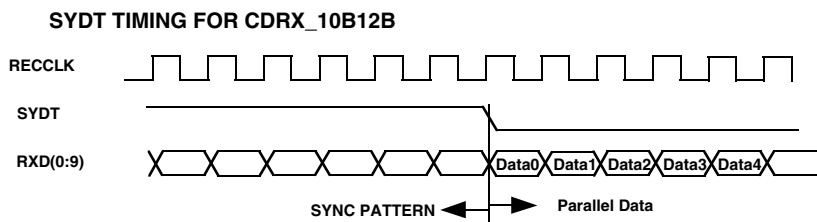
## CDR\_10B12B LOCK-IN TIMING



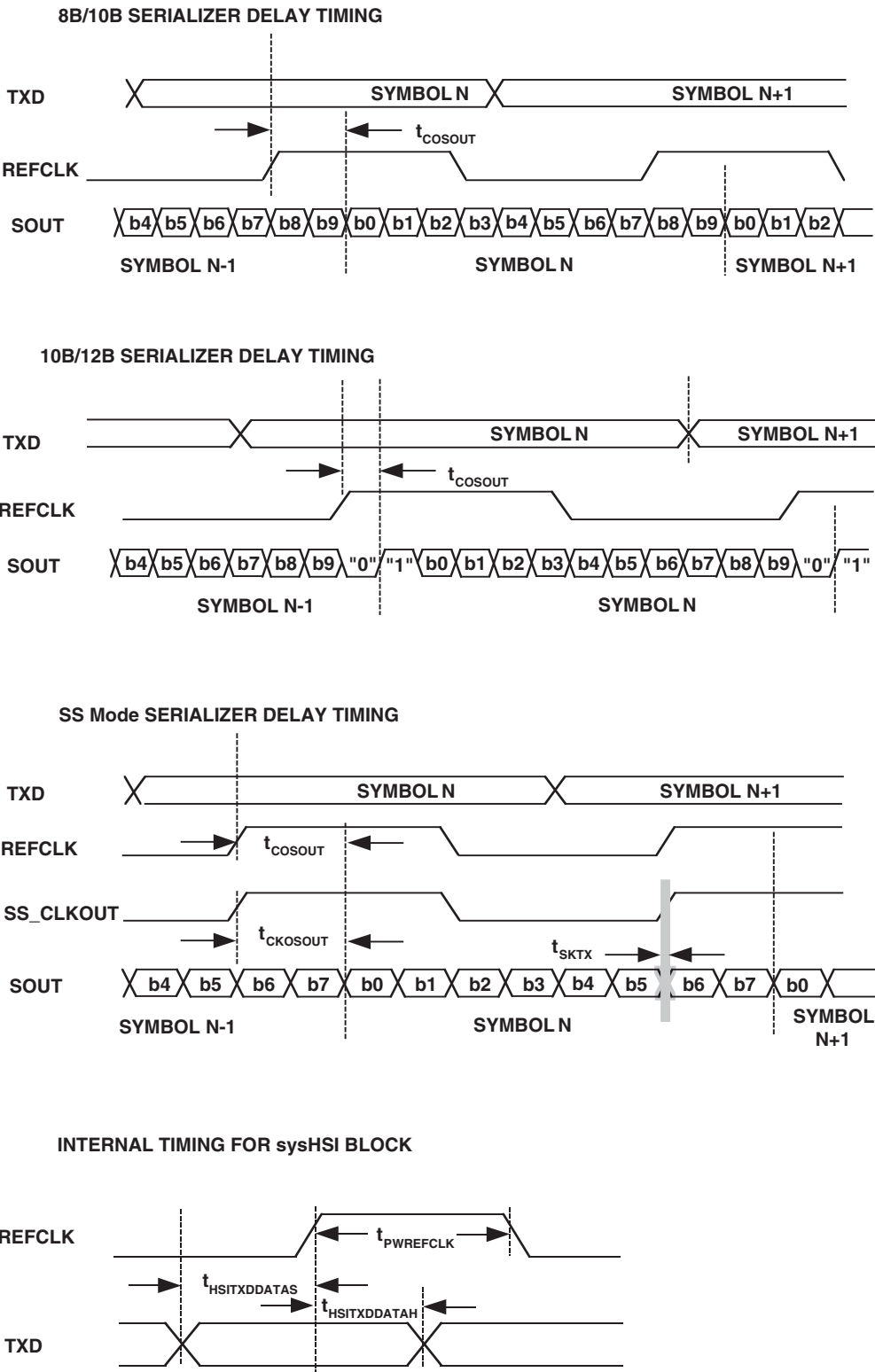
Lock-in Timing (Continued)



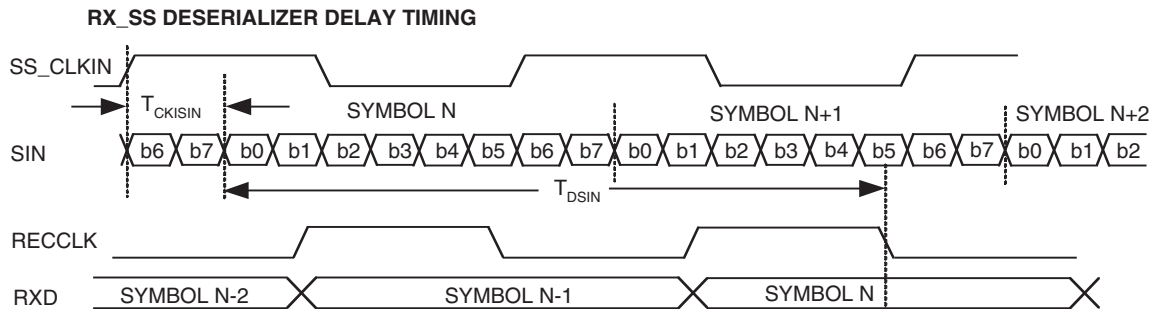
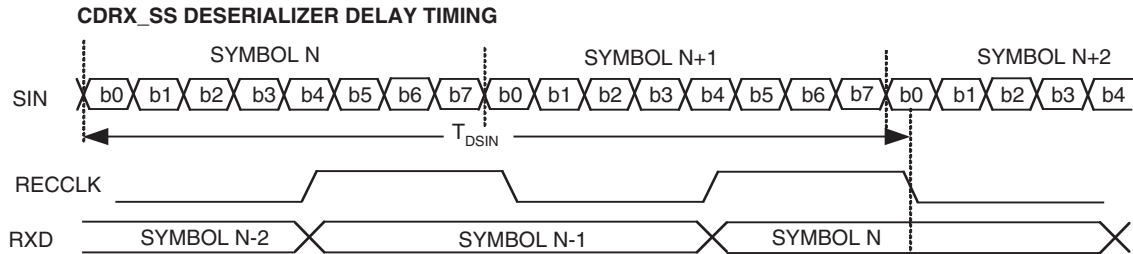
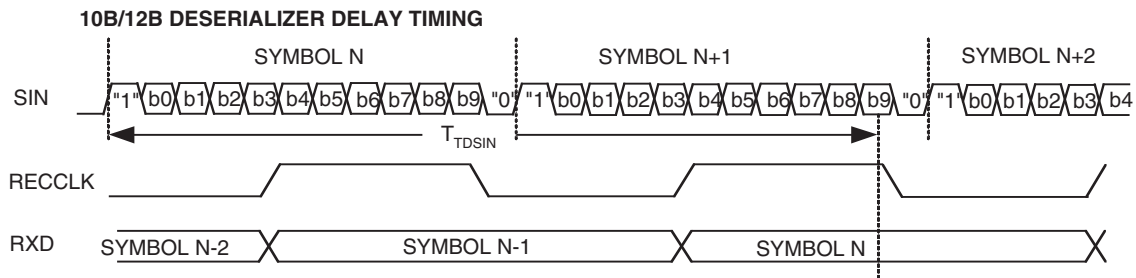
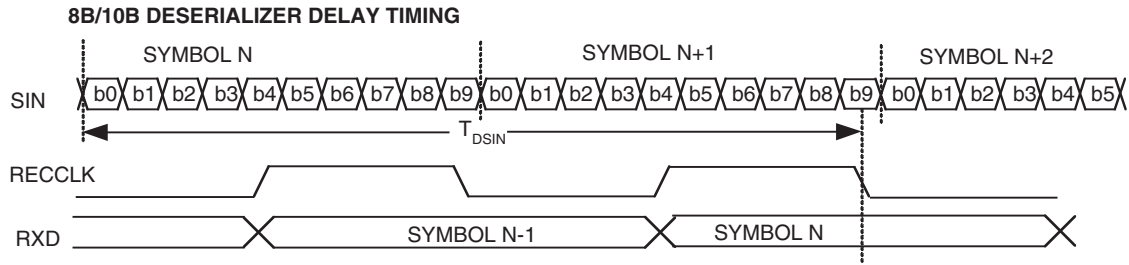
SYDT Timing



Serializer Timing



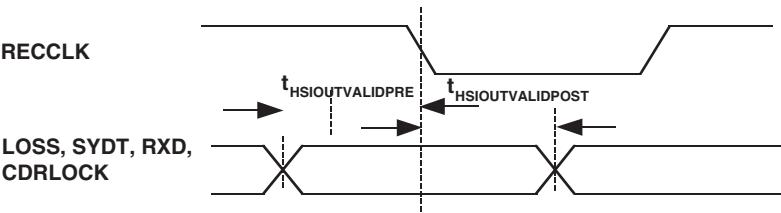
## Deserializer Timing





Deserializer Timing (Continued)

INTERNAL TIMING FOR sysHSI BLOCK



**sysCLOCK PLL Timing****Over Recommended Operating Conditions**

Symbol	Parameter	Conditions	Min	Max	Units
$t_{PWH}$	Input clock, high time	80% to 80%	0.5	—	ns
$t_{PWL}$	Input clock, low time	20 % to 20%	0.5	—	ns
$t_R, t_F$	Input Clock, rise and fall time	20% to 80%	—	3.0	ns
$t_{INSTB}$	Input clock stability, cycle to cycle (peak)		—	+/- 300	ps
$f_{MDIVIN}$	M Divider input, frequency range		10	320	MHz
$f_{MDIVOUT}$	M Divider output, frequency range		10	320	MHz
$f_{NDIVIN}$	N Divider input, frequency range		10	320	MHz
$f_{NDIVOUT}$	N Divider output, frequency range		10	320	MHz
$f_{VDIVIN}$	V Divider input, frequency range		100	400	MHz
$f_{VDIVOUT}$	V Divider output, frequency range		10	320	MHz
$t_{OUTDUTY}$	Output clock, duty cycle		40	60	%
$t_{JIT(CC)}$	Output clock, cycle to cycle jitter (peak)	Clean reference: 10 MHz $\leq f_{MDIVOUT} < 20$ MHz or 100 MHz $\leq f_{VDIVIN} < 160$ MHz	—	+/- 250	ps
		Clean reference: 20 MHz $\leq f_{MDIVOUT} \leq 320$ MHz and 160 MHz $\leq f_{VDIVIN} \leq 400$ MHz	—	+/- 100	ps
$T_{JIT(PERIOD)}^2$	Output clock, period jitter (peak)	Clean reference: 10 MHz $\leq f_{MDIVOUT} < 20$ MHz or 100 MHz $\leq f_{VDIVIN} < 160$ MHz	—	+/- 300	ps
		Clean reference: 20 MHz $\leq f_{MDIVOUT} \leq 320$ MHz and 160 MHz $\leq f_{VDIVIN} \leq 400$ MHz	—	+/- 150	ps
$t_{CLK\_OUT\_DLY}$	Input clock to CLK_OUT delay	Internal feedback	—	3.4	ns
$t_{PHASE}$	Input clock to external feedback delta	External feedback	—	500	ps
$t_{LOCK}$	Time to acquire phase lock after input stable		—	25	us
$t_{PLL\_DELAY}$	Delay increment (Lead/Lag)		+/- 120	+/- 550	ps
$t_{RANGE}$	Total output delay range (lead/lag)		+/- 0.84	+/- 3.85	ns
$t_{PLL\_RSTW}$	Minimum reset pulse width		—	1.8	ns

1. This condition assures that the output phase jitter will remain within specification

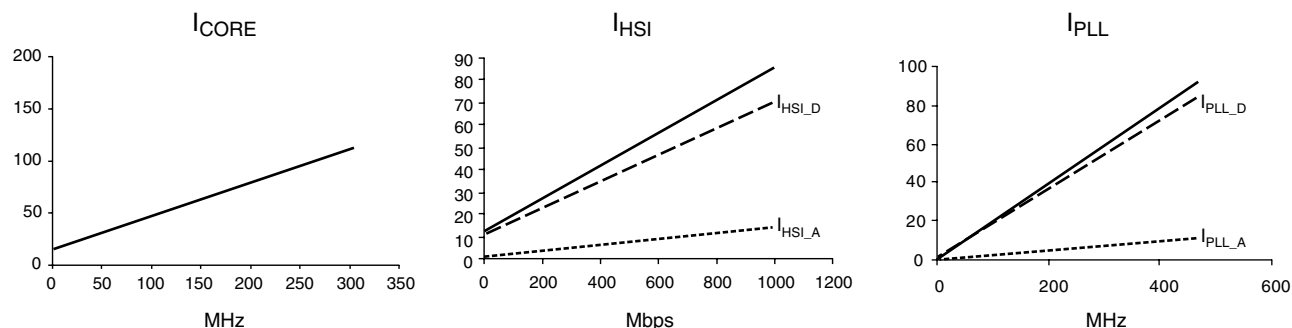
2. Accumulated jitter measured over 10,000 waveform samples

## Boundary Scan Timing Specifications

Over Recommended Operating Conditions

Parameter	Description	Min	Max	Units
$t_{BTCP}$	TCK [BSCAN] clock pulse width	40	—	ns
$t_{BTCPH}$	TCK [BSCAN] clock pulse width high	20	—	ns
$t_{BTCPL}$	TCK [BSCAN] clock pulse width low	20	—	ns
$t_{BTS}$	TCK [BSCAN] setup time	8	—	ns
$t_{BTH}$	TCK [BSCAN] hold time	10	—	ns
$t_{BTRF}$	TCK [BSCAN] rise/fall time	50	—	mV/ns
$t_{BTCO}$	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
$t_{BTCOEN}$	TAP controller falling edge of clock to valid enable	—	10	ns
$t_{BTCRS}$	BSCAN test capture register setup time	8	—	ns
$t_{BTCRH}$	BSCAN test capture register hold time	10	—	ns
$t_{BUTCO}$	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

## Power Consumption



### Power Estimation Coefficients – Core and PLL

Device	V <sub>CC</sub>	I <sub>DC</sub> (mA)	K <sub>REF</sub>	K <sub>IN</sub>	K <sub>CORE</sub>	K <sub>PLLD</sub>	K <sub>PLLA</sub>
ispGDX2-256	3.3	10.0	2.054	0.0139	0.292	0.157	0.024
	2.5	10.0	2.054	0.0139	0.292	0.157	0.024
	1.8	4.0	1.334	0.0213	0.239	0.179	0.024

$I_{DC}$ : Blank chip background current  
 $K_{REF}$ : Reference voltage circuit current per bank  
 $K_{IN}$ : I/O current per input per MHz  
 $K_{CORE}$ : Core current per MHz with GRP fanout of 1  
 $K_{PLLD}$ : PLL logic current per MHz per PLL  
 $K_{PLLA}$ : PLL analog portion current per MHz per PLL

### Power Estimation Coefficients – sysHSI

Device	V <sub>CC</sub>	K <sub>RXD</sub>	K <sub>RXSTBY</sub>	K <sub>RXA</sub>	K <sub>TXD</sub>	K <sub>TXSTBY</sub>	K <sub>TXA</sub>
ispGDX2-256	3.3	0.027	1.3	0.0023	0.011	2.4	0.0018
	2.5	0.027	1.3	0.0023	0.011	2.4	0.0018
	1.8	0.019	3.7	0.0040	0.011	1.2	0.0023

$K_{RXD}$ : Receiver Logic current per Mbps  
 $K_{RXSTBY}$ : Receiver Logic standby current  
 $K_{RXA}$ : Receiver Analog portion current per Mbps  
 $K_{TXD}$ : Transmitter Logic current per Mbps  
 $K_{TXSTBY}$ : Transmitter Logic standby current  
 $K_{TXA}$ : Transmitter Analog portion current per Mbps

## Power Consumption (Continued)

Power consumption in the ispGDX2 family is the sum of three components:

$$I_{CC-TOTAL} = I_{CORE} + I_{PLL} + I_{HSI} \text{ (} I_{CC-TOTAL} \text{ combines current supplied via } V_{CC} \text{ pins and } V_{CCP} \text{ pins)}$$

$$\begin{aligned} I_{CORE} &= I_{DC} + I_{REF} + I_{IN} \\ &= \text{Blank chip background current} \\ &\quad + K_{REF} * \text{Number of Banks with } V_{REF} \text{ active} \\ &\quad + (K_{IN} * \text{Number of inputs} + K_{CORE}) * \text{Average Input Switching Frequency (MHz)} \\ I_{PLL} &= I_{PLL\_D} + I_{PLL\_A} \\ &= [K_{PLLD} * F_{VCO} * \text{Number of PLLs used}] + [K_{PLLA} * F_{VCO} * \text{Number of PLLs used}] \\ &= [(K_{PLLD} + K_{PLLA}) * F_{VCO}] * \text{Number of PLLs used} \\ I_{HSI} &= I_{RX} + I_{TX} \\ &= [(K_{RXD} + K_{RXA}) * F_{RX} + I_{RXSTBY}] * \text{Number of Receiver Channels} \\ &\quad + [(K_{TXD} + K_{TXA}) * F_{TX} + I_{TXSTBY}] * \text{Number of Transmitter Channels} \end{aligned}$$

Where:

$F_{VCO}$ : sysClock PLL VCO Frequency in MHz  
 $F_{RX}$ : sysHSI Receiver Serial Data Rate  
 $F_{TX}$ : sysHSI Transmitter Serial Data Rate

$I_{HSI}$  can also be determined by calculating  $I_{HSI\_D}$ , the current supplied by the  $V_{CC}$  pin, and  $I_{HSI\_A}$ , the current supplied by the  $V_{CCP0}$  and  $V_{CCP1}$ .

$$\begin{aligned} I_{HSI} &= I_{HSI\_D} + I_{HSI\_A} \\ &= [(K_{RXD} * F_{RX} + I_{RXSTBY}) * \text{Number of Receiver Channels} \\ &\quad + (K_{TXD} * F_{TX} + I_{TXSTBY}) * \text{Number of Transmitter Channels}] \\ &\quad + [(K_{RXA} * F_{RX}) * \text{Number of Receiver Channels} \\ &\quad + [(K_{TXA} * F_{TX}) * \text{Number of Transmitter Channels}] \end{aligned}$$

The  $I_{CCP}$  is supplied through  $V_{CCP0}$  and  $V_{CCP1}$  pins for PLL and sysHSI analog portion. The equation for  $I_{CCP}$  can be derived from the equations below.

$$\begin{aligned} I_{CCP} &= I_{PLL\_A} + I_{HSI\_A} \\ &= [(K_{PLLA} * F_{VCO}) * \text{Number of PLLs used}] \\ &\quad + [(K_{RXA} * F_{RX}) * \text{Number of Receiver Channels} \\ &\quad + (K_{TXA} * F_{TX}) * \text{Number of Transmitter Channels}] \end{aligned}$$

Where:

$I_{PLL\_A}$ : PLL Analog Portion Current  
 $I_{HSI\_A}$ : HSI Analog Portion Current

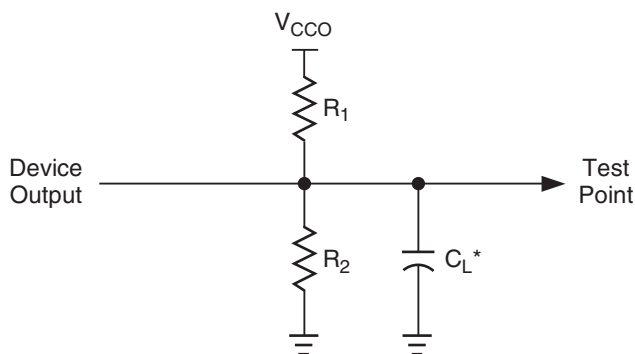
Note: For further information about the use of these coefficients, refer to Technical Note TN1034, *Power Estimation in the ispGDX2 Family*.

$I_{CC-TOTAL}$  estimates are based on typical conditions. These values are for estimates only. Since the value of  $I_{CC-TOTAL}$  is sensitive to operating conditions and the program in the device, the actual current should be verified.

## Switching Test Conditions

Figure 21 shows the output test load used for AC testing. Specific values for resistance, capacitance, voltage and other test conditions are shown in Table 7.

**Figure 21. Output Test Load, LVTTTL and LVCMOS Standards (1.8V)**



\* $C_L$  includes Test Fixture and Probe Capacitance.

**Table 7. Test Fixture Required Components**

Test Condition	$R_1$	$R_2$	$C_L$	Timing Ref.	$V_{CCO}$
Default LVCMOS 1.8 I/O (L -> H, H -> L)	106	106	35pF	$V_{CCO}/2$	1.8V
LVCMOS I/O (L -> H, H -> L)	—	—	35pF	LVC MOS3.3 = 1.5V	LVC MOS3.3 = 3.0V
				LVC MOS2.5 = $V_{CCO}/2$	LVC MOS2.5 = 2.3V
				LVC MOS1.8 = $V_{CCO}/2$	LVC MOS1.8 = 1.65V
Default LVCMOS 1.8 I/O (Z -> H)	—	106	35pF	$V_{CCO}/2$	1.65V
Default LVCMOS 1.8 I/O (Z -> L)	106	—	35pF	$V_{CCO}/2$	1.65V
Default LVCMOS 1.8 I/O (H -> Z)	—	106	5pF	$V_{OH} - 0.15$	1.65V
Default LVCMOS 1.8 I/O (L -> Z)	106	—	5pF	$V_{OL} + 0.15$	1.65V

Note: Output test conditions for all other interfaces are determined by the respective standards.

## Signal Descriptions<sup>1</sup>

Signal Names	Description
<b>General Purpose</b>	
BKx_IOy	Input/Output – General purpose I/O number y in I/O Bank X.
GCLK/CE0, GCLK/CE1, GCLK/CE2, GCLK/CE3	Input – Global clock/clock enable inputs.
SEL0, SEL1, SEL2 <sup>2</sup> , SEL3 <sup>2</sup>	Input – Global MUX select inputs.
GOE0, GOE1, GOE2 <sup>2</sup> , GOE3 <sup>2</sup>	Input – Global output enable inputs.
RESETb	Input – Global RESET signal (active low).
NC	No connect.
GND	GND – Ground.
V <sub>CC</sub>	VCC – The power supply pins for core logic.
V <sub>CCJ</sub>	VCC – The power supply for the JTAG logic.
V <sub>CCOx</sub>	VCC – The power supply pins for I/O Bank X.
V <sub>REFx</sub>	Input – Defines the reference voltage for I/O Bank X.
<b>Testing and Programming</b>	
TMS	Input – Test Mode Select input, used to control the 1149.1 state machine.
TCK	Input – Test Clock Input pin, used to clock the 1149.1 state machine.
TDI	Input – Test Data In pin, used to load data into device using 1149.1 state machine.
TDO	Output – Test Data Out pin used to shift data out of device using 1149.1.
TOE	Input – Test Output Enable pin. TOE tristates all I/O pins when driven low.
<b>PLL Functions</b>	
PLL_FBKz	Input – Optional feedback input allows external feedback for PLL z.
PLL_RSTz	Input – Optional input resets the M divider in PLL z.
CLK_OUTz	Output – Optional clock output from PLL z (clock signal occupies the input path of this I/O pad).
PLL_LOCKz	Output – Optional lock output from PLL z (lock signal occupies the input path of this I/O pad).
GND <sub>P0</sub> , GND <sub>P1</sub>	GND – Ground for PLLs.
V <sub>CCP0</sub> , V <sub>CCP1</sub>	VCC – The power supply pins for PLLs.
<b>FIFO Functions</b>	
FIFOy_DINw	Input – DATA IN Bit w of FIFO y.
FIFOy_DOUTw	Internal Signal – DATA OUT Bit w of FIFO y
FIFOy_FIFORSTb	Input – Reset input for FIFO y (active low).
FIFOy_FULL	Output – FULL flag for FIFO y.
FIFOy_EMPTY	Output – EMPTY flag for FIFO y.
FIFOy_STRDb	Output – Start read (STRDb) flag for FIFO y.
<b>SERDES Functions</b>	
HSImA_SINP, HSImB_SINP	Input – Positive sense serial input for sysHSI BLOCK m channel A, B.
HSImA_SINN, HSImB_SINN	Input – Negative (minus) sense serial input for sysHSI BLOCK m channel A, B.
HSImA_SOUTP, HSImB_SOUTP	Output – Positive sense serial output for sysHSI BLOCK m channel A, B.
HSImA_SOUTN, HSImB_SOUTN	Output – Negative (minus) sense serial output for sysHSI BLOCK m channel A, B.
HSImA_LOSS, HSImB_LOSS	Output – Loss of signal flag for sysHSI BLOCK m channel A, B.
HSImA_SYDT, HSImB_SYDT	Output – Symbol alignment detect for sysHSI BLOCK m channel A, B.
HSImA_RECCLK, HSImB_RECCLK	Internal Signal – Recovered clock for sysHSI BLOCK m channel A, B.
HSImA_CDRLOCK, HSImB_CDRLOCK	Internal Signal – CDR lock output for sysHSI BLOCK m channel A, B.

## Signal Descriptions<sup>1</sup> (Continued)

Signal Names	Description
HSImA_CDRRSTb, HSImB_CDRRSTb	Input – Resets the CDR circuit of sysHSI BLOCK m channel A, B.
HSImA_EXLOSS, HSImB_EXLOSS	Input – Forces LOS signal for sysHSI BLOCK m channel A, B.
HSIm_CSLOCK	Output – LOCK output of the PLL associated with channel m.
HSImA_TXDw, HSImB_TXDw	Internal Signal – Parallel data in bit w for sysHSI BLOCK m channel A, B.
HSImA_RXDw, HSImB_RXDw	Internal Signal – Parallel data out bit w for sysHSI BLOCK m channel A, B.
<b>Source Synchronous Functions</b>	
SS_SCLKIN0P, SS_SCLKIN1P	Input – Positive sense clock input for Source Synchronous group A, B.
SS_SCLKIN0N, SS_SCLKIN1N	Input – Negative (minus) sense clock input for Source Synchronous group A, B.
SS_CLKOUT0N, SS_CLKOUT1P	Output – Positive sense clock output for Source Synchronous group A, B.
SS_CLKOUT0N, SS_CLKOUT1N	Output – Negative (minus) sense clock output for Source Synchronous group A, B.
CAL	Input – Initiates source synchronous calibration sequence.

1. m, w, x, y and z are variables.

2. Not on ispGDX2-64

## ispGDX2-256 Power Supply and NC Connections<sup>1</sup>

Signals	ispGDX2-256 (484-Ball fpBGA)
V <sub>CC</sub>	AA3, AA20, B3, B20, C2, C11, C12, C21, H9, H10, H11, H12, H13, H14, J8, J15, K8, K15, L8, L15, L20, M3, M8, M15, M20, N8, N15, P8, P15, R9, R10, R11, R12, R13, R14, Y2, Y11, Y12, Y21
V <sub>CCO0</sub>	AA14, AB20, Y17
V <sub>CCO1</sub>	P21, U20, Y22
V <sub>CCO2</sub>	C22, E20, J21
V <sub>CCO3</sub>	A20, B14, C17
V <sub>CCO4</sub>	A3, B9, C6
V <sub>CCO5</sub>	C1, F3, J2
V <sub>CCO6</sub>	P2, U3, Y1
V <sub>CCO7</sub>	AA9, AB3, Y6
V <sub>CCP0</sub>	K1
V <sub>CCP1</sub>	N22
V <sub>CCJ</sub>	L3
GND <sub>P0</sub>	J1
GND <sub>P1</sub>	K22
GND	A2, A11, A12, A21, A1, A22, AA1, AA2, AA11, AA12, AA21, AA22, AB1, AB2, AB11, AB12, AB21, AB22, B1, B2, B11, B12, B21, B22, C3, C20, D4, D19, E5, E18, F6, F17, G7, G16, H8, H15, J9, J10, J11, J12, J13, J14, K9, K10, K11, K12, K13, K14, L1, L2, L7, L9, L10, L11, L12, L13, L14, L16, L21, L22, M1, M2, M7, M9, M10, M11, M12, M13, M14, M16, M21, M22, N9, N10, N11, N12, N13, N14, P9, P10, P11, P12, P13, P14, R8, R15, T7, T16, U6, U17, V5, V18, W4, W19, Y3, Y20
NC <sup>2</sup>	D8, D11, E6, E7, E8, E9, E12, E13, E14, E15, E16, F7, F16, G5, G6, G18, G19, H19, K4, K19, L19, M4, M19, N4, P4, P19, R4, R18, T4, T5, T17, T18, U5, U7, U16, V7, V8, V9, V10, V11, V12, V15, V16, V17, W14, Y18

1. All grounds must be electrically connected at the board level.

2. NC pins should not be connected to any active signals, V<sub>CC</sub> or GND.



ispGDX2-256 Logic Signal Connections<sup>1,2</sup>

Signal Name	sysIO Bank	LVDS Buffer		GDX Block	MRB	SERDES Mode I/O Functions	SERDES Mode SERDES to FIFO Core	FIFO Mode I/O Function	484 fpBGA
		Polarity	Pair						
BK0_IO0	0	N	0	0A	0	-	-	FIFO0A_FULL	AB13
BK0_IO1	0	P	0	0A	1	-	-	-	AA13
BK0_IO2/ PLL_LOCK2	0	N	1	0A	2	-	-	-	V13
BK0_IO3	0	P	1	0A	3	-	-	FIFO0A_EMPTY	V14
GND	0	-	-	-	-	-	-	-	GND
BK0_IO4	0	N	2	0A	4	HSI0A_SINN	HSI0A_RXD0	FIFO0A_DIN0	U12
BK0_IO5	0	P	2	0A	5	HSI0A_SINP	HSI0A_RXD1	FIFO0A_DIN1	U13
BK0_IO6	0	N	3		6	-	HSI0A_RXD2	FIFO0A_DIN2	W12
BK0_IO7	0	P	3	0A	7	HSI0A_EXLOSS	HSI0A_RXD3	FIFO0A_DIN3	Y13
BK0_IO8	0	N	4	0A	8		HSI0A_RXD4	FIFO0A_DIN4	W13
BK0_IO9/ PLL_FB2	0	P	4	0A	9	-	HSI0A_RXD5	FIFO0A_DIN5	Y14
BK0_IO10	0	N	5	0A	10	HSI0A_SOUTN	HSI0A_RXD6	FIFO0A_DIN6	T12
BK0_IO11	0	P	5	0A	11	HSI0A_SOUTP	HSI0A_RXD7	FIFO0A_DIN7	T13
GND	0	-	-	-	-	-	-	-	GND
BK0_IO12	0	N	6	0A	12	HSI0A_LOSS_0A	HSI0A_RXD8	FIFO0A_DIN8	AB14
BK0_IO13	0	P	6	0A	13	HSI0A_SYDT	HSI0A_RXD9	FIFO0A_DIN9	AB15
BK0_IO14	0	N	7	0A	14	HSI0A_CDRRSTb	HSI0A_RECCLK	FIFO0A_FIFORSTb	Y15
BK0_IO15	0	P	7	0A	15	-	HSI0A_CDRLOCK	FIFO0A_STRDb	W15
BK0_IO16	0	N	8	1A	0	-	-	FIFO1A_FULL	AA15
BK0_IO17/ PLL_RST2	0	P	8	1A	1	-	-	-	AA16
BK0_IO18	0	N	9	1A	2	-	-	-	Y16
BK0_IO19	0	P	9	1A	3	HSI1A_EXLOSS	HSI1A_RXD0	FIFO1A_DIN0	W16
GND	0	-	-	-	-	-	-	-	GND
BK0_IO20	0	N	10	1A	4	HSI1A_SOUTN	HSI1A_RXD1	FIFO1A_DIN1	U14
BK0_IO21/ VREF0	0	P	10	1A	5	HSI1A_SOUTP	HSI1A_RXD2	FIFO1A_DIN2	U15
BK0_IO22	0	N	11	1A	6	-	HSI1A_RXD3	FIFO1A_DIN3	AB16
BK0_IO23	0	P	11	1A	7		HSI1A_RXD4	FIFO1A_DIN4	AB17
BK0_IO24	0	N	12	1A	8	-	HSI1A_RXD5	FIFO1A_DIN5	AA17
BK0_IO25	0	P	12	1A	9	HSI1A_LOSS	HSI1A_RXD6	FIFO1A_DIN6	W17
BK0_IO26	0	N	13	1A	10	HSI1A_SINN	HSI1A_RXD7	FIFO1A_DIN7	T14
BK0_IO27	0	P	13	1A	11	HSI1A_SINP	HSI1A_RXD8	FIFO1A_DIN8	T15
BK0_IO28	0	N	14	1A	12	HSI1A_SYDT	HSI1A_RXD9	FIFO1A_DIN9	AA18
BK0_IO29	0	P	14	1A	13	HSI1A_CDRRSTb	HSI1A_RECCLK	FIFO1A_FIFORSTb	AB18
BK0_IO30	0	N	15	1A	14	-	HSI1A_CDRLOCK	FIFO1A_STRDb	W18
BK0_IO31	0	P	15	1A	15	-	-	FIFO1A_EMPTY	Y19
GND	0	-	-	-	-	-	-	-	GND
GOE3	-	-	-	-	-	-	-	-	AA19
TDO	-	-	-	-	-	-	-	-	AB19
GND	1	-	-	-	-	-	-	-	GND
BK1_IO0	1	P	16	0B	0	-	-	FIFO0B_FULL	W21
BK1_IO1	1	N	16	0B	1	-	-	-	W20
BK1_IO2	1	P	17	0B	2	HSI0B_EXLOSS	HSI0B_RXD0	FIFO0B_DIN0	V22
BK1_IO3	1	N	17	0B	3		HSI0B_RXD1	FIFO0B_DIN1	W22

ispGDX2-256 Logic Signal Connections<sup>1, 2</sup> (Continued)

Signal Name	sysIO Bank	LVDS Buffer		GDX Block	MRB	SERDES Mode I/O Functions	SERDES Mode SERDES to FIFO Core	FIFO Mode I/O Function	484 fpBGA
		Polarity	Pair						
BK1_IO4	1	P	18	0B	4	HSI0B_SINP	HSI0B_RXD2	FIFO0B_DIN2	P16
BK1_IO5	1	N	18	0B	5	HSI0B_SINN	HSI0B_RXD3	FIFO0B_DIN3	P17
BK1_IO6	1	P	19	0B	6	HSI0_CSLOCK	HSI0B_RXD4	FIFO0B_DIN4	U18
BK1_IO7	1	N	19	0B	7	-	HSI0B_RXD5	FIFO0B_DIN5	V19
BK1_IO8	1	P	20	0B	8	HSI0B_LOSS	HSI0B_RXD6	FIFO0B_DIN6	V20
BK1_IO9	1	N	20	0B	9	HSI0B_SYDT	HSI0B_RXD7	FIFO0B_DIN7	V21
BK1_IO10/ VREF1	1	P	21	0B	10	HSI0B_SOUTP	HSI0B_RXD8	FIFO0B_DIN8	R16
BK1_IO11	1	N	21	0B	11	HSI0B_SOUTN	HSI0B_RXD9	FIFO0B_DIN9	R17
GND	1	-	-	-	-	-	-	-	GND
BK1_IO12	1	P	22	0B	12	HSI0B_CDRRSTb	HSI0B_RECCLK	FIFO0B_FIFORSTb	U19
BK1_IO13	1	N	22	0B	13	-	HSI0B_CDRLOCK	FIFO0B_STRDb	T19
BK1_IO14	1	P	23	0B	14	-	-	-	U21
BK1_IO15	1	N	23	0B	15	-	-	FIFO0B_EMPTY	U22
BK1_IO16	1	P	24	1B	0	-	-	FIFO1B_FULL	R19
BK1_IO17	1	N	24	1B	1	HSI1B_EXLOSS	HSI1B_RXD0	FIFO1B_DIN0	T20
BK1_IO18	1	P	25	1B	2	-	HSI1B_RXD1	FIFO1B_DIN1	T21
BK1_IO19	1	N	25	1B	3	-	HSI1B_RXD2	FIFO1B_DIN2	T22
GND	1	-	-	-	-	-	-	-	GND
BK1_IO20	1	P	26	1B	4	HSI1B_SOUTP	HSI1B_RXD3	FIFO1B_DIN3	N16
BK1_IO21	1	N	26	1B	5	HSI1B_SOUTN	HSI1B_RXD4	FIFO1B_DIN4	N17
BK1_IO22	1	P	27	1B	6	HSI1_CSLOCK	HSI1B_RXD5	FIFO1B_DIN5	R20
BK1_IO23	1	N	27	1B	7	HSI1B_SYDT	HSI1B_RXD6	FIFO1B_DIN6	R21
BK1_IO24	1	P	28	1B	8	-	HSI1B_RXD7	FIFO1B_DIN7	N19
BK1_IO25	1	N	28	1B	9	HSI1B_LOSS	HSI1B_RXD8	FIFO1B_DIN8	P20
BK1_IO26	1	P	29	1B	10	HSI1B_SINP	HSI1B_RXD9	FIFO1B_DIN9	P18
BK1_IO27	1	N	29	1B	11	HSI1B_SINN	HSI1B_RECCLK	-	N18
GND	1	-	-	-	-	-	-	-	GND
BK1_IO28	1	P	30	1B	12	-	HSI1B_CDRLOCK	FIFO1B_STRDb	R22
BK1_IO29	1	N	30	1B	13	HSI1B_CDRRSTb	-	FIFO1B_FIFORSTb	P22
BK1_IO30	1	P	31	1B	14	SS_CLKIN1P	-	-	M18
BK1_IO31/ CLK_OUT2	1	N	31	1B	15	SS_CLKIN1N	-	FIFO1B_EMPTY	M17
GCLK/CE2	-	P	CLK2	-	-	-	-	-	N20
SEL2	-	-	-	-	-	-	-	-	N21
SEL3	-	-	-	-	-	-	-	-	K21
GCLK/CE3	-	N	CLK2	-	-	-	-	-	K20
BK2_IO0/ CLK_OUT3	2	N	32	3A	0	SS_CLKOUT1N	-	FIFO3A_FULL	K17
BK2_IO1	2	P	32	3A	1	SS_CLKOUT1P	-	-	K18
BK2_IO2	2	N	33	3A	2	-	-	-	L17
BK2_IO3	2	P	33	3A	3	HSI3A_EXLOSS	HSI3A_RXD0	FIFO3A_DIN0	L18
GND	2	-	-	-	-	-	-	-	GND
BK2_IO4	2	N	34	3A	4	HSI3A_SINN	HSI3A_RXD1	FIFO3A_DIN1	J17
BK2_IO5	2	P	34	3A	5	HSI3A_SINP	HSI3A_RXD2	FIFO3A_DIN2	J18
BK2_IO6	2	N	35	3A	6	HSI3_CSLOCK	HSI3A_RXD3	FIFO3A_DIN3	J22
BK2_IO7	2	P	35	3A	7	-	HSI3A_RXD4	FIFO3A_DIN4	J20

ispGDX2-256 Logic Signal Connections<sup>1, 2</sup> (Continued)

Signal Name	sysIO Bank	LVDS Buffer		GDX Block	MRB	SERDES Mode I/O Functions	SERDES Mode SERDES to FIFO Core	FIFO Mode I/O Function	484 fpBGA
		Polarity	Pair						
BK2_IO8	2	N	36	3A	8	CAL	HSI3A_RXD5	FIFO3A_DIN5	H22
BK2_IO9	2	P	36	3A	9	HSI3A_LOSS	HSI3A_RXD6	FIFO3A_DIN6	H21
BK2_IO10	2	N	37	3A	10	HSI3A_SOUTN	HSI3A_RXD7	FIFO3A_DIN7	K16
BK2_IO11	2	P	37	3A	11	HSI3A_SOUTP	HSI3A_RXD8	FIFO3A_DIN8	J16
GND	2	-	-	-	-	-	-	-	GND
BK2_IO12	2	N	38	3A	12	HSI3A_SYDT	HSI3A_RXD9	FIFO3A_DIN9	J19
BK2_IO13	2	P	38	3A	13	HSI3A_CDRRSTb	HSI3A_RECCLK	FIFO3A_FIFORSTb	H20
BK2_IO14	2	N	39	3A	14	-	HSI3A_CDRLOCK	FIFO3A_STRDb	G21
BK2_IO15	2	P	39	3A	15	-	-	FIFO3A_EMPTY	G20
BK2_IO16	2	N	40	2A	0	-	-	FIFO2A_FULL	G22
BK2_IO17	2	P	40	2A	1	-	-	-	F22
BK2_IO18	2	N	41	2A	2	HSI2A_EXLOSS	HSI2A_RXD0	FIFO2A_DIN0	F20
BK2_IO19	2	P	41	2A	3	-	HSI2A_RXD1	FIFO2A_DIN1	F21
GND	2	-	-	-	-	-	-	-	GND
BK2_IO20/ PLL_FB3	2	N	42	2A	4	HSI2A_SOUTN	HSI2A_RXD2	FIFO2A_DIN2	H18
BK2_IO21/ VREF2	2	P	42	2A	5	HSI2A_SOUTP	HSI2A_RXD3	FIFO2A_DIN3	G17
BK2_IO22	2	N	43	2A	6	HSI2_CSLOCK	HSI2A_RXD4	FIFO2A_DIN4	E21
BK2_IO23	2	P	43	2A	7	-	HSI2A_RXD5	FIFO2A_DIN5	F19
BK2_IO24	2	N	44	2A	8	HSI2A_LOSS	HSI2A_RXD6	FIFO2A_DIN6	E22
BK2_IO25	2	P	44	2A	9	HSI2A_SYDT	HSI2A_RXD7	FIFO2A_DIN7	D22
BK2_IO26	2	N	45	2A	10	HSI2A_SINN	HSI2A_RXD8	FIFO2A_DIN8	H17
BK2_IO27	2	P	45	2A	11	HSI2A_SINP	HSI2A_RXD9	FIFO2A_DIN9	H16
BK2_IO28	2	N	46	2A	12	HSI2A_CDRRSTb	HSI2A_RECCLK	FIFO2A_FIFORSTb	E19
BK2_IO29	2	P	46	2A	13	-	HSI2A_CDRLOCK	FIFO2A_STRDb	F18
BK2_IO30	2	N	47	2A	14	-	-	-	D20
BK2_IO31	2	P	47	2A	15	-	-	FIFO2A_EMPTY	D21
GND	2	-	-	-	-	-	-	-	GND
TCK	-	-	-	-	-	-	-	-	B19
GOE2	-	-	-	-	-	-	-	-	C19
BK3_IO0	3	P	48	3B	0	-	-	FIFO3B_FULL	E17
BK3_IO1	3	N	48	3B	1	HSI3B_EXLOSS	HSI3B_RXD0	FIFO3B_DIN0	D18
BK3_IO2	3	P	49	3B	2	-	HSI3B_RXD1	FIFO3B_DIN1	A19
BK3_IO3	3	N	49	3B	3	-	HSI3B_RXD2	FIFO3B_DIN2	A18
GND	3	-	-	-	-	-	-	-	GND
BK3_IO4	3	P	50	3B	4	HSI3B_SINP	HSI3B_RXD3	FIFO3B_DIN3	G15
BK3_IO5	3	N	50	3B	5	HSI3B_SINN	HSI3B_RXD4	FIFO3B_DIN4	G14
BK3_IO6	3	P	51	3B	6	-	HSI3B_RXD5	FIFO3B_DIN5	D17
BK3_IO7	3	N	51	3B	7	HSI3B_SYDT	HSI3B_RXD6	FIFO3B_DIN6	D16
BK3_IO8	3	P	52	3B	8	-	HSI3B_RXD7	FIFO3B_DIN7	C18
BK3_IO9	3	N	52	3B	9	HSI3B_LOSS	HSI3B_RXD8	FIFO3B_DIN8	B18
BK3_IO10/ VREF3	3	P	53	3B	10	HSI3B_SOUTP	HSI3B_RXD9	FIFO3B_DIN9	F15
BK3_IO11	3	N	53	3B	11	HSI3B_SOUTN	HSI3B_RECCLK	-	F14
GND	3	-	-	-	-	-	-	-	GND
BK3_IO12	3	P	54	3B	12	-	HSI3B_CDRLOCK	FIFO3B_STRDb	B17

ispGDX2-256 Logic Signal Connections<sup>1, 2</sup> (Continued)

Signal Name	sysIO Bank	LVDS Buffer		GDX Block	MRB	SERDES Mode I/O Functions	SERDES Mode SERDES to FIFO Core	FIFO Mode I/O Function	484 fpBGA
		Polarity	Pair						
BK3_IO13	3	N	54	3B	13	HSI3B_CDRRSTb	HSI3B_RECCLK	FIFO3B_FIFORSTb	A17
BK3_IO14/ PLL_RST3	3	P	55	3B	14	-	-	-	A16
BK3_IO15	3	N	55	3B	15	-	-	FIFO3B_EMPTY	C16
BK3_IO16	3	P	56	2B	0	HSI2B_EXLOSS	HSI2B_RXD0	FIFO2B_DIN0	D15
BK3_IO17	3	N	56	2B	1	-	HSI2B_RXD1	FIFO2B_DIN1	D14
BK3_IO18	3	P	57	2B	2	-	HSI2B_RXD2	FIFO2B_DIN2	B16
BK3_IO19	3	N	57	2B	3	-	HSI2B_RXD3	FIFO2B_DIN3	C15
GND	3	-	-	-	-	-	-	-	GND
BK3_IO20	3	P	-	2B	4	HSI2B_SOUTP	HSI2B_RXD4	FIFO2B_DIN4	G13
BK3_IO21	3	N	58	2B	5	HSI2B_SOUTN	HSI2B_RXD5	FIFO2B_DIN5	G12
BK3_IO22	3	P	59	2B	6	-	HSI2B_RXD6	FIFO2B_DIN6	B15
BK3_IO23	3	N	59	2B	7	-	HSI2B_RXD7	FIFO2B_DIN7 / FIFO2B_STRDb	A15
BK3_IO24	3	P	60	2B	8	HSI2B_LOSS	HSI2B_RXD8	FIFO2B_DIN8	C14
BK3_IO25	3	N	60	2B	9	HSI2B_SYDT	HSI2B_RXD9	FIFO2B_DIN9	A14
BK3_IO26	3	P	61	2B	10	HSI2B_SINP	HSI2B_RECCLK	-	F13
BK3_IO27	3	N	61	2B	11	HSI2B_SINN	HSI2B_CDRLOCK	-	F12
GND	3	-	-	-	-	-	-	-	GND
BK3_IO28	3	P	62	2B	12	-	-	FIFO2B_FULL	D13
BK3_IO29	3	N	62	2B	13	HSI2B_CDRRSTb	-	FIFO2B_FIFORSTb	C13
BK3_IO30/ PLL_LOCK3	3	P	63	2B	14	-	-	-	B13
BK3_IO31	3	N	63	2B	15	-	-	FIFO2B_EMPTY	A13
RESETb	-	-	-	-	-	-	-	-	D12
BK4_IO0	4	N	64	4A	0	-	-	FIFO4A_EMPTY	A10
BK4_IO1/ PLL_LOCK0	4	P	64	4A	1	-	-	-	B10
BK4_IO2	4	N	65	4A	2	HSI4A_CDRRSTb	-	FIFO4A_FIFORSTb	E11
BK4_IO3	4	P	65	4A	3	-	-	FIFO4A_FULL	E10
GND	4	-	-	-	-	-	-	-	GND
BK4_IO4	4	N	66	4A	4	HSI4A_SINN	HSI4A_CDRLOCK	-	F11
BK4_IO5	4	P	66	4A	5	HSI4A_SINP	HSI4A_RECCLK	-	F10
BK4_IO6	4	N	67	4A	6	HSI4A_SYDT	HSI4A_RXD9	FIFO4A_DIN9	C10
BK4_IO7	4	P	67	4A	7	HSI4A_LOSS	HSI4A_RXD8	FIFO4A_DIN8	C9
BK4_IO8	4	N	68	4A	8	-	HSI4A_RXD7	FIFO4A_DIN7 / FIFO4A_STRDb	D10
BK4_IO9/ PLL_FB0	4	P	68	4A	9	-	HSI4A_RXD6	FIFO4A_DIN6	D9
BK4_IO10	4	N	69	4A	10	HSI4A_SOUTN	HSI4A_RXD5	FIFO4A_DIN5	G11
BK4_IO11	4	P	69	4A	11	HSI4A_SOUTP	HSI4A_RXD4	FIFO4A_DIN4	G10
GND	4	-	-	-	-	-	-	-	GND
BK4_IO12	4	N	70	4A	12	-	HSI4A_RXD3	FIFO4A_DIN3	A9
BK4_IO13	4	P	70	4A	13	-	HSI4A_RXD2	FIFO4A_DIN2	C8
BK4_IO14	4	N	71	4A	14	-	HSI4A_RXD1	FIFO4A_DIN1	B8
BK4_IO15	4	P	71	4A	15	HSI4A_EXLOSS	HSI4A_RXD0	FIFO4A_DIN0	A8
BK4_IO16	4	N	72	5A	0	-	-	FIFO5A_EMPTY	B7

ispGDX2-256 Logic Signal Connections<sup>1, 2</sup> (Continued)

Signal Name	sysIO Bank	LVDS Buffer		GDX Block	MRB	SERDES Mode I/O Functions	SERDES Mode SERDES to FIFO Core	FIFO Mode I/O Function	484 fpBGA
		Polarity	Pair						
BK4_IO17/ PLL_RST0	4	P	72	5A	1	-	-	-	C7
BK4_IO18	4	N	73	5A	2	HSI5A_CDRRSTb	-	FIFO5A_FIFORSTb	A7
BK4_IO19	4	P	73	5A	3	-	HSI5A_CDRLOCK	FIFO5A_STRDb	B6
GND	4	-	-	-	-	-	-	-	GND
BK4_IO20	4	N	74	5A	4	HSI5A_SOUTN	HSI5A_RECCLK	-	F9
BK4_IO21/ VREF4	4	P	74	5A	5	HSI5A_SOUTP	HSI5A_RXD9	FIFO5A_DIN9	F8
BK4_IO22	4	N	75	5A	6	HSI5A_LOSS	HSI5A_RXD8	FIFO5A_DIN8	D7
BK4_IO23	4	P	75	5A	7	-	HSI5A_RXD7	FIFO5A_DIN7	D6
BK4_IO24	4	N	76	5A	8	HSI5A_SYDT	HSI5A_RXD6	FIFO5A_DIN6	A6
BK4_IO25	4	P	76	5A	9	-	HSI5A_RXD5	FIFO5A_DIN5	A5
BK4_IO26	4	N	77	5A	10	HSI5A_SINN	HSI5A_RXD4	FIFO5A_DIN4	G9
BK4_IO27	4	P	77	5A	11	HSI5A_SINP	HSI5A_RXD3	FIFO5A_DIN3	G8
BK4_IO28	4	N	78	5A	12	-	HSI5A_RXD2	FIFO5A_DIN2	C5
BK4_IO29	4	P	78	5A	13	-	HSI5A_RXD1	FIFO5A_DIN1	B5
BK4_IO30	4	N	79	5A	14	HSI5A_EXLOSS	HSI5A_RXD0	FIFO5A_DIN0	D5
BK4_IO31	4	P	79	5A	15	-	-	FIFO5A_FULL	C4
GND	4	-	-	-	-	-	-	-	GND
GOE1	-	-	-	-	-	-	-	-	B4
TMS	-	-	-	-	-	-	-	-	A4
GND	5	-	-	-	-	-	-	-	GND
BK5_IO0	5	P	80	4B	0	-	-	FIFO4B_EMPTY	D2
BK5_IO1	5	N	80	4B	1	-	-	-	D3
BK5_IO2	5	P	81	4B	2	-	HSI4B_CDRLOCK	FIFO4B_STRDb	F5
BK5_IO3	5	N	81	4B	3	HSI4B_CDRRSTb	HSI4B_RECCLK	FIFO4B_FIFORSTb	E4
BK5_IO4	5	P	82	4B	4	HSI4B_SINP	HSI4B_RXD9	FIFO4B_DIN9	J7
BK5_IO5	5	N	82	4B	5	HSI4B_SINN	HSI4B_RXD8	FIFO4B_DIN8	J6
BK5_IO6	5	P	83	4B	6	HSI4B_SYDT	HSI4B_RXD7	FIFO4B_DIN7	D1
BK5_IO7	5	N	83	4B	7	HSI4B_LOSS	HSI4B_RXD6	FIFO4B_DIN6	E1
BK5_IO8	5	P	84	4B	8	-	HSI4B_RXD5	FIFO4B_DIN5	F4
BK5_IO9	5	N	84	4B	9	HSI4_CSLOCK	HSI4_RXD4	FIFO4B_DIN4	E3
BK5_IO10/ VREF5	5	P	85	4B	10	HSI4B_SOUTP	HSI4B_RXD3	FIFO4B_DIN3	H7
BK5_IO11	5	N	85	4B	11	HSI4B_SOUTN	HSI4B_RXD2	FIFO4B_DIN2	H6
GND	5	-	-	-	-	-	-	-	GND
BK5_IO12	5	P	86	4B	12	-	HSI4B_RXD1	FIFO4B_DIN1	E2
BK5_IO13	5	N	86	4B	13	HSI4B_EXLOSS	HSI4B_RXD0	FIFO4B_DIN0	F2
BK5_IO14	5	P	87	4B	14	-	-	-	G4
BK5_IO15	5	N	87	4B	15	-	-	FIFO4B_FULL	H5
BK5_IO16	5	P	88	5B	0	-	-	FIFO5B_EMPTY	F1
BK5_IO17	5	N	88	5B	1	-	HSI5B_CDRLOCK	FIFO5B_STRDb	G1
BK5_IO18	5	P	89	5B	2	HSI5B_CDRRSTb	HSI5B_RECCLK	FIFO5B_FIFORSTb	G3
BK5_IO19	5	N	89	5B	3	HSI5B_SYDT	HSI5B_RXD9	FIFO5B_DIN9	G2
GND	5	-	-	-	-	-	-	-	GND
BK5_IO20	5	P	90	5B	4	HSI5B_SOUTP	HSI5B_RXD8	FIFO5B_DIN8	K7
BK5_IO21	5	N	90	5B	5	HSI5B_SOUTN	HSI5B_RXD7	FIFO5B_DIN7	K6

ispGDX2-256 Logic Signal Connections<sup>1, 2</sup> (Continued)

Signal Name	sysIO Bank	LVDS Buffer		GDX Block	MRB	SERDES Mode I/O Functions	SERDES Mode SERDES to FIFO Core	FIFO Mode I/O Function	484 fpBGA
		Polarity	Pair						
BK5_IO22	5	P	91	5B	6	HSI5B_LOSS	HSI5B_RXD6	FIFO5B_DIN6	H4
BK5_IO23	5	N	91	5B	7	-	HSI5B_RXD5	FIFO5B_DIN5	H3
BK5_IO24	5	P	92	5B	8	-	HSI5B_RXD4	FIFO5B_DIN4	H1
BK5_IO25	5	N	92	5B	9	HSI5_CSLOCK	HSI5B_RXD3	FIFO5B_DIN3	H2
BK5_IO26	5	P	93	5B	10	HSI5B_SINP	HSI5B_RXD2	FIFO5B_DIN2	J5
BK5_IO27	5	N	93	5B	11	HSI5B_SINN	HSI5B_RXD1	FIFO5B_DIN1	K5
GND	5	-	-	-	-	-	-	-	GND
BK5_IO28	5	P	94	5B	12	HSI5B_EXLOSS	HSI5B_RXD0	FIFO5B_DIN0	J4
BK5_IO29	5	N	94	5B	13	-	-	-	J3
BK5_IO30	5	P	95	5B	14	SS_CLKIN0P	-	-	L6
BK5_IO31/ CLK_OUT0	5	N	95	5B	15	SS_CLKIN0N	-	FIFO5B_FULL	L5
GCLK/CE0	-	P	CLK0	-	-	-	-	-	L4
SEL0	-	-	-	-	-	-	-	-	K3
SEL1	-	-	-	-	-	-	-	-	K2
GCLK/CE1	-	N	CLK0	-	-	-	-	-	N1
BK6_IO0/ CLK_OUT1	6	N	96	7A	0	SS_CLKOUT0N	-	FIFO7A_EMPTY	N6
BK6_IO1	6	P	96	7A	1	SS_CLKOUT0P	-	-	N5
BK6_IO2	6	N	97	7A	2	HSI7A_CDRRST	-	FIFO7A_FIFORSTb	M5
BK6_IO3	6	P	97	7A	3	-	HSI7A_CDRLOCK	FIFO7A_STRDb	M6
GND	6	-	-	-	-	-	-	-	GND
BK6_IO4	6	N	98	7A	4	HSI7A_SINN	HSI7A_RECCLK	-	P6
BK6_IO5	6	P	98	7A	5	HSI7A_SINP	HSI7A_RXD9	FIFO7A_DIN9	P5
BK6_IO6	6	N	99	7A	6	HSI7A_LOSS	HSI7A_RXD8	FIFO7A_DIN8	N3
BK6_IO7	6	P	99	7A	7	-	HSI7A_RXD7	FIFO7A_DIN7	N2
BK6_IO8	6	N	100	7A	8	HSI7A_SYDT	HSI7A_RXD6	FIFO7A_DIN6	P3
BK6_IO9	6	P	100	7A	9	HSI7_CSLOCK	HSI7A_RXD5	FIFO7A_DIN5	P1
BK6_IO10	6	N	101	7A	10	HSI7A_SOUTN	HSI7A_RXD4	FIFO7A_DIN4	N7
BK6_IO11	6	P	101	7A	11	HSI7A_SOUTP	HSI7A_RXD3	FIFO7A_DIN3	P7
GND	6	-	-	-	-	-	-	-	GND
BK6_IO12	6	N	102	7A	12	-	HSI7A_RXD2	FIFO7A_DIN2	R3
BK6_IO13	6	P	102	7A	13	-	HSI7A_RXD1	FIFO7A_DIN1	R2
BK6_IO14	6	N	103	7A	14	HSI7A_EXLOSS	HSI7A_RXD0	FIFO7A_DIN0	R1
BK6_IO15	6	P	103	7A	15	-	-	FIFO7A_FULL	T1
BK6_IO16	6	N	104	6A	0	-	-	FIFO6A_EMPTY	T2
BK6_IO17	6	P	104	6A	1	-	-	-	T3
BK6_IO18	6	N	105	6A	2	-	HSI6A_CDRLOCK	FIFO6A_STRDb	U1
BK6_IO19	6	P	105	6A	3	HSI6A_CDRRSTb	HSI6_RECCLK	FIFO6A_FIFORSTb	U2
GND	6	-	-	-	-	-	-	-	GND
BK6_IO20/ PLL_FB1	6	N	106	6A	4	HSI6A_SOUTN	HSI6A_RXD9	FIFO6A_DIN9	R5
BK6_IO21/ VREF6	6	P	106	6A	5	HSI6A_SOUTP	HSI6A_RXD8	FIFO6A_DIN8	T6
BK6_IO22	6	N	107	6A	6	HSI6A_SYDT	HSI6A_RXD7	FIFO6A_DIN7	U4
BK6_IO23	6	P	107	6A	7	HSI6A_LOSS	HSI6A_RXD6	FIFO6A_DIN6	V4
BK6_IO24	6	N	108	6A	8	-	HSI6A_RXD5	FIFO6A_DIN5	V3

ispGDX2-256 Logic Signal Connections<sup>1, 2</sup> (Continued)

Signal Name	sysIO Bank	LVDS Buffer		GDX Block	MRB	SERDES Mode I/O Functions	SERDES Mode SERDES to FIFO Core	FIFO Mode I/O Function	484 fpBGA
		Polarity	Pair						
BK6_IO25	6	P	108	6A	9	HSI6_CSLOCK	HSI6A_RXD4	FIFO6A_DIN4	V2
BK6_IO26	6	N	109	6A	10	HSI6A_SINN	HSI6A_RXD3	FIFO6A_DIN3	R6
BK6_IO27	6	P	109	6A	11	HSI6A_SINP	HSI6A_RXD2	FIFO6A_DIN2	R7
BK6_IO28	6	N	110	6A	12		HSI6A_RXD1	FIFO6A_DIN1	W1
BK6_IO29	6	P	110	6A	13	HSI6A_EXLOSS	HSI6A_RXD0	FIFO6A_DIN0	V1
BK6_IO30	6	N	111	6A	14	-	-	-	W2
BK6_IO31	6	P	111	6A	15	-	-	FIFO6A_FULL	W3
GND	6	-	-	-	-	-	-	-	GND
TDI	-	-	-	-	-	-	-	-	AA4
GOE0	-	-	-	-	-	-	-	-	Y4
GND	7	-	-	-	-	-	-	-	GND
BK7_IO0	7	P	112	7B	0	-	-	FIFO7B_EMPTY	AB4
BK7_IO1	7	N	112	7B	1	-	HSI7B_CDRLOCK	FIFO7B_STRDb	AB5
BK7_IO2	7	P	113	7B	2	HSI7B_CDRRSTb	HSI7B_RECCLK	FIFO7B_FIFORSTb	V6
BK7_IO3	7	N	113	7B	3	HSI7B_SYDT	HSI7B_RXD9	FIFO7B_DIN9	W5
BK7_IO4	7	P	114	7B	4	HSI7B_SINP	HSI7B_RXD8	FIFO7B_DIN8	T8
BK7_IO5	7	N	114	7B	5	HSI7B_SINN	HSI7B_RXD7	FIFO7B_DIN7	T9
BK7_IO6	7	P	115	7B	6	HSI7B_LOSS	HSI7B_RXD6	FIFO7B_DIN6	W6
BK7_IO7	7	N	115	7B	7	-	HSI7B_RXD5	FIFO7B_DIN5	Y5
BK7_IO8	7	P	116	7B	8	-	HSI7B_RXD4	FIFO7B_DIN4	AA5
BK7_IO9	7	N	116	7B	9	-	HSI7B_RXD3	FIFO7B_DIN3	AA6
BK7_IO10/ VREF7	7	P	117	7B	10	HSI7B_SOUTP	HSI7B_RXD2	FIFO7B_DIN2	U8
BK7_IO11	7	N	117	7B	11	HSI7B_SOUTN	HSI7B_RXD1	FIFO7B_DIN1	U9
GND	7	-	-	-	-	-	-	-	GND
BK7_IO12	7	P	118	7B	12	HSI7B_EXLOSS	HSI7B_RXD0	FIFO7B_DIN0	W7
BK7_IO13	7	N	118	7B	13	-	-	-	W8
BK7_IO14/ PLL_RST1	7	P	119	7B	14	-	-	-	AB6
BK7_IO15	7	N	119	7B	15	-	-	FIFO7B_FULL	AB7
BK7_IO16	7	P	120	6B	0	-	HSI6B_CDRLOCK	FIFO6B_STRDb	Y7
BK7_IO17	7	N	120	6B	1	HSI6B_CDRRSTb	HSI6B_RECCLK	FIFO6B_FIFORSTb	AA7
BK7_IO18	7	P	121	6B	2	HSI6B_SYDT	HSI6B_RXD9	FIFO6B_DIN9	W9
BK7_IO19	7	N	121	6B	3	HSI6B_LOSS	HSI6B_RXD8	FIFO6B_DIN8	Y8
GND	7	-	-	-	-	-	-	-	GND
BK7_IO20	7	P	122	6B	4	HSI6B_SOUTP	HSI6B_RXD7	FIFO6B_DIN7	T10
BK7_IO21	7	N	122	6B	5	HSI6B_SOUTN	HSI6B_RXD6	FIFO6B_DIN6	T11
BK7_IO22	7	P	123	6B	6	-	HSI6B_RXD5	FIFO6B_DIN5	AA8
BK7_IO23	7	N	123	6B	7	-	HSI6B_RXD4	FIFO6B_DIN4	AB8
BK7_IO24	7	P	124	6B	8	-	HSI6B_RXD3	FIFO6B_DIN3	W10
BK7_IO25	7	N	124	6B	9	-	HSI6B_RXD2	FIFO6B_DIN2	Y9
BK7_IO26	7	P	125	6B	10	HSI6B_SINP	HSI6B_RXD1	FIFO6B_DIN1	U10
BK7_IO27	7	N	125	6B	11	HSI6B_SINN	HSI6B_RXD0	FIFO6B_DIN0	U11
GND	7	-	-	-	-	-	-	-	GND
BK7_IO28	7	P	126	6B	12	-	-	FIFO6B_EMPTY	W11
BK7_IO29/ PLL_LOCK1	7	N	126	6B	13	-	-	-	Y10

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**ispGDX2-256 Logic Signal Connections<sup>1, 2</sup> (Continued)**

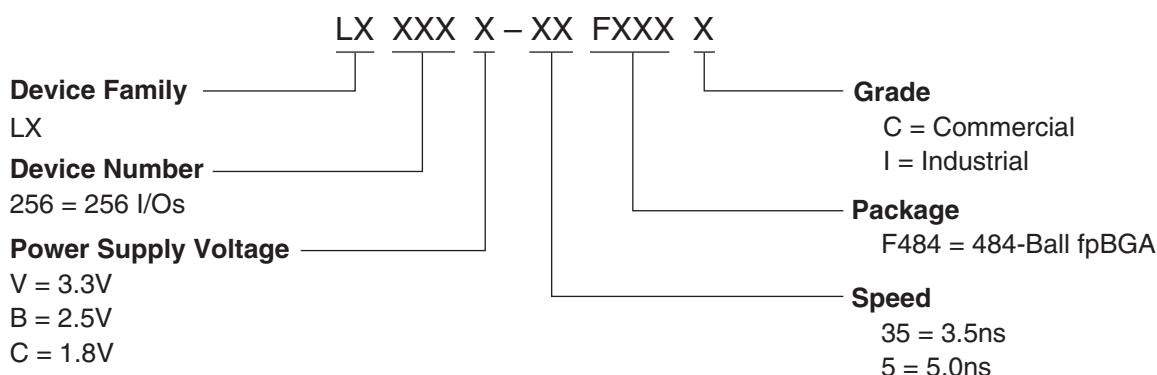
Signal Name	sysIO Bank	LVDS Buffer		GDX Block	MRB	SERDES Mode I/O Functions	SERDES Mode SERDES to FIFO Core	FIFO Mode I/O Function	484 fpBGA
		Polarity	Pair						
BK7_IO30	7	P	127	6B	14	-	-	-	AA10
BK7_IO31	7	N	127	6B	15	-	-	FIFO6B_FULL	AB9
TOE	-	-	-	-	-	-	-	-	AB10

1. FIFO DOUT signals are associated with same pins as their respective FIFO DIN signals.

2. SERDES DIN signals are associated with the same pins as their respective SERDES DOUT signals.



## Part Number Description



## Ordering Information

### Commercial

Part Number	I/Os	Voltage	t <sub>PD</sub>	Package	Pins
LX256V-35F484C	256	3.3	3.5	fpBGA	484
LX256V-5F484C	256	3.3	5.0	fpBGA	484
LX256B-35F484C	256	2.5	3.5	fpBGA	484
LX256B-5F484C	256	2.5	5.0	fpBGA	484
LX256C-35F484C	256	1.8	3.5	fpBGA	484
LX256C-5F484C	256	1.8	5.0	fpBGA	484

Note: the ispGDX2 family is dual-marked with both Commercial and Industrial grades. The Commercial speed grade is one speed grade faster (i.e. LX256V-35F484C) than the Industrial speed grade (i.e. LX256V-5F484I).

### Industrial

Part Number	I/Os	Voltage	t <sub>PD</sub>	Package	Pins
LX256V-5F484I	256	3.3	5.0	fpBGA	484
LX256B-5F484I	256	2.5	5.0	fpBGA	484
LX256C-5F484I	256	1.8	5.0	fpBGA	484

Note: the ispGDX2 family is dual-marked with both Commercial and Industrial grades. The Commercial speed grade is one speed grade faster (i.e. LX256V-35F484C) than the Industrial speed grade (i.e. LX256V-5F484I).

## For Further Information

In addition to this data sheet, the following Lattice technical notes may be helpful when designing with the ispGDX2 Family:

- *sysIO Design and Usage Guidelines* (TN1000)
- *sysCLOCK PLL Design and Usage Guidelines* (TN1003)
- *sysHSI Usage Guide* (TN1020)
- *Power Estimation in ispGDX2 Devices* (TN1021)