Isolated Secondary Synchronous Rectifier Controller

FEATURES

- **High Efficiency Over Wide Load Current Range**
- **±0.8% Output Voltage Accuracy**
- Dual N-Channel MOSFET Synchronous Drivers
- Pulse Transformer Synchronization
- Optocoupler Feedback Driver
- Programmable Current Limit Protection
- ±5% Margin Output Voltage Adjustment
- Adjustable Overvoltage Fault Protection
- Power Good Flag
- Auxiliary 3.3V Logic Supply
- Available in 16-Lead SSOP and SO Packages

APPLICATIONS

- 48V Input Isolated DC/DC Converters
- Isolated Telecommunication Power Systems
- Distributed Power Step-Down Converters
- Industrial Control Systems
- Automotive and Heavy Equipment

DESCRIPTION

The LTC®1698 is a precision secondary-side forward converter controller that synchronously drives external N-channel MOSFETs. It is designed for use with the LT®3781 primary-side synchronous forward converter controller to create a completely isolated power supply. The LT3781 synchronizes the LTC1698 through a small pulse transformer and the LTC1698 drives a feedback optocoupler to close the feedback loop. Output accuracy of ±0.8% and high efficiency over a wide range of load currents are obtained.

The LTC1698 provides accurate secondary-side current limit using an external current sense resistor. The input voltage at the MARGIN pin provides ±5% output voltage adjustment. A power good flag and overvoltage input are provided to ensure proper power supply conditions. An auxiliary 3.3V logic supply is included that supplies up to 10mA of output current.

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TYPICAL APPLICATION

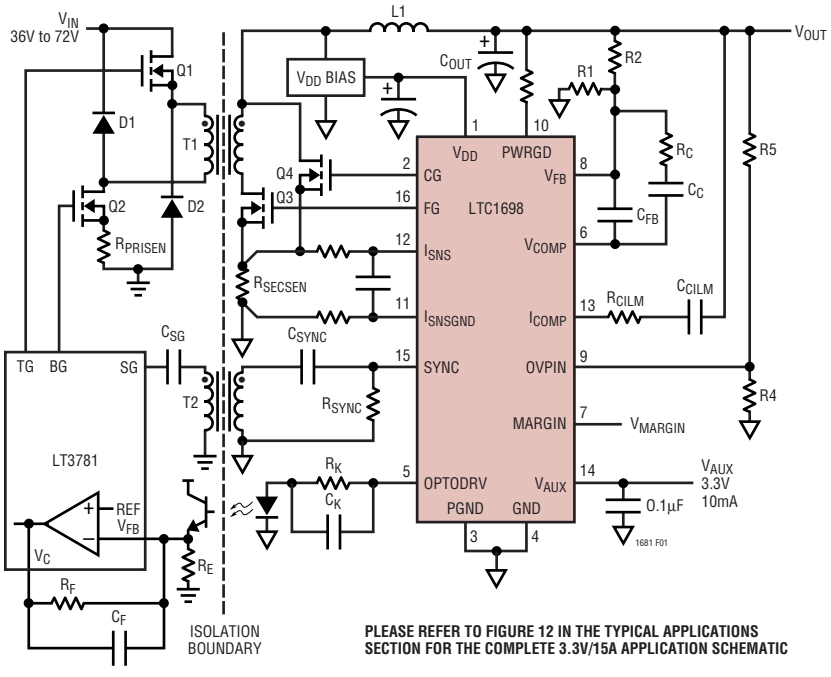


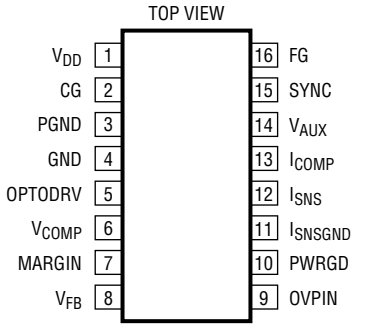
Figure 1. Simplified 2-Transistor Isolated Forward Converter

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{DD}, PWRGD 13.2V
Input Voltage
MARGIN, V_{FB}, OVPIN, I_{SNSGND}, I_{SNS} ... –0.3V to 5.3V
SYNC ..... –14V to 14V
Output Voltage
V_{COMP}, I_{COMP} (Note 2) ..... –0.3V to 5.3V
Power Dissipation 500mW
Operating Temperature Range
LTC1698E (Note 3) ..... –40°C to 85°C
LTC1698I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
16-LEAD PLASTIC SSOP

S PACKAGE
16-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 130°C/W (GN)
T_{JMAX} = 125°C, θ_{JA} = 110°C/W (SO)

ORDER PART NUMBER
LTC1698EGN LTC1698ES LTC1698IGN LTC1698IS
GN PART MARKING
1698 1698I

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 8V, unless otherwise noted. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Supply Voltage		●	6	8	12.6	V
V_{UVLO}	Undervoltage Lockout				4		V
I_{VDD}	V_{DD} Supply Current	V_{FB}, OVPIN, V_{ISNS}, $V_{ISNSGND}$ = 0V, C_{FG} = C_{CG} = 1000pF, C_{VAUX} = 0.1µF, V_{SYNC} = 0V	●		1.8	4	mA
		f_{SYNC} = 100kHz (Note 5)			5.0		mA
MARGIN and Error Amplifier							
V_{FB}	Feedback Voltage	MARGIN = Open, V_{COMP} = 1V (Note 7)	 ●	1.223 1.215	1.233 1.233	1.243 1.251	V V
I_{VFB}	Feedback Input Current	V_{FB} = 1.233V	●		0.05	1	µA
V_{MARGIN}	MARGIN Voltage	MARGIN = Open			1.65		V
R_{MARGIN}	MARGIN Input Resistance				16.5		kΩ
ΔV_{FB}	Feedback Voltage Adjustment	V_{MARGIN} = 3.3V V_{MARGIN} = 0V	● ●	4 –6	5 –5	6 –4	% %
G_{ERR}	Error Amplifier Open-Loop DC Gain	V_{COMP} = 0.8V to 1.2V, Load = 2kΩ, 100pF	●	65	90		dB
BW_{ERR}	Error Amplifier Unity-Gain Bandwidth	No Load (Note 6)			2		MHz
V_{CLAMP}	Error Amplifier Output Clamp Voltage	V_{FB} = 0V			2		V
I_{VCOMP}	Error Amplifier Source Current Error Amplifier Sink Current	V_{FB} = 0V V_{FB} = 5V, V_{COMP} = 1.233V	● ●	 3	–25 7	–10	mA mA
OPTODRV							
G_{OPTO}	Opto Driver DC Gain	OVPIN, V_{ISNS}, $V_{ISNSGND}$ = 0V	●	4.75	5	5.25	V/V
BW_{OPTO}	Opto Driver Unity-Gain Bandwidth	No Load (Note 6)			1		MHz
$V_{OPTOHIGH}$	Opto Driver Output High Voltage	V_{FB}, OVPIN, $V_{ISNSGND}$ = 0V, V_{ISNS} = –50mV, $I_{OPTODRV}$ = –10mA	●	4	5		V
I_{OPTOSC}	Opto Driver Output Short-Circuit Current	OVPIN, $V_{ISNSGND}$, V_{ISNS} = 0V, V_{FB} = 1.233V	●	–50	–25	–10	mA

ELECTRICAL CHARACTERISTICS

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 8V, unless otherwise noted. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{AUX}							
V_{AUX}	Auxiliary Supply Voltage	C_{VAUX} = 0.1µF, I_{LOAD} = 0mA to 10mA, V_{DD} = 7V to 12.6V	●	3.135	3.320	3.465	V
Current Limit Amplifier							
$I_{ISNSGND}$	I_{SNSGND} Input Current	$V_{ISNSGND}$ = 0V	●		0.05	1	µA
I_{ISNS}	I_{SNS} Input Current	V_{ISNS} = 0V	●		0.05	1	µA
V_{ILIMTH}	Current Limit Threshold (V_{ISNS} – $V_{ISNSGND}$)	V_{ICOMP} = 2.5V, $V_{ISNSGND}$ = 0V	 ●	–27.0 –27.5	–25 –25	–23.0 –22.5	mV mV
I_{ICOMP}	I_{COMP} Source Current	$V_{ISNSGND}$ = 0V, V_{ISNS} = –0.3V, V_{ICOMP} = 2.5V (Note 8)	 ●	–280 –370	–200 –200	–120 –80	µA µA
	I_{COMP} Sink Current	$V_{ISNSGND}$ = 0V, V_{ISNS} = 0.3V, V_{ICOMP} = 2.5V (Note 8)	 ●	120 80	200 200	280 370	µA µA
g_{mILIM}	Current Limit Amplifier Transconductance	$V_{ISNSGND}$ = 0V, V_{ICOMP} = 2.5V, I_{ICOMP} = ±10µA	●	2.2	3.5	5	millimho
G_{ICOMP}	Current Limit Amplifier Open-Loop DC Gain	V_{ICOMP} = 2.5V, No Load	●	48	60		dB
PWRGD and OVP Comparators							
V_{PWRGD}	Percent Below V_{FB}	V_{FB} ↓, MARGIN = Open (Note 9)	●	–9	–6	–3	%
I_{PWRGD}	Power Good Sink Current	V_{FB} = 2V V_{FB} = 0V	● ●	 10		10	µA mA
V_{OL}	Power Good Output Low Voltage	I_{PWRGD} = 3mA, V_{FB} = 0V	●			0.4	V
V_{OVPREF}	OVPIN Threshold	V_{FB} = V_{ISNS} = $V_{ISNSGND}$ = 0V, OVPIN ↑ (Note 9)	●	1.18	1.233	1.28	V
I_{OVPIN}	OVPIN Input Bias Current	V_{OVPIN} = 1.233V	●		0.1	1	µA
t_{PWRGD}	Power Good Response Time Power Bad Response Time	V_{FB} ↑ V_{FB} ↓	● ●	1 0.5	2 1	5 2.5	ms ms
t_{OVP}	Overvoltage Response Time	V_{OVPIN} ↑, $C_{OPTODRV}$ = 0.1µF	●		5	20	µs
SYNC and Drivers							
V_{PT}	SYNC Input Positive Threshold		●	1	1.6	2.2	V
V_{NT}	SYNC Input Negative Threshold		●	–2.2	–1.6	–1	V
I_{SYNC}	SYNC Input Current	V_{SYNC} = ±10V	●		1	50	µA
f_{SYNC}	SYNC Frequency Range	C_{FG} = C_{CG} = 1000pF, V_{SYNC} = ±5V	●	50		400	kHz
t_d	SYNC Input to Driver Output Delay	C_{FG} = C_{CG} = 1000pF, f_{SYNC} = 100kHz, V_{SYNC} = ±5V	●		40	90	ns
t_{SYNC}	Minimum SYNC Pulse Width	f_{SYNC} = 100kHz, V_{SYNC} = ±10V (Note 6)	●	75			ns
t_r, t_f	Driver Rise and Fall Time	C_{FG} = C_{CG} = 1000pF, f_{SYNC} = 100kHz, V_{SYNC} = ±5V, 10% to 90%	●		10	40	ns
t_{DDIS}	Driver Disable Time-Out	C_{FG} = C_{CG} = 1000pF, f_{SYNC} = 100kHz, V_{SYNC} = ±5V Measured from CG ↑ (Note 10)	●	10	15	20	µs

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. All voltages refer to GND.

Note 2: The LTC1698 incorporates a 5V linear regulator to power internal circuitry. Driving these pins above 5.3V may cause excessive current flow. Guaranteed by design and not subject to test.

Note 3: The LTC1698E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls. For guaranteed performance to specifications over the –40°C to 85°C range, the LTC1698I is available.

Note 4: All currents into device pins are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified. For applications with V_{DD} < 7V, refer to the Typical Performance Characteristics.

Note 5: Supply current in active operation is dominated by the current needed to charge and discharge the external FET gates. This will vary with the LTC1698 operating frequency, supply voltage and the external FETs used.

Note 6: This parameter is guaranteed by correlation and is not tested.

Note 7: V_{FB} is tested in an op amp feedback loop which servos V_{FB} to the internal bandgap voltage.

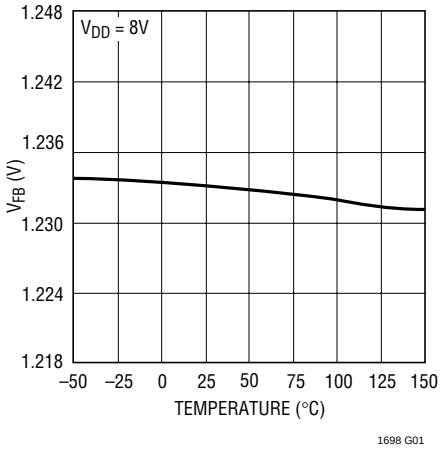
Note 8: The current comparator output current varies linearly with temperature.

Note 9: The PWRGD and OVP comparators incorporate 10mV of hysteresis.

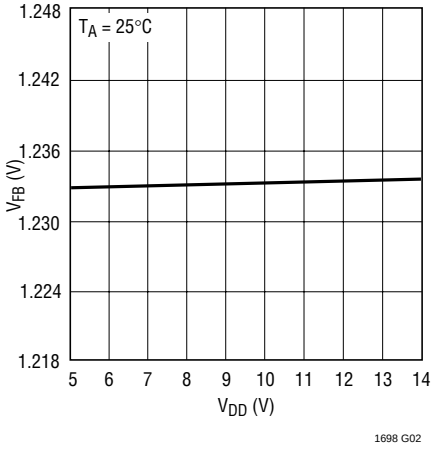
Note 10: The driver disable time-out is proportional to the SYNC period within the frequency synchronization range.

TYPICAL PERFORMANCE CHARACTERISTICS

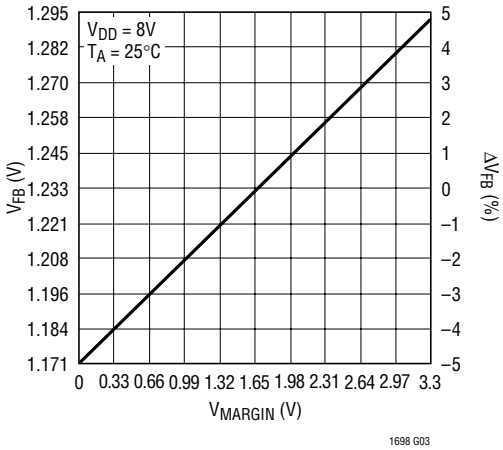
V_{FB} vs Temperature



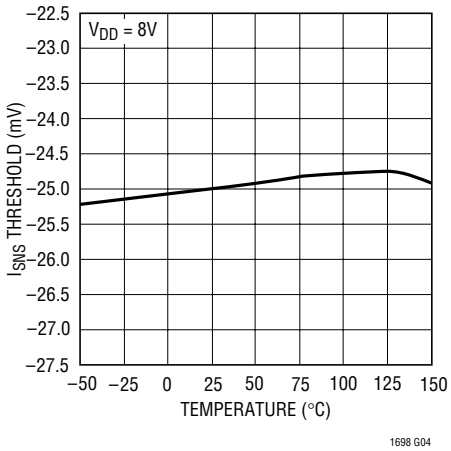
V_{FB} vs V_{DD}



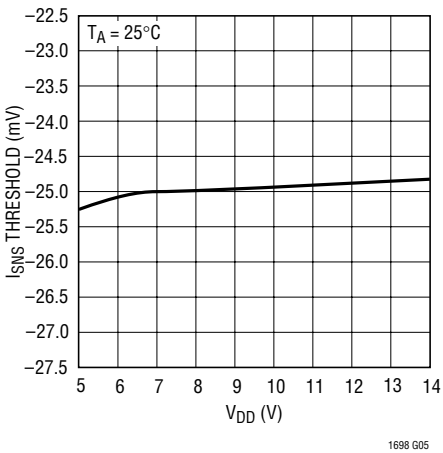
V_{FB} vs V_{MARGIN}



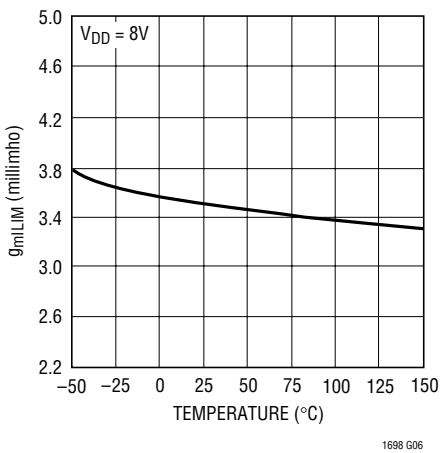
I_{SNS} Threshold vs Temperature



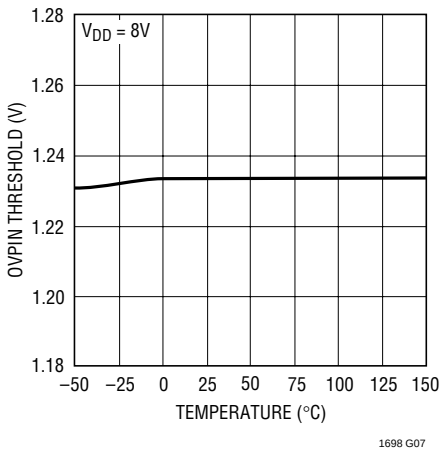
I_{SNS} Threshold vs V_{DD}



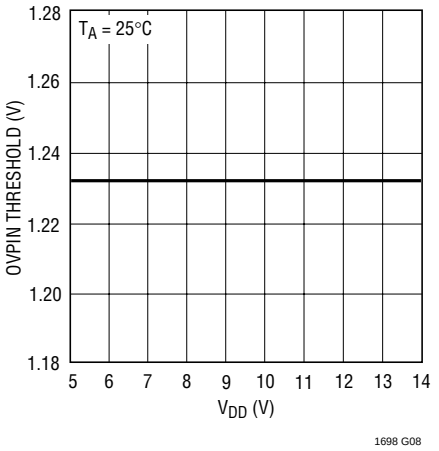
Current Limit Amplifier g_m vs Temperature



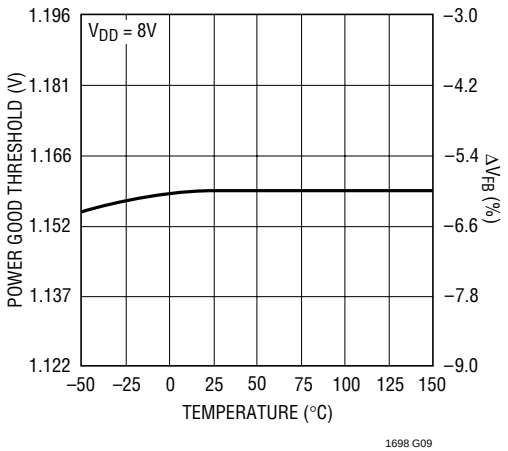
OVPIN Threshold vs Temperature



OVPIN Threshold vs V_{DD}

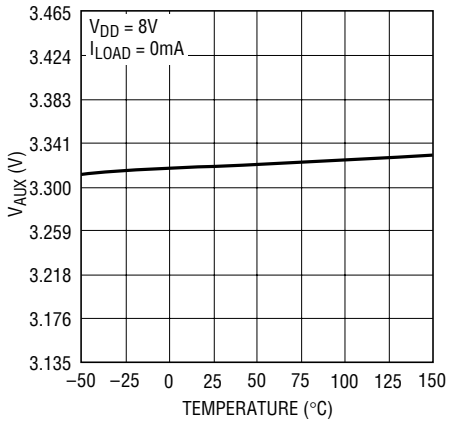


Power Good Threshold vs Temperature

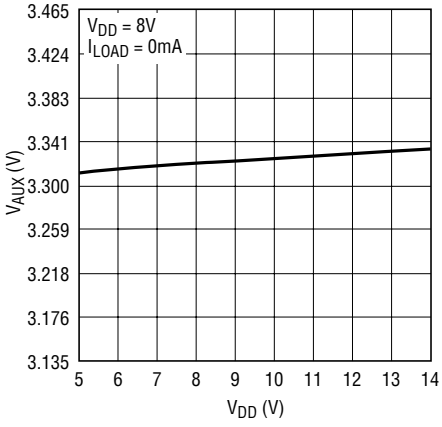


TYPICAL PERFORMANCE CHARACTERISTICS

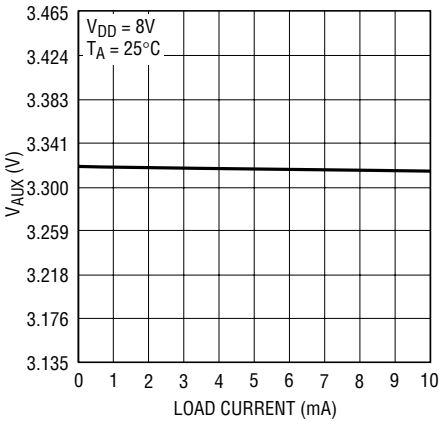
V_{AUX} vs Temperature



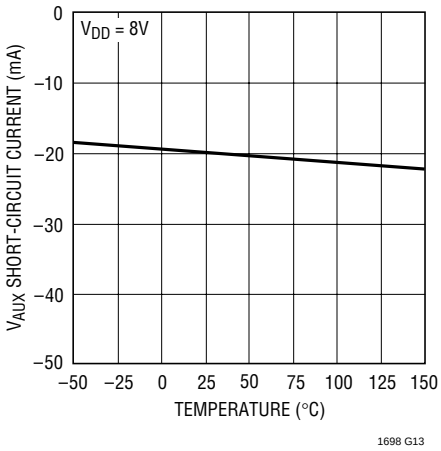
V_{AUX} vs Line Voltage



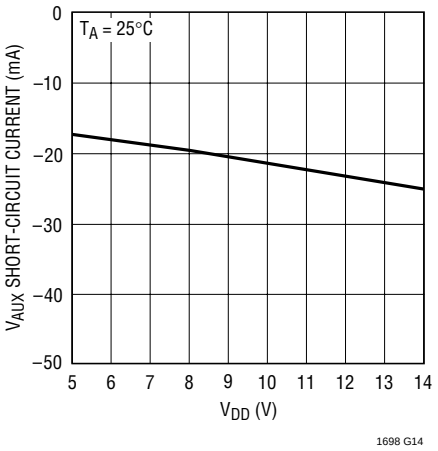
V_{AUX} vs Load Current



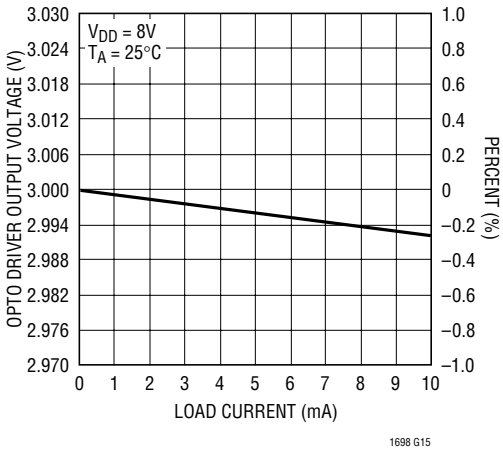
V_{AUX} Short-Circuit Current vs Temperature



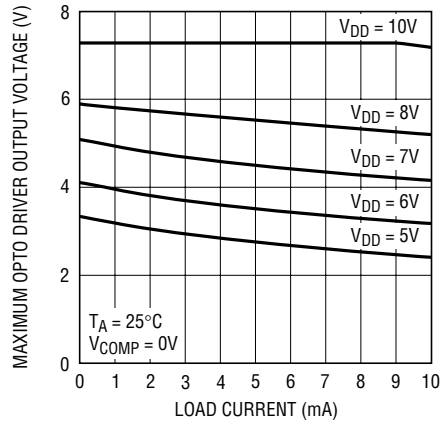
V_{AUX} Short-Circuit Current vs V_{DD}



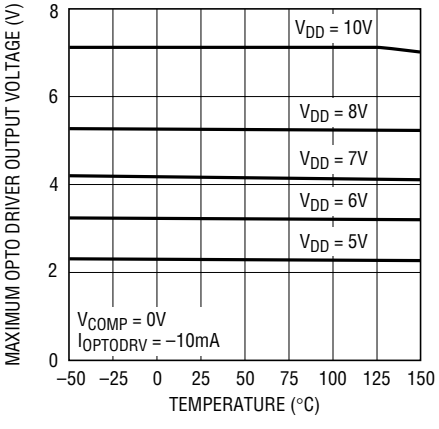
Opto Driver Load Regulation



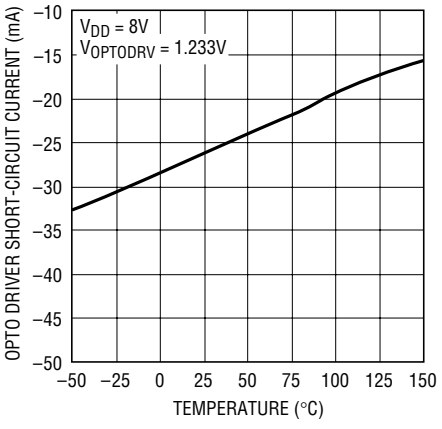
Maximum OPTO Driver Output Voltage vs Load Current



Maximum OPTO Driver Output Voltage vs Temperature

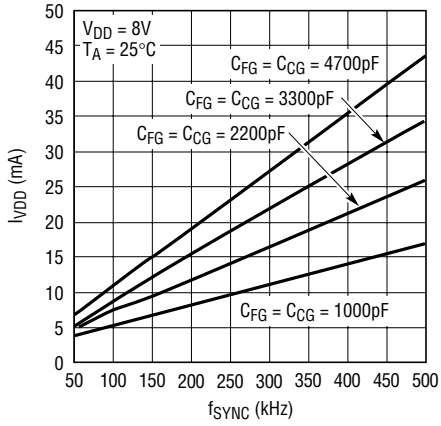


Opto Driver Short-Circuit Current vs Temperature



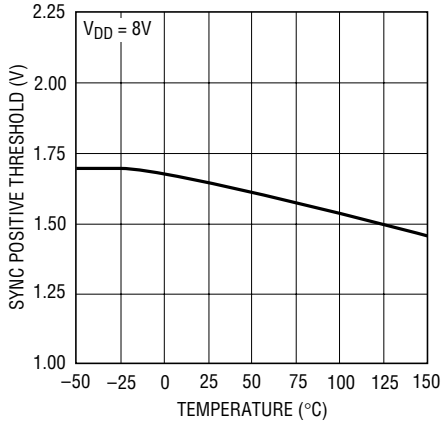
TYPICAL PERFORMANCE CHARACTERISTICS

I_{VDD} vs SYNC Frequency



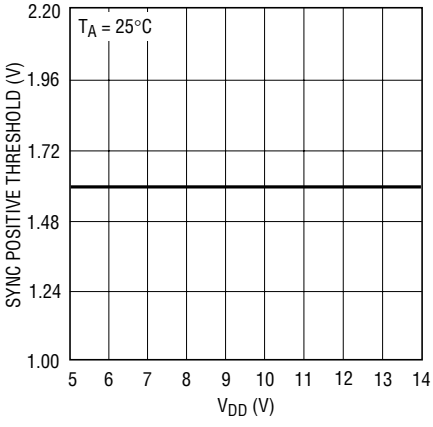
1698 G19

SYNC Positive Threshold vs Temperature



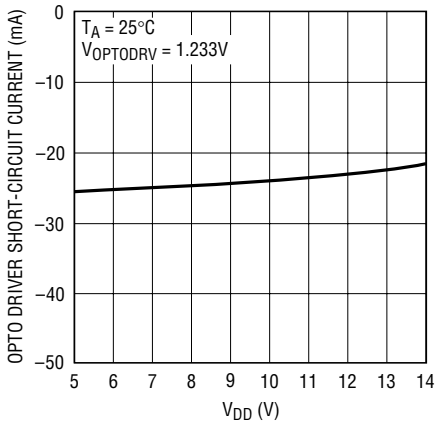
1698 G20

SYNC Positive Threshold vs V_{DD}



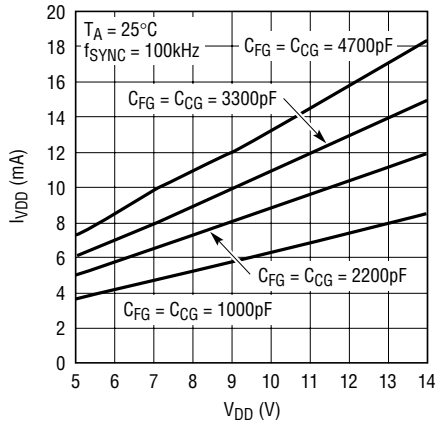
1698 G21

Opto Driver Short-Circuit Current vs V_{DD}



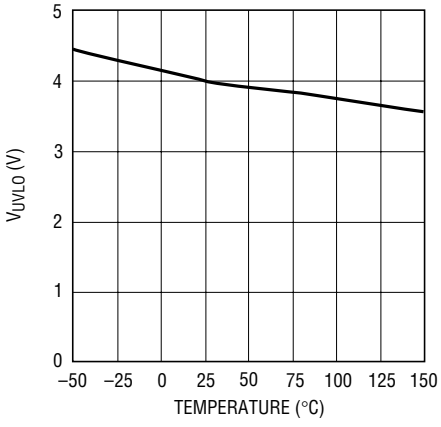
1698 G17

I_{VDD} vs V_{DD}



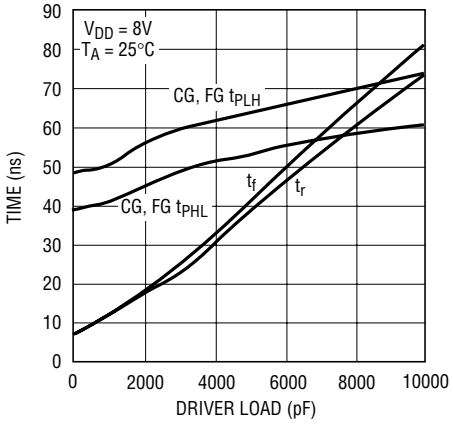
1698 G18

Undervoltage Lockout Threshold vs Temperature



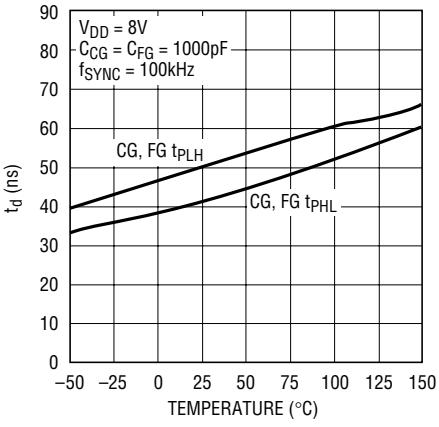
1698 G24

Driver Rise, Fall and Propagation Delay vs Driver Load



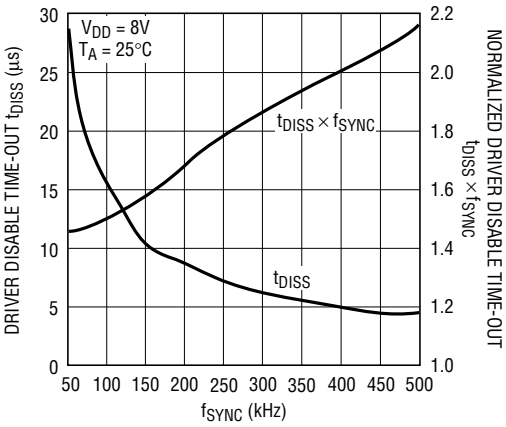
1698 G25

SYNC Input to Driver Output Delay vs Temperature



1698 G26

Driver Disable Time-Out vs SYNC Frequency



1698 G27

PIN FUNCTIONS

V_{DD} (Pin 1): Power Supply Input. For isolated applications, a simple rectifier from the power transformer is used to power the chip. This pin powers the opto driver, the V_{AUX} supply and the FG and CG drivers. An internal 5V regulator powers the remaining circuitry. V_{DD} requires an external 4.7µF bypass capacitor.

CG (Pin 2): Catch Gate Driver. If SYNC slews positive, CG pulls high to drive an external N-channel MOSFET. CG draws power from the V_{DD} pin and swings between V_{DD} and PGND.

PGND (Pin 3): Power Ground. Connect PGND to a low impedance ground plane in close proximity to the ground terminal of the external current sensing resistor.

GND (Pin 4): Logic and Signal Ground. GND is referenced to the internal low power circuitry. Careful board layout techniques must be used to prevent corruption of signal ground reference. Connect GND and PGND together directly at the LTC1698.

OPTODRV (Pin 5): Optocoupler Driver Output. This pin drives a ground referenced optocoupler through an external resistor. If V_{FB} is low, OPTODRV pulls low. If V_{FB} is high, OPTODRV pulls high. This optocoupler driver has a DC gain of 5. During overvoltage or overcurrent conditions, OPTODRV pulls high. The output is capable of sourcing 10mA of current and will drive an external 0.1µF capacitive load and is short-circuit protected.

V_{COMP} (Pin 6): Error Amplifier Output. This error amplifier is able to drive more than 2kΩ and 100pF of load. The internal diode connected from V_{FB} to V_{COMP} reduces OPTODRV recovery time under start-up conditions.

MARGIN (Pin 7): Current Input to Adjust the Output Voltage Linearly. The MARGIN pin connects to an internal 16.5k resistor. The other end of this resistor is regulated to 1.65V. Connecting MARGIN to a 3.3V logic supply sources 100µA of current into the chip and moves the output voltage 5% higher. Connecting MARGIN to 0V sinks 100µA out of the pin and moves the regulated output voltage 5% lower. The MARGIN pin voltage does not affect the PWRGD and OVPIN trip points.

V_{FB} (Pin 8): Feedback Voltage. V_{FB} senses the regulated output voltage through an external resistor divider. The V_{FB} pin is servoed to the reference voltage of 1.233V under closed-loop conditions. An RC network from V_{FB} to V_{COMP} compensates the feedback loop. If V_{FB} goes low, V_{COMP} pulls high and OPTODRV goes low.

OVPIN (Pin 9): Overvoltage Input. OVPIN is a high impedance input to an internal comparator. The threshold of this comparator is set to 1.233V. If the OVPIN potential is higher than the threshold voltage, OPTODRV pulls high immediately. Use an external RC lowpass filter to prevent noisy signals from triggering this comparator.

PWRGD (Pin 10): Power Good Output. This is an open-drain output. PWRGD floats if V_{FB} is above 94% of the nominal value for more than 2ms. PWRGD pulls low if V_{FB} is below 94% of the nominal value for more than 1ms. The PWRGD threshold is independent of the MARGIN pin potential.

I_{SNSGND} (Pin 11): Current Sense Ground. Connect to the positive side of the sense resistor, normally grounded.

I_{SNS} (Pin 12): Current Sense Input. Connect to the negative side of the sense resistor through an external RC lowpass filter. This pin normally sees a negative voltage, which is proportional to the average load current. If current limit is exceeded, OPTODRV pulls high.

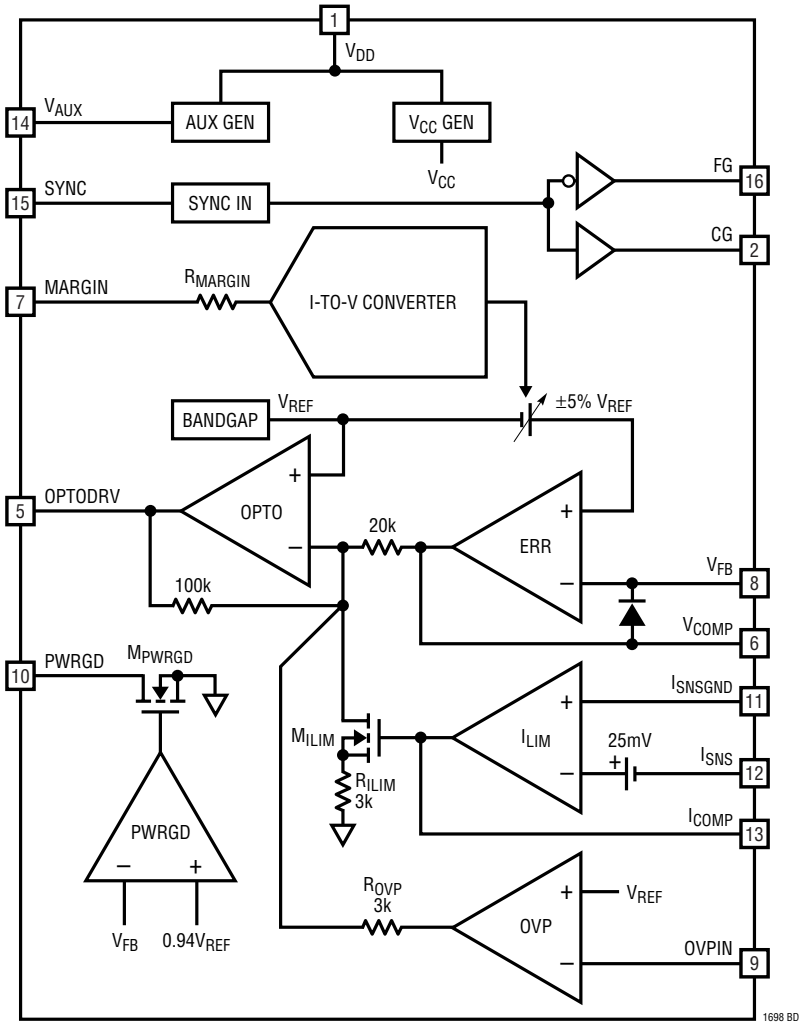
I_{COMP} (Pin 13): Current Amplifier Output. An RC network at this pin compensates the current limit feedback loop. Referencing the RC to V_{OUT} controls output voltage overshoot on start-up. This pin can float if current limit loop compensation is not required.

V_{AUX} (Pin 14): Auxiliary 3.3V Logic Supply. This pin requires a 0.1µF or greater bypass capacitor. This auxiliary power supply can power external devices and sources 10mA of current. Internal current limiting is provided.

SYNC (Pin 15): Drivers Synchronization Input. A negative voltage slew at SYNC forces FG to pull high and CG to pull low. A positive voltage slew at SYNC resets the FG pin and CG pulls high. If SYNC loses its synchronization signal for more than the driver disable time-out interval, both the forward and catch drivers output are forced low. The SYNC circuit accepts pulse and square wave signals. The minimum pulse width is 75ns. The synchronization frequency range is between 50kHz to 400kHz.

FG (Pin 16): Forward Gate Driver. If SYNC slews negative, FG goes high. FG draws power from V_{DD} and swings between V_{DD} and PGND.

BLOCK DIAGRAM



OPERATION (Refer to Block Diagram)

The LTC1698 is a secondary-side synchronous rectifier controller designed to work with the LT3781 primary-side synchronous controller chip to form an isolated synchronous forward converter. This chip set uses a dual transistor forward topology that is predominantly used in distributed power supply systems where isolated low voltages are needed to power complex electronic equipment. The primary stage is a current mode, fixed frequency forward converter and provides the typical PWM operation. A power transformer is used to provide the functions of input/output isolation and voltage step-down to achieve the required low output voltage. Instead of using typical Schottky diodes, synchronous rectification on the secondary offers isolation with high efficiency. It supplies high power without the need of bulky heat sinks, which is often a problem in any space constrained application.

The LTC1698 not only provides synchronous drivers for the external MOSFETs, it comes with other housekeeping functions performed on the secondary side of the power supply, all within a single integrated controller. Figure 1 shows the typical chip-set application. Upon power up, the LTC1698's V_{DD} input is low, the gate drivers TG and BG are both at the ground potential. The secondary forward and

OPERATION (Refer to Block Diagram)

catch MOSFETs Q3 and Q4 are off. As soon as transistors Q1 and Q2 turn on, the flux in the power transformer T1 forces the body diodes of Q3 and Q4 to conduct, and the whole circuit starts like a conventional forward converter. At the same time, the LTC1698 V_{DD} potential ramps up quickly through the V_{DD} bias circuitry. Once the V_{DD} voltage exceeds 4.0V, the LTC1698 enables its drivers and enters synchronous operation.

The pulse transformer T2 synchronizes the primary and secondary MOSFET drivers. In a typical conversion cycle, the primary MOSFETs Q1 and Q2 turn on simultaneously. SG goes low and generates a negative spike at the LTC1698 SYNC input through the pulse transformer. The LTC1698 forces FG to turn on and CG to turn off. Power is delivered to the load through the transformer T1 and the inductor L1. At the beginning of the next phase in which Q1 and Q2 turn off, SG goes high, SYNC sees a positive spike, the MOSFET Q3 shuts off, Q4 conducts and allows continuous current to flow through the inductor L1. The capacitor C_{OUT} filters the switching waveform to provide a steady DC output voltage for the load.

The LTC1698 error amplifier ERR senses the output voltage through an external resistor divider and regulates the V_{FB} pin potential to the 1.233V internal bandgap voltage. An external RC network across the V_{FB} and V_{COMP} pins frequency compensates the error amplifier feedback. The opto driver amplifies the voltage difference between the V_{COMP} pin and the bandgap potential, driving the external optocoupler diode with an inverting gain of 5. The optocoupler feeds the amplified output error signal to the primary controller and closes the forward converter voltage feedback loop. Under start-up conditions, the internal diode across the LTC1698 error amplifier clamps the V_{COMP} pin. This speeds up the opto driver recovery time by reducing the negative slew rate excursion at the COMP pin.

The forward converter output voltage can be easily adjusted. The potential at the MARGIN pin is capable of forcing the error amplifier reference voltage to move linearly by ±5%. The internal R_{MARGIN} resistor converts the MARGIN voltage to a current and linearly controls the offset of the error amplifier. Connecting the MARGIN pin to 3.3V increases the V_{FB} voltage by 5%, and connecting the MARGIN pin to 0V reduces V_{FB} by 5%. With the MARGIN pin floating, the VFB voltage is regulated to the internal bandgap voltage.

The current limit transconductance amplifier I_{LIM} provides the secondary side average current limit function. The average voltage drops across the R_{SECSEN} resistor is sensed and compared to the –25mV threshold set by the internal I_{LIM} amplifier. Once I_{LIM} detects high output current, the current amplifier output pulls high, overrides the error amplifier, injects more current into the photo diode and forces a lower duty cycle. An RC network connected to the I_{COMP} pin is used to stabilize the secondary current limit loop. Alternatively, if only overcurrent fault protection is required, I_{COMP} can float.

If under abnormal conditions the feedback path is broken, OVPIN provides another route for overvoltage fault protection. If the voltage at OVPIN is higher than the bandgap voltage, the OVP comparator forces OPTODRV high immediately. A simple external RC filter prevents a momentary overshoot at OVPIN from triggering the OVP comparator. Short OVPIN to ground if this pin is not used.

The LTC1698 provides an open-drain PWRGD output. If V_{FB} is less than 94% of its nominal value for more than 1ms, the PWRGD comparator pulls the PWRGD pin low. If V_{FB} is higher than 94% of its nominal value for more than 2ms, the transistor M_{PWRGD} shuts off, and an external resistor pulls the PWRGD pin high.

The LTC1698 provides an auxiliary 3.3V logic power supply. This auxiliary power supply is externally compensated with a minimum 0.1µF bypass capacitor. It supplies up to 10mA of current to any external devices.

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Undervoltage Lockout

In UVLO (low V_{DD} voltage) the drivers FG and CG are shut off and the pins OPTODRV, V_{AUX}, PWRGD and I_{COMP} are forced low. The LTC1698 allows the bandgap and the internal bias currents to reach their steady-state values before releasing UVLO. Typically, this happens when V_{DD} reaches approximately 4.0V. Beyond this threshold, the drivers start switching. The OPTODRV, V_{AUX}, PWRGD and I_{COMP} pins return to their normal values and the chip is fully functional. However, if the V_{DD} voltage is less than 7V, the OPTODRV and V_{AUX} current sourcing capabilities are limited. See the OPTO driver graphs in the Typical Performance Characteristics section.

V_{DD} Regulator

The bias supply for the LTC1698 is generated by peak rectifying the isolated transformer secondary winding. As shown in Figure 2, the zener diode Z1 is connected from base of Q5 to ground such that the emitter of Q5 is regulated to one diode drop below the zener voltage. R_Z is selected to bring Z1 into conduction and also provide base current to Q5. A resistor (on the order of a few hundred ohms), in series with the base of Q5, may be required to surpress high frequency oscillations depending on Q5's selection. A power MOSFET can also be used by increasing the zener diode value to offset the drop of the gate-to-source voltage. V_{DD} supply current varies linearly with the supply voltage, driver load and clock frequency. A 4.7µF bypass capacitor for the V_{DD} supply is sufficient for most applications. This capacitor must be large enough to provide a stable DC voltage to meet the LTC1698 V_{DD} supply requirement. Under start-up conditions, it must be small enough to power up instantaneously, enabling the LTC1698 to regulate the feedback loop. Using a larger capacitor requires evaluation of the start-up performance.

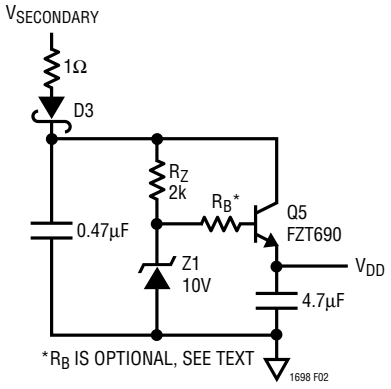

Figure 2. V_{DD} Regulator

SYNC Input

Figure 3 shows the synchronous forward converter application. The primary controller LT3781 runs at a fixed frequency and controls MOSFETs Q1 and Q2. The secondary controller LTC1698 controls MOSFETs Q3 and Q4. An inexpensive, small-size pulse transformer T2 synchronizes the primary and the secondary controllers. Figure 4 shows the pulse transformer timing waveforms. When the LT3781 synchronization output SG goes low, MOSFET

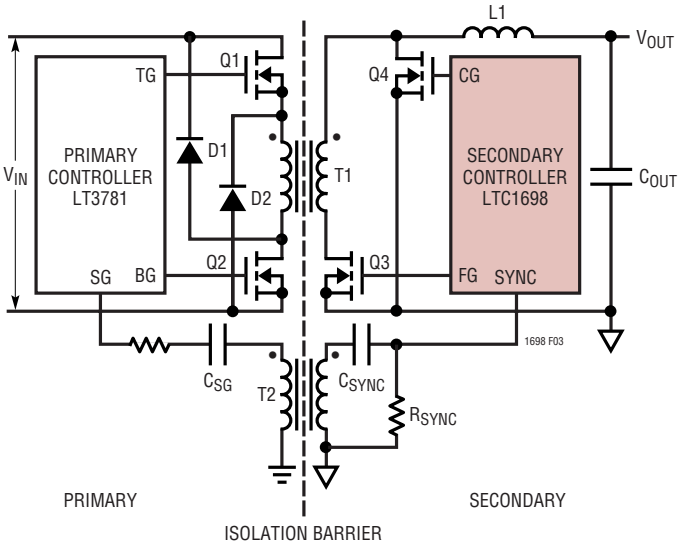

Figure 3. Synchronization Using Pulse Transformer

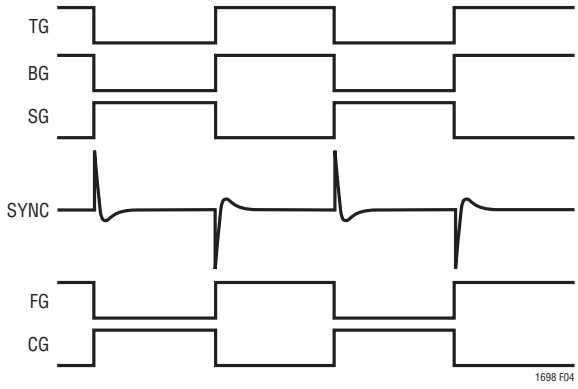

Figure 4. Primary Side and Secondary Side Synchronization Waveforms

APPLICATIONS INFORMATION

drivers TG and BG go high. The pulse transformer T2 generates a negative slew at the SYNC pin and forces the secondary MOSFET driver FG to go high and CG to go low. When TG and BG go low, SG goes high and the secondary controller forces CG high and FG low.

For a given pulse transformer, a bigger capacitor C_{SG} generates a higher and wider SYNC pulse. The peak of this pulse should be much higher than the SYNC threshold. Amplitudes greater than ±5V help to speed up the SYNC comparator and reduce the SYNC to FG and CG drivers propagation delay. The minimum pulse width is 75ns. Overshoot during the pulse transformer reset interval must be minimized and kept below the minimum comparator thresholds of ±1V. The amount of overshoot can be reduced by having a smaller reset resistor R_{SYNC}. For nonisolated applications, the SYNC input can be driven directly by a square pulse. To reduce the propagation delay, make the positive and negative magnitude of the square wave much greater than the ±2.2V maximum threshold.

In addition to the simple driver synchronization, the secondary controller requires a driver disable signal. Loss of synchronization while CG is high will cause Q4 to discharge the output capacitor. This produces a negative output voltage transient and possible damage to the load circuitry connected to V_{OUT}. To overcome this problem, the LTC1698 comes with a unique adaptive time-out circuit. It works well within the 50kHz to 400kHz frequency range. At every positive SYNC pulse, the internal timer resets. If the SYNC signal is missing, the internal timer loses its reset command, and eventually exceeds the internal time-out limit. This forces both the FG and CG drivers to go low immediately.

The time-out duration varies linearly with the LT3781 primary controller clocking frequency. Upon power up, the time-out circuitry takes a few clock cycles to adapt to the input clock frequency. During this time interval, the drivers pulse width might be prematurely terminated, and the inductor current flows through the MOSFETs body diode. Once the LTC1698 timer locks to the clocking frequency, the LTC1698 drivers follow the SYNC signal without fail. Figure 5 shows the SYNC time-out waveforms. The time-out circuit guarantees that if the SYNC pulse is missing for more than one period, both the drivers will be shut down preventing the output voltage from going below ground. The wide synchronization frequency range adds flexibility to the forward converter and allows this converter chip set to meet different application requirements.

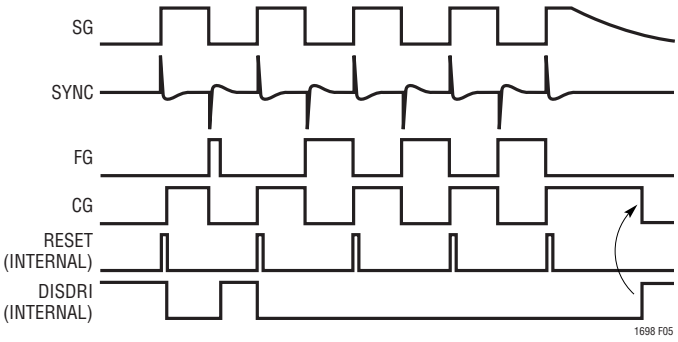

Figure 5. SYNC Time-Out Waveforms

Under normal operating conditions, the time-out circuitry adapts to the switching frequency within a few cycles. Once synchronized, internal circuitry ensures the maximum time that the Catch FET (Q4) could be left turned on is typically just over one switching period. This is particularly important with high output voltages that can generate significant negative output inductor currents if the Catch FET Q4 is left on. Poor feedback loop performance including output voltage overshoot can cause the primary controller to interrupt the synchronization pulse train. While this generally is not a problem, it is possible that low frequency interruptions could lead to a time-out period longer than a switching period, limited only by the internal timer clamp (50µs typical).

Output Voltage Programming

The switching regulator output voltage is programmed through a resistor feedback network (R1 and R2 in Figure 1) connected to V_{FB}. If the output is at its nominal value, the divider output is regulated to the error amplifier threshold of 1.233V.

The output voltage is thus set according to the relation:

$$V_{OUT} = 1.233 \bullet (1 + R2/R1)$$

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MARGIN Adjustment

The MARGIN input is used for adjusting the programmed output voltage linearly by varying the current flowing into and out of the pin. Forcing 100µA into the pin moves the output voltage 5% higher. Forcing 100µA out of the pin moves the output voltage 5% lower. With the MARGIN pin floating, the V_{FB} pin is regulated to the bandgap voltage of 1.233V. The MARGIN pin is a high impedance input. It is important to keep this pin away from any noise source like the inductor switching node. Any stray signal coupled to the MARGIN pin can affect the switching regulator output voltage.

This pin is internally connected to a 16.5k resistor that feeds the I-V converter. The I-V converter output linearly controls the error amplifier offset voltage. The input of the I-V converter is biased at 1.65V. This allows the ±100µA current to be obtained by connecting the MARGIN pin to the V_{AUX} 3.3V supply (+5%) or GND (–5%). For output voltage adjustment smaller than ±5%, an external resistor R_{EXT} as shown in Figure 6 is added in series with the internal resistor to lower the current flowing into or out of the MARGIN pin. The value of R_{EXT} is calculated as follow:

$$R_{EXT} = \left(\frac{5\%}{\text{REQUIRED }\%} - 1 \right) \bullet 16.5k$$

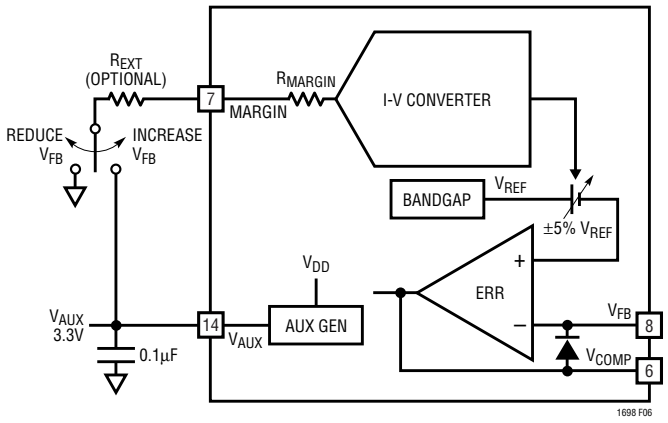

Figure 6. Output Voltage Adjustment

Overvoltage Function

The OVPIN is used for overvoltage protection and is designed to protect against an open V_{FB} loop. Opening the V_{FB} loop causes the error amplifier to drive the OPTODRV pin low, forcing the primary controller to increase the duty cycle. This causes the output voltage to increase to a dangerously high level. To eliminate this fault condition, the OVP comparator monitors the output voltage with a resistive divider at OVPIN. A voltage at OVPIN higher than the V_{REF} potential forces the OPTODRV pin high and reduces the duty cycle, thus preventing the output voltage from increasing further.

The OVPIN senses the output voltage through a resistor divider network (R4 and R5 in Figure 1). The divider is ratioed such that the voltage at OVPIN equals 1.233V when the output voltage rises to the overvoltage level. The overvoltage level is set following the relation:

$$V_{OVERVOLTAGE} = 1.233 \bullet (1 + R5/R4)$$

The OVP comparator is designed to respond quickly to an overvoltage condition. A small capacitor from OVPIN to ground keeps any noise spikes from coupling to the OVP pin. This simple RC filter prevents a momentary overshoot from triggering the OVP comparator.

The OVP comparator threshold is independent of the potential at the MARGIN pin. If the OVP function is not used, connect OVPIN to ground.

Power Good

The PWRGD pin is an open-drain output for power good indication. PWRGD floats if V_{FB} is above 94% of the nominal value for more than 2ms. An external pull-up resistor is required for PWRGD to swing high. PWRGD pulls low if V_{FB} drops below 94% of the nominal value for more than 1ms. The PWRGD threshold is referenced to the 1.233V bandgap voltage, which remains unchanged if the MARGIN pin is exercised.

Opto Feedback and Frequency Compensation

For a forward converter to obtain good load and line regulation, the output voltage must be sensed and compared to an accurate reference potential. Any error voltage must be amplified and fed back to the supply's control circuitry where the sensed error can be corrected. In an isolated supply, the control circuitry is frequently located on the primary. The output error signal in this type of

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supply must cross the isolation boundary. Coupling this signal requires an element that will withstand the isolation potentials and still transfer the loop error signal. Optocouplers are widely used for this function due to their ability to couple DC signals. To properly apply them, a number of factors must be considered. The gain, or current transfer ratio (CTR) through an optocoupler is loosely specified and is a strong function of the input current through the diode. It changes considerably as a function of time (aging) and temperature. The amount of aging accelerates with higher operating current. This variation directly affects the overall loop gain of the system. To be an effective optical detector, the output transistor of the optocoupler must have a large base area to collect the light energy. This gives it a large collector to base capacitance which can introduce a pole into the feedback loop. This pole varies considerably with the current and interacts with the overall loop frequency compensation network.

The common collector optocoupler configuration removes the miller effect due to the parasitic capacitance and increases the frequency response. Figure 7 shows the optocoupler feedback circuitry using the common collector approach. Note that the terms R_D, CTR, C_{DE} and r_π vary from part to part. They also change with bias current. The dominant pole of the opto feedback is due to R_F and C_F. The feedforward capacitor C_K at the optocoupler creates a low frequency zero. This zero should be chosen to provide a phase boost at the loop crossover frequency. The parallel combination of R_K and R_D form a high frequency pole with C_K. For most optocouplers, R_D is 50Ω at a DC bias of 1mA, and 25Ω at a DC bias of 2mA. The CTR term is the small signal AC current transfer ratio. For the QT Optoelectronics MOC207 optocoupler used here, the AC CTR is around 1, even though the DC CTR is much lower when biased at 1mA or 2mA. The first denominator term in the V_C/V_{OUT} equation has been simplified and assumes that $C_{FB} << C_C$. The actual term is:

$$s \bullet R2 \bullet (C_C + C_{FB}) \bullet \left(1 + s \bullet R_C \bullet \frac{C_C \bullet C_{FB}}{C_C + C_{FB}}\right)$$

$$\frac{V_C}{V_{OUT}} = -\frac{(1 + s \bullet C_C \bullet R_C)}{(s \bullet R2 \bullet C_C) \bullet (1 + s \bullet R_C \bullet C_{FB})} \bullet 5 \bullet \frac{(1 + s \bullet R_K \bullet C_K)}{\left(1 + s \bullet C_K \bullet \frac{R_K \bullet R_D}{R_K + R_D}\right)} \bullet \left(\frac{R_F \bullet CTR}{R_D + R_K}\right) \bullet \frac{1}{(1 + s \bullet r_\pi \bullet C_{DE})} \bullet \frac{1}{(1 + s \bullet R_F \bullet C_F)}$$

where:

R_D = Optocoupler diode equivalent small – signal resistance
CTR = Optocoupler current transfer ratio
C_{DE} = Optocoupler nonlinear capacitor across base to emitter
r_π = Optocoupler small – signal resistance across the base emitter

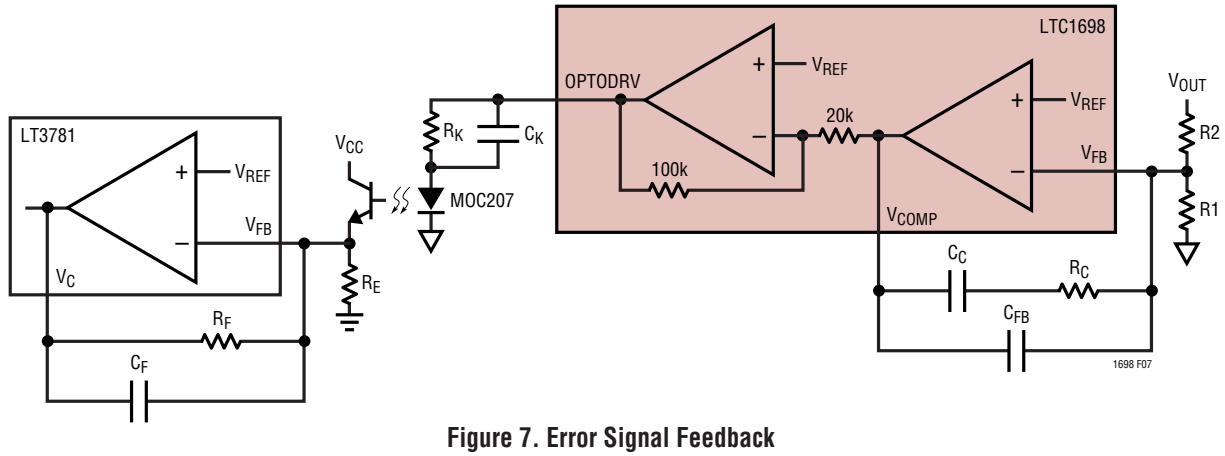

Figure 7. Error Signal Feedback

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A series RC network can be added in parallel with R2 (Figure 7) to provide a zero for the feedback loop frequency compensation.

The opto driver will drive a capacitive load up to 0.1µF. For optocouplers with a base pin, switching signal noise can get into this high impedance node. Connect a large resistor, 1M or 2M between the base and the emitter. This increases the diode current and the overall feedback bandwidth slightly, and decreases the optocoupler gain.

When designing the resistor in series with the optocoupler diode, it is important to consider the part to part variations in the current transfer ratio and its reduction over temperature and aging. The bigger the biasing current, the faster the aging. The LTC1698 opto driver is designed to source up to 10mA of current and swing between 0.4V to (V_{DD} – 2.5V). This should meet the design consideration of most optocouplers.

Besides the voltage feedback function, the LTC1698 opto driver couples fault signals to the primary controller and prevents catastrophic damage to the circuit. Upon current limit or an overvoltage fault, the I_{LIM} or OVP comparator overrides the error amplifier output and forces the OPTODRV pin high. This sources maximum current into the external optodiode and reduces the forward converter duty cycle.

Average Current Limit

The secondary current limit function is implemented by measuring the negative voltage across the current sense resistor R_{SECSEN}. The current limit transconductance amplifier I_{LIM} has a –25mV threshold. As shown in Figure 8, if the secondary current is small, the I_{COMP} pin goes low and the transistor M_{ILIM} shuts off. The potential at V_{COMP} determines the OPTODRV output. If the secondary current is large, I_{COMP} pulls high and forces the transistor M_{ILIM} to turn on hard. Thus the current limit circuit overrides the voltage feedback and forces OPTODRV high and injects maximum current into the external optocoupler. The R_{ILIM} resistor provides a linear relationship between the current sensed and the OPTODRV output.

The I_{SNS} and I_{SNSGND} pins allow a true Kelvin current sense measurement and offer true differential measurement across the sense resistor. A differential lowpass filter formed by R6 and C2 removes the pulse-to-pulse inductor current ripple and generates the average secondary current which is equal to the load current. The lowpass corner frequency is typically set to 1 to 2 orders of magnitude below the switching frequency and follows the relationship:

$$R_{SECSEN} = \frac{25mV}{I_{LMAX}}$$

$$R6 = \frac{1}{2 \bullet \pi \bullet C2 \bullet \frac{f_{SW}}{10}}$$

where:

R_{SECSEN} = Secondary current sense resistor

I_{LMAX} = Maximum allowed secondary current

f_{SW} = Forward converter switching frequency

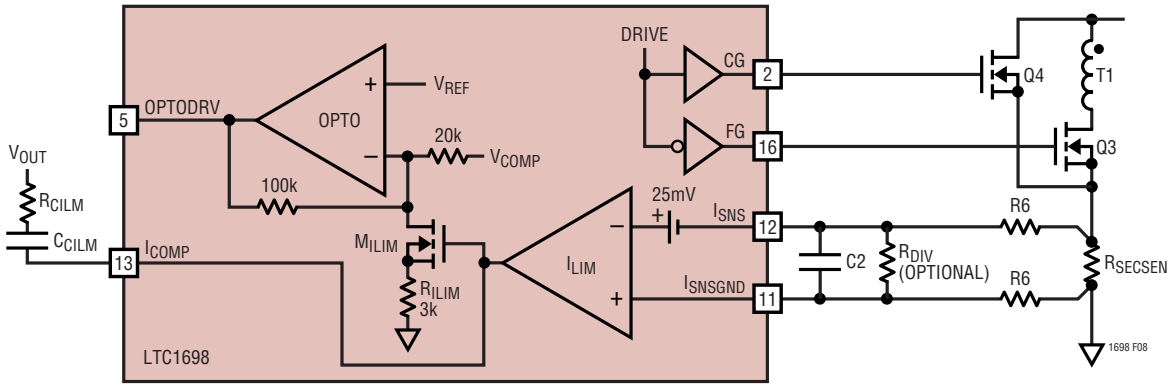

Figure 8. Secondary Average Current Limit

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If the application generates a bigger current sense voltage, a potential divider can be easily obtained by adding a resistor across C2. With this additional resistor, the voltage sensed by the current comparator becomes:

$$\frac{R_{DIV}}{R_{DIV} + (2 \bullet R6)} \bullet V_{RSENSE}$$

An RC network formed by R_{CILM} and C_{CILM} between I_{COMP} and V_{OUT} can be used to stabilize the current limit loop. Connecting the compensation network to V_{OUT} minimizes output overshoot during start-up or short-circuit recovery. The R_{CILM} and C_{CILM} zero should be chosen to be well within the closed-loop crossover frequency. This pin can be left floating if current loop compensation is not required. The forward converter secondary current limit function can be disabled by shorting I_{SNS} and I_{SNSGND} to ground.

Auxiliary 3.3V Logic Power Supply

An internal P-channel LDO (low dropout regulator) produces the 3.3V auxiliary supply that can power external devices or drive the MARGIN pin. This supply can source up to 10mA of current and the current limit is provided internally. The pin requires at least a 0.1µF bypass capacitor.

MOSFET Selection

Two logic-level N-channel power MOSFETs (Q3 and Q4 in Figure 1) are required for most LTC1698 circuits. They are selected based primarily on the on-resistance and body diode considerations. The required MOSFET $R_{DS(ON)}$ should be determined based on input and output voltage, allowable power dissipation and maximum required output current.

The average inductor (L1) current is equal to the output load current. This current is always flowing through either Q3 or Q4 with the power dissipation split up according to the duty cycle:

$$DC(Q3) = \frac{V_{OUT}}{V_{IN}} \bullet \frac{N_P}{N_S}$$

$$DC(Q4) = 1 - \left(\frac{V_{OUT}}{V_{IN}} \bullet \frac{N_P}{N_S} \right)$$

where N_P/N_S is the turns ratio of the transformer T1.

The $R_{DS(ON)}$ required for a given conduction loss can now be calculated by rearranging the relation $P = I^2R$.

$$P_{MAX(Q3)} = I_{MAX}^2 \bullet R_{DS(ON)Q3} \bullet DC(Q3)$$

$$\Rightarrow R_{DS(ON)Q3} = \frac{P_{MAX(Q3)}}{I_{MAX}^2 \bullet DC(Q3)}$$

$$P_{MAX(Q4)} = I_{MAX}^2 \bullet R_{DS(ON)Q4} \bullet DC(Q4)$$

$$\Rightarrow R_{DS(ON)Q4} = \frac{P_{MAX(Q4)}}{I_{MAX}^2 \bullet DC(Q4)}$$

where I_{MAX} is the maximum load current and P_{MAX} is the allowable conduction loss.

In a typical 2-transistor forward converter circuit, the duty cycle is less than 50% to prevent the transformer core from saturating. This results in the duty cycle of Q4 being greater than that of Q3. Q4 will dissipate more power due to the higher duty cycle. A lower $R_{DS(ON)}$ MOSFET can be used for Q4. This will slow down the turn-on time of Q4 since a lower $R_{DS(ON)}$ MOSFET will have a larger gate capacitance.

The next consideration for the MOSFET is the characteristic of the body diode. The body diodes conduct during the power-up phase, when the LTC1698 V_{DD} supply is ramping up and the time-out circuit is adapting to the SYNC input frequency. The CG and FG signals terminate prematurely and the inductor current flows through the body diodes. The body diodes must be able to take the comparable amount of current as the MOSFETs. Most power MOSFETs have the same current rating for the body diode and the MOSFET itself.

The LTC1698 CG and FG MOSFET drivers will dissipate power. This will increase with higher switching frequency, higher V_{DD} or larger MOSFETs. To calculate the driver dissipation, the total gate charge Qg is used. This parameter is found on the MOSFET manufacturers data sheet. The power dissipated in each LTC1698 MOSFET driver is:

$$P_{DRIVER} = Qg \bullet V_{DD} \bullet f_{SW}$$

where f_{SW} is the switching frequency of the converter.

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Power Transformer Selection

The forward transformer provides DC isolation and delivers energy from the primary to the secondary. Unlike the flyback topology, the transformer in the forward converter is not an energy storage device. As such, ungapped ferrite material is typically used. Select a power material rated with low loss at the switching frequency. Many core manufacturers have selection guides and application notes for transformer design. A brief overview of the more important design considerations is presented here.

For operating frequencies greater than 100kHz, the flux in the core is usually limited by core loss, not saturation. It is important to review both criteria when selecting the transformer. The AC operating flux density for core loss is given by:

$$B_{AC} = \frac{V_{IN} \bullet DC \bullet 10^8}{2 \bullet N_P \bullet A_e \bullet f_{SW}}$$

where:

B_{AC} is the AC operating flux density (gauss)

DC is the operating duty cycle

A_e is the effective cross sectional core area (cm^2)

f_{SW} is the switching frequency

To prevent core saturation during a transient condition, the peak flux density is:

$$B_{PK} = \frac{V_{IN(MAX)} \bullet DC\,(MAX) \bullet 10^8}{N_P \bullet A_e \bullet f_{SW}}$$

The minimum secondary turns count is:

$$N_{S(MIN)} = N_P \bullet \frac{V_{OUT} + V_D}{V_{IN(MIN)} \bullet DC\,(MAX)}$$

where:

V_{OUT} is the secondary output voltage

V_D is the voltage drop across the rectifier in the secondary

$V_{IN(MIN)}$ is the minimum input voltage

DC(MAX) is the maximum duty cycle

The core must be sized to provide sufficient window area for the amount of wire and insulation needed. The best performance is achieved by making each winding a single layer evenly distributed across the width of the bobbin. Multiple layers may be used to increase the copper area. Interleaving the primary and secondary windings will decrease the leakage inductance.

In a single-ended forward converter, much of the energy stored in the leakage inductance is dissipated in the primary-side MOSFET during turn-off. It is good design practice to sandwich the secondary winding between two primary windings.

For the 2-transistor forward converter shown in Figure 1, energy stored in the leakage inductance is returned to the input by diodes D1 and D2. With this topology, additional insulation for higher isolation can be used without significant penalty.

For a more detailed discussion on transformer core and winding losses, see Application Note AN19.

Inductor Selection

The output inductor in a typical LTC1698 circuit is chosen for inductance value and saturation current rating. The output inductor in a forward converter operates the same as in a buck regulator. The inductance sets the ripple current, which is commonly chosen to be 40% of the full load current. Ripple current is set by:

$$I_{RIPPLE} = \frac{V_{OUT} \bullet t_{OFF(MAX)}}{L}$$

where:

$$t_{OFF(MAX)} = \frac{\left(1 - DC\,(MIN)\right)}{f_{SW}}$$

and DC(MIN) is calculated based on the maximum input voltage.

$$DC\,(MIN) = \frac{N_P}{N_S} \bullet \frac{V_{OUT}}{V_{IN(MAX)}}$$

APPLICATIONS INFORMATION

Once the value of the inductor has been determined, an inductor with sufficient DC current rating is selected. Core saturation must be avoided under all operating conditions. Under start-up conditions, the converter sees a short circuit while charging the output capacitor. If the inductor saturates, the peak current will dramatically increase. The current will be limited only by the primary controller minimum on time and the circuit impedances.

High efficiency converters generally cannot afford the core loss found in low cost iron powder cores, forcing the use of more expensive ferrite, molypermalloy, or Kool Mμ® cores. As inductance increases, core loss goes down. Increased inductance requires more turns of wire so copper losses will increase. The optimum inductor will have equal core and copper loss.

Ferrite designs have very low core losses and are preferred at higher switching frequencies. Therefore, design goals concentrate on minimizing copper loss and preventing saturation. Kool Mμ is a very good, low-loss powder material with a "soft" saturation characteristic. Molypermalloy is more efficient at higher switching frequencies, but is also more expensive. Surface mount designs are available from many manufacturers using all of these materials.

Output Capacitor Selection

The output capacitor selection is primarily determined by the effective series resistance (ESR) to minimize voltage ripple. In a forward converter application, the inductor current is constantly flowing to the output capacitor, therefore, the ripple current at the output capacitor is small. The output ripple voltage is approximately given by:

$$V_{RIPPLE} \approx I_{RIPPLE} \bullet \left(ESR + \frac{1}{8 \bullet f_{SW} \bullet C_{OUT}} \right)$$

The output ripple is highest at maximum input voltage since I_{RIPPLE} increases with input voltage. Typically, once the ESR requirement for C_{OUT} has been satisfied the capacitance is adequate for filtering and has the required RMS current rating.

Fast load current transitions at the output will appear as a voltage across the ESR of the output capacitor until the feedback loop can change the inductor current to match the new load current value. As an example: at 3.3V out, a 10A load step with a 0.01Ω ESR output capacitor would experience a 100mV step at the output, a 3% output change. In surface mount applications, multiple capacitors may have to be placed in parallel to meet the ESR requirement.

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1698. These items are also illustrated graphically in Figure 9. Check the following for your layout:

1. Keep the power circuit and the signal circuit segregated. Place the power circuit, shown in bold, so that the two MOSFET drain connections are made directly at the transformer. The two MOSFET sources should be as close together as possible.
2. Connect PGND directly to the sense resistor with as short a path as possible. The MOSFET gate drive return currents flow through this connection.
3. Connect the 4.7μF ceramic capacitor directly between V_{DD} and PGND. This supplies the FG and CG drivers and must supply the gate drive current.
4. Bypass the V_{AUX} supply with a 0.1μF ceramic capacitor returned to GND.
5. Place all signal components in close proximity to their associated LTC1698 pins. Return all signal component grounds directly to the GND pin. One common connection can be made to V_{OUT}^+ from R2, R5 and C_{CILM}.
6. Make the connection between GND and PGND right at the LTC1698 pins.
7. Use a Kelvin-sense connection from the I_{SNS} and I_{SNSGND} pins to the secondary-side current-limit resistor R_{SECSEN}.

Kool Mμ is a registered trademark of Magnetics, Inc.

APPLICATIONS INFORMATION

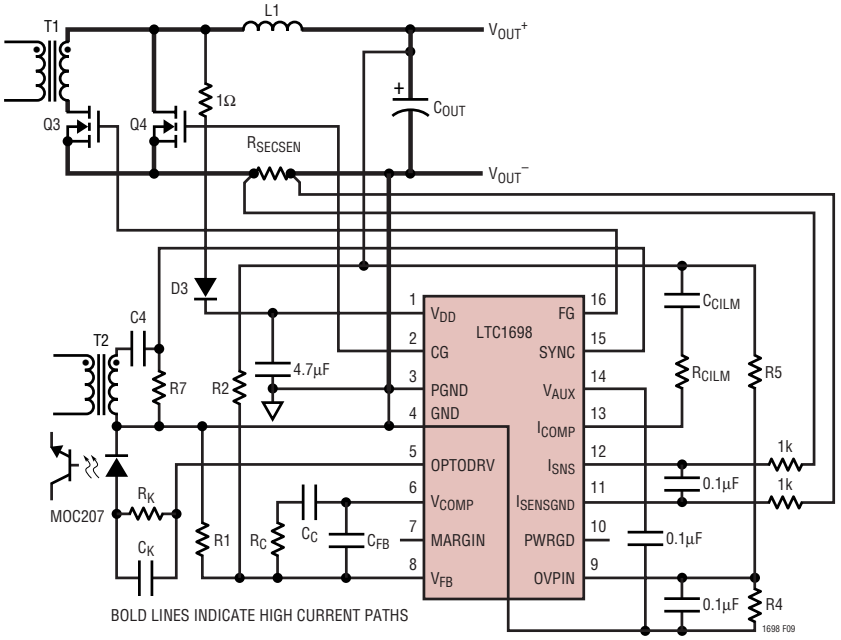


Figure 9. LTC1698 Layout Diagram

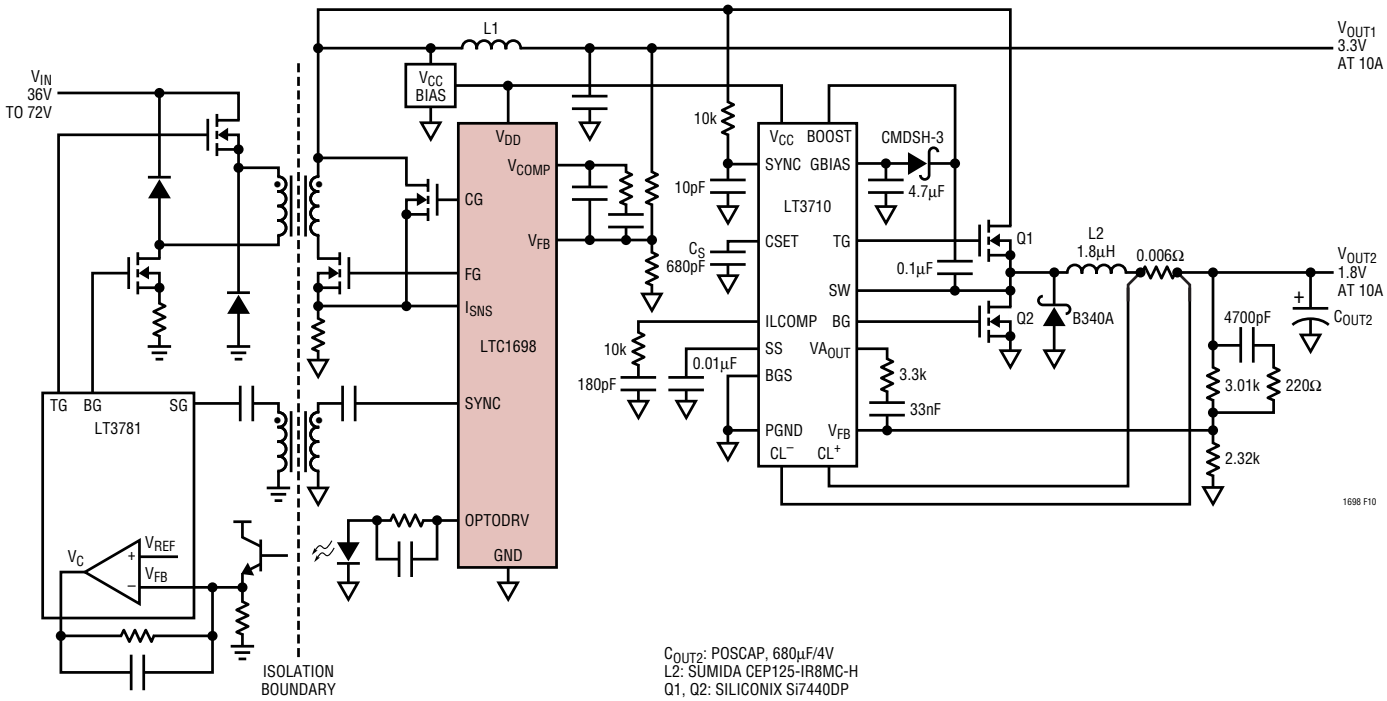


Figure 10. Simplified Single Secondary Winding 3.3V and 1.8V Output Isolated DC/DC Converter

TYPICAL APPLICATIONS

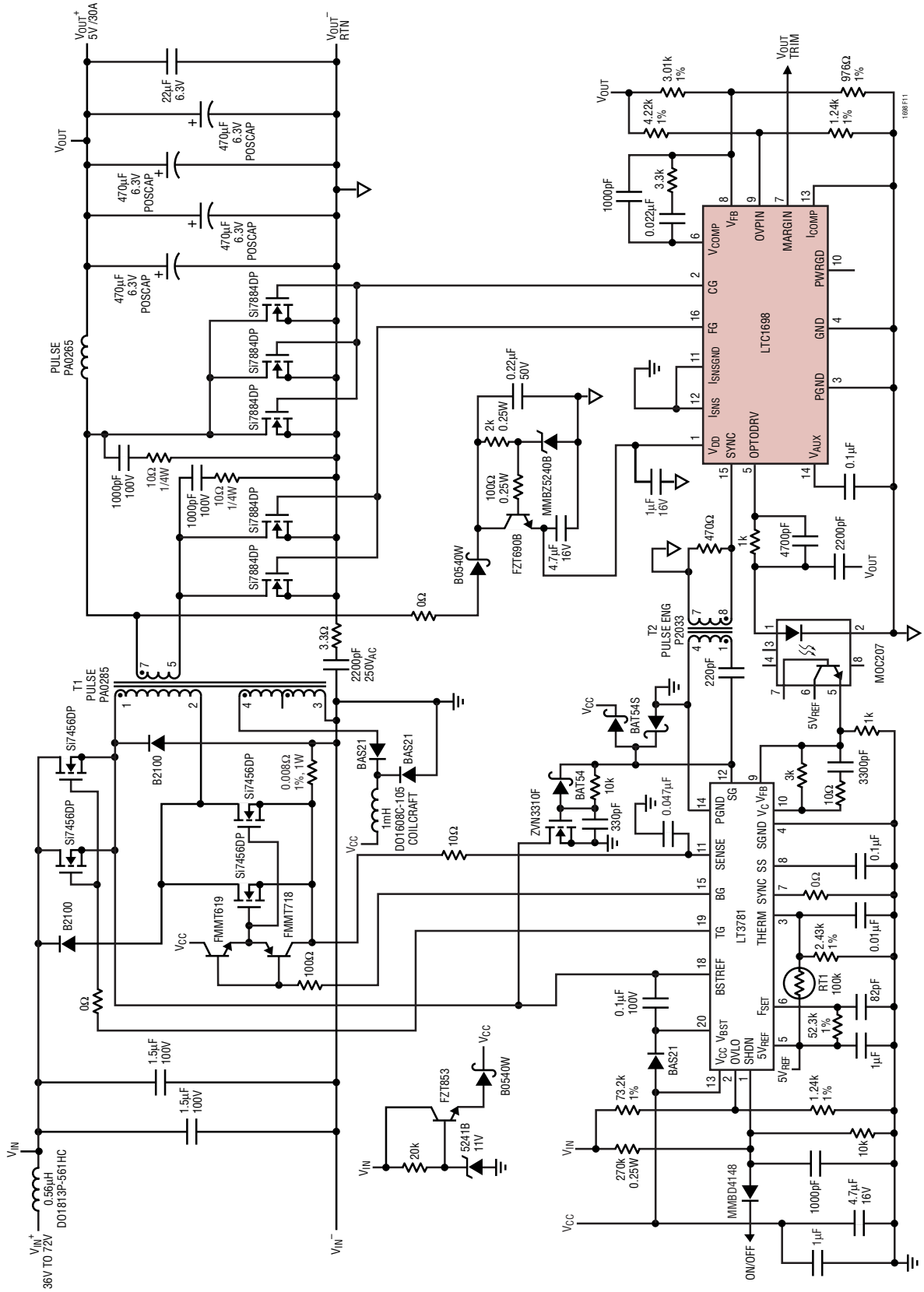


Figure 11. $36V_{IN}$-$72V_{IN}$ to 5V/30A Isolated Synchronous Forward Converter

TYPICAL APPLICATIONS

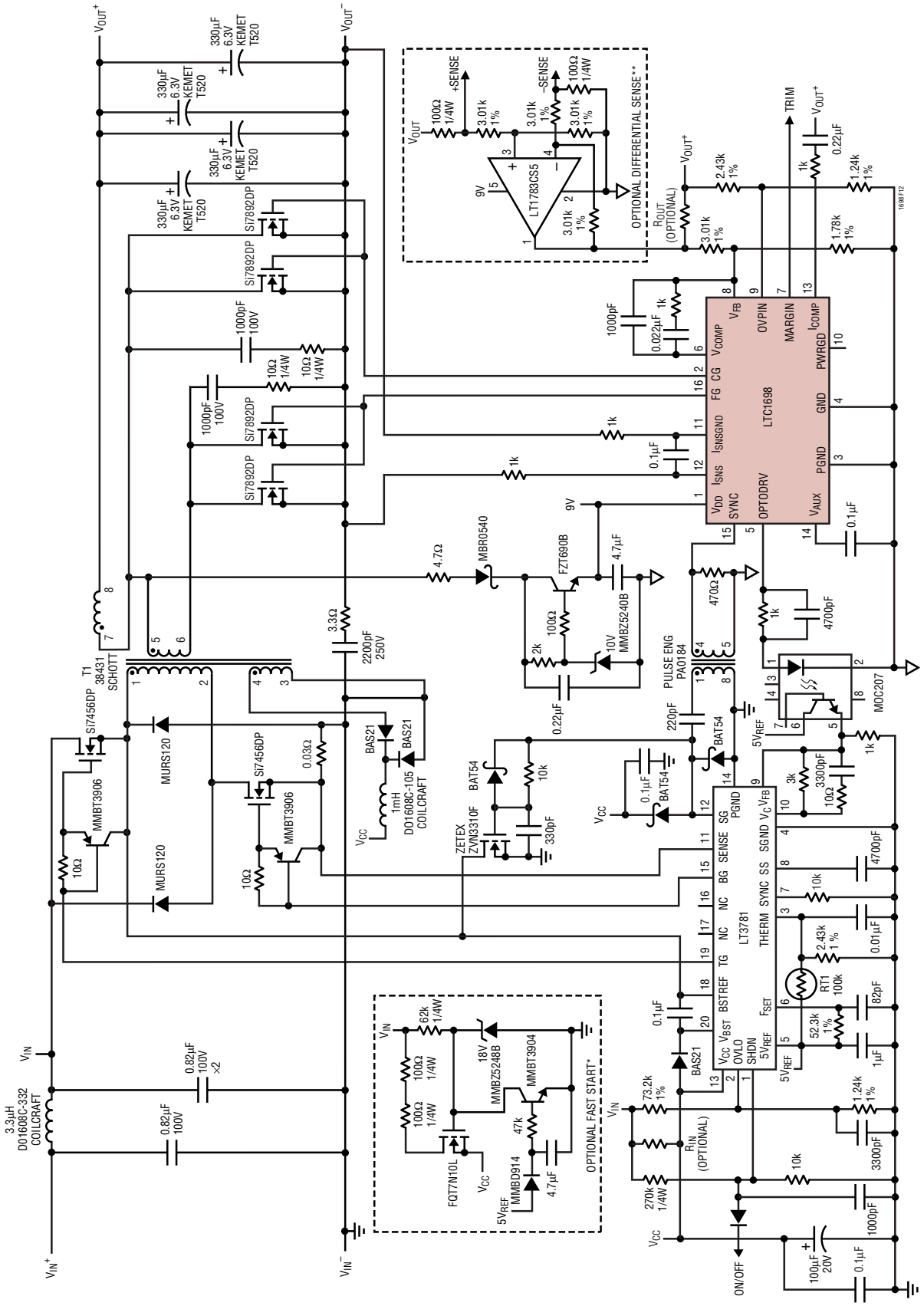


Figure 12. LT3781/LTC1698 36V$_{IN}$-72V$_{IN}$ to 3.3V/15A Isolated Synchronous Forward Converter-Quarter Brick

TYPICAL APPLICATIONS

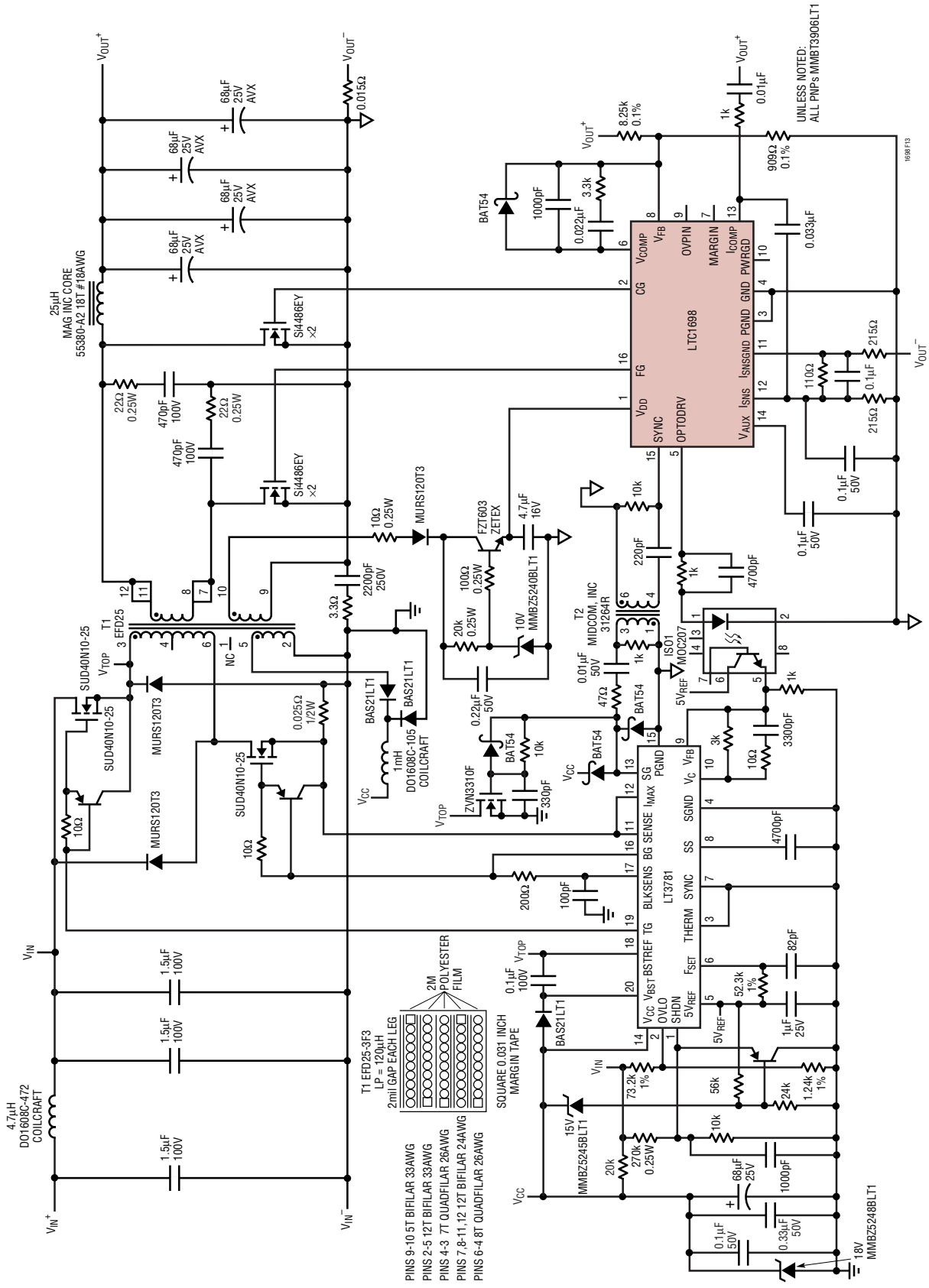
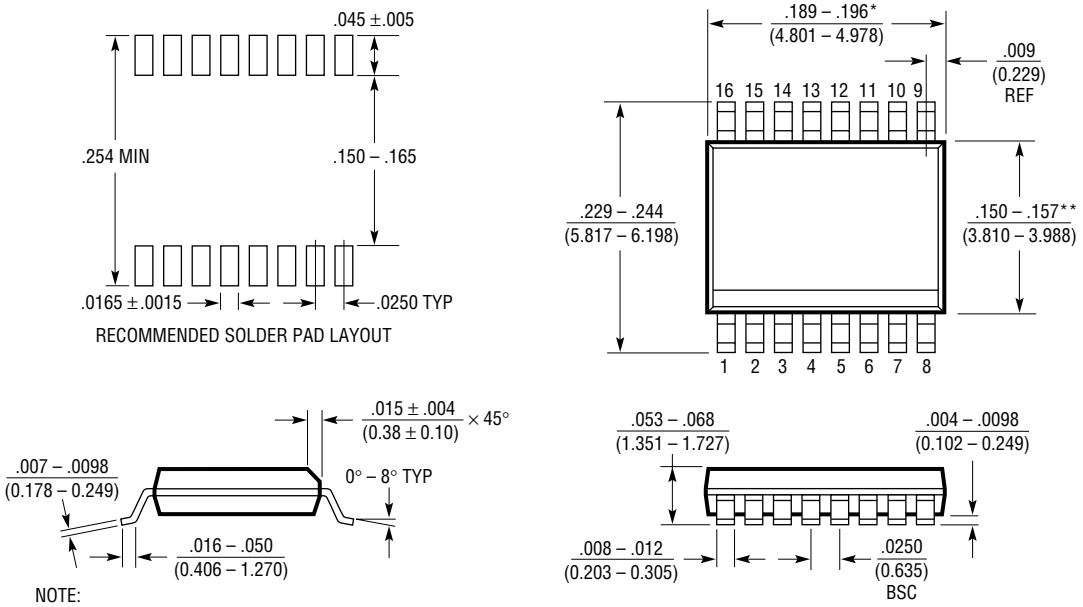


Figure 13. 36V$_{IN}$-72V$_{IN}$ to 12V/5A Isolated Synchronous Forward Converter

PACKAGE DESCRIPTION

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

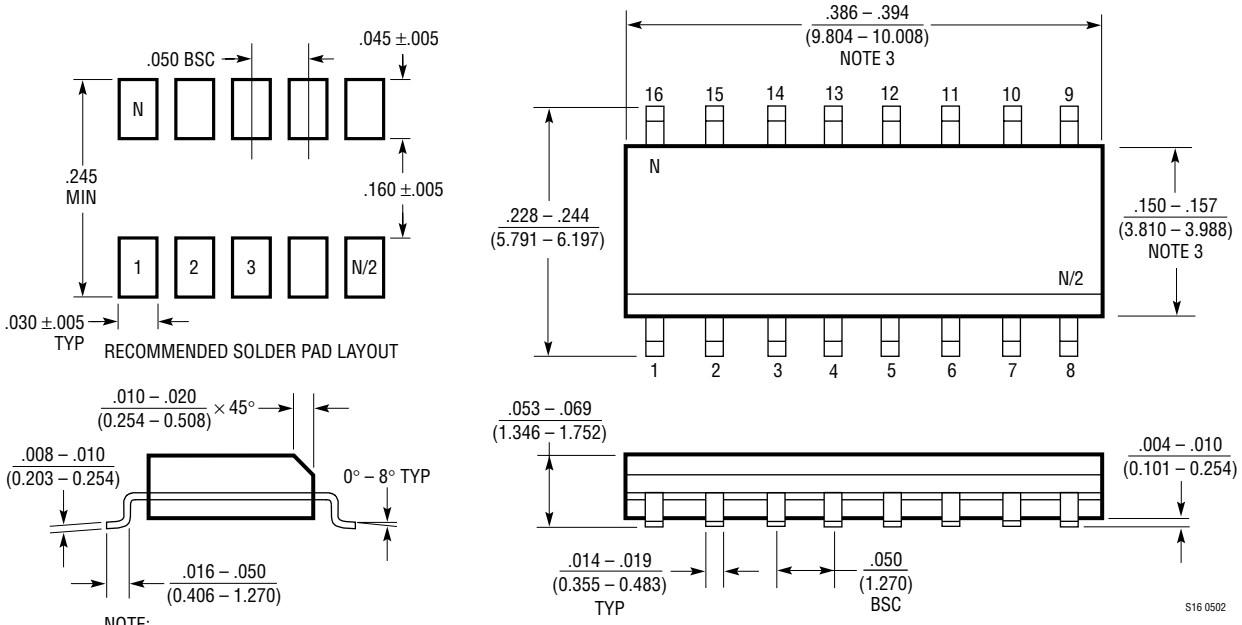
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN16 (SSOP) 0502

PACKAGE DESCRIPTION

S Package
16-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)

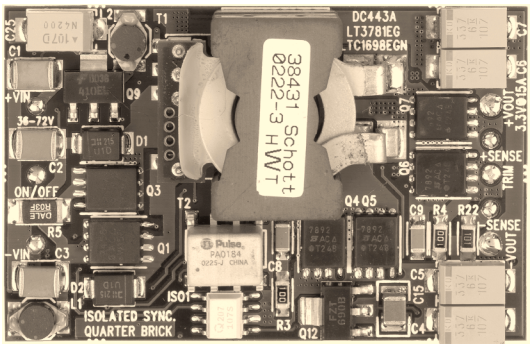


NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

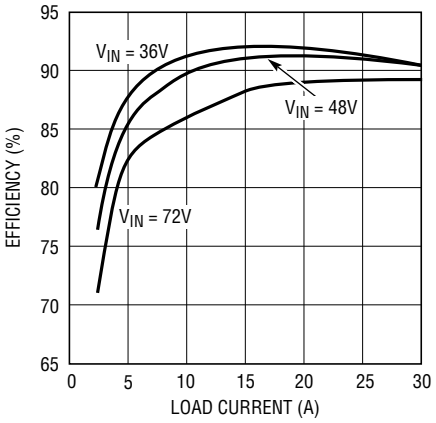
TYPICAL APPLICATIONS

LT3781/LTC1698 Isolated 3.3V/15A Converter



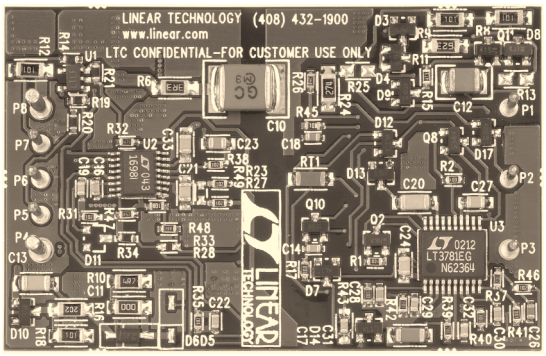
TOP

LT3781/LTC1698 Isolated 5V/30A Converter Efficiency vs Load Current



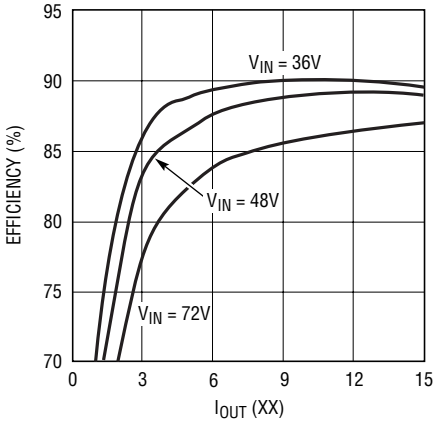
1698 TA01

LT3781/LTC1698 Isolated 3.3V/15A Converter



BOTTOM

LT3781/LTC1698 Isolated 3.3V/15A Converter Efficiency vs Load Current



1698 TA02

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1339	High Power Synchronous DC/DC Controller	Operation Up to 60V Maximum
LT1425	Isolated Flyback Switching Regulator	General Purpose with External Application Resistor
LT1431	Programmable Reference	0.4% Initial Voltage Tolerance
LT1680	High Power DC/DC Step-Up Controller	Operation Up to 60V Maximum
LT1681	Dual Transistor Synchronous Forward Controller	Operation Up to 72V Maximum
LT1725	General Purpose Isolated Flyback Controller	Drives External Power MOSFET with External I_{SENSE} Resistor
LT1737	High Power Isolated Flyback Controller	Sense Output Voltage Directly from Primary-Side Winding
LT3710	Secondary Side Synchronous Post Regulator	Generates a Regulated Auxiliary Output in Isolated DC/DC Converters, Dual N-Channel MOSFET Synchronous Drivers
LT3781	Dual Transistor Synchronous Forward Controller	Operation up to 72V Maximum

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