

## Dual and Quad, JFET Input Precision High Speed Op Amps

### FEATURES

- 14V/ $\mu$ s Slew Rate: 10V/ $\mu$ s Min
- 5MHz Gain-Bandwidth Product
- Fast Settling Time: 1.3 $\mu$ s to 0.02%
- 150 $\mu$ V Offset Voltage (LT1057): 450 $\mu$ V Max
- 180 $\mu$ V Offset Voltage (LT1058): 600 $\mu$ V Max
- 2 $\mu$ V/ $^{\circ}$ C  $V_{OS}$  Drift: 7 $\mu$ V/ $^{\circ}$ C Max
- 50pA Bias Current at 70 $^{\circ}$ C
- Low Voltage Noise:  
     13nV/ $\sqrt{\text{Hz}}$  at 1kHz  
     26nV/ $\sqrt{\text{Hz}}$  at 10Hz

### APPLICATIONS

- Precision, High Speed Instrumentation
- Fast, Precision Sample-and-Hold
- Logarithmic Amplifiers
- D/A Output Amplifiers
- Photodiode Amplifiers
- Voltage-to-Frequency Converters
- Frequency-to-Voltage Converters

### DESCRIPTION

The LT<sup>®</sup>1057 is a matched JFET input dual op amp in the industry standard 8-pin configuration, featuring a combination of outstanding high speed and precision specifications. It replaces all the popular bipolar and JFET input dual op amps. In particular, the LT1057 upgrades the performance of systems using the LF412A and OP-215 JFET input duals.

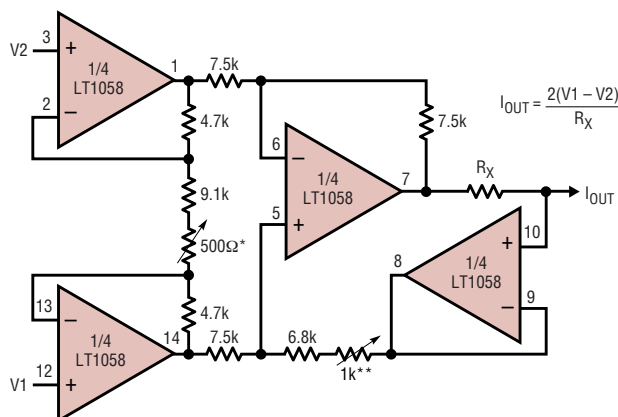
The LT1058 is the lowest offset quad JFET input operational amplifier in the standard 14-pin configuration. It offers significant accuracy improvement over presently available JFET input quad operational amplifiers. The LT1058 can replace four single precision JFET input op amps, while saving board space, power dissipation and cost.

Both the LT1057 and LT1058 are available in the plastic PDIP package and the surface mount SO package.

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### TYPICAL APPLICATION

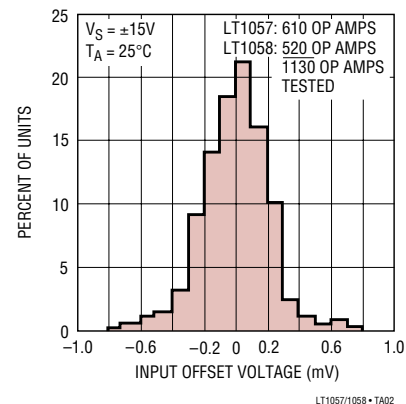
**Current Output, High Speed, High Input Impedance Instrumentation Amplifier**



\*GAIN ADJUST  
 \*\*COMMON MODE REJECTION ADJUST  
 BANDWIDTH  $\approx$  2MHz

LT1057/1058 • TA01

**Distribution of Offset Voltage (All Packages, LT1057 and LT1058)**



LT1057/1058 • TA02

# LT1057/LT1058

## ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage .....  $\pm 20\text{V}$   
 Differential Input Voltage .....  $\pm 40\text{V}$   
 Input Voltage .....  $\pm 20\text{V}$   
 Output Short-Circuit Duration ..... Indefinite  
 Storage Temperature Range .....  $-65^{\circ}\text{C}$  to  $150^{\circ}\text{C}$   
 Lead Temperature (Soldering, 10 sec) .....  $300^{\circ}\text{C}$

Operating Temperature Range

LT1057AM/LT1057M/  
 LT1058AM/LT1058M (**OBSOLETE**)...  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$   
 LT1057AC/LT1057C/LT1057S  
 LT1058AC/LT1058C/LT1058S .....  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$   
 LT1057I .....  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$

## PACKAGE/ORDER INFORMATION

<p>TOP VIEW</p> <p>SW PACKAGE 16-LEAD PLASTIC (WIDE) SO <math>T_{JMAX} = 150^{\circ}\text{C}</math>, <math>\theta_{JA} = 90^{\circ}\text{C/W}</math></p>	<p>TOP VIEW</p> <p>SW PACKAGE 16-LEAD PLASTIC (WIDE) SO <math>T_{JMAX} = 150^{\circ}\text{C}</math>, <math>\theta_{JA} = 90^{\circ}\text{C/W}</math></p>	<p>TOP VIEW</p> <p>S8 PACKAGE 8-LEAD PLASTIC SO <math>T_{JMAX} = 150^{\circ}\text{C}</math>, <math>\theta_{JA} = 200^{\circ}\text{C/W}</math></p> <p>Please note that the LT1057S8/LT1057IS8 standard surface mount pin-out differs from that of the LT1057 standard CERDIP/PDIP packages.</p>	<p>ORDER PART NUMBER</p> <p>LT1057S8 LT1057IS8</p> <p>S8 PART MARKING</p> <p>1057 1057I</p>
<p>ORDER PART NUMBER</p> <p>LT1057SW LT1057ISW</p>	<p>ORDER PART NUMBER</p> <p>LT1058SW LT1058ISW</p>	<p>TOP VIEW</p> <p>H PACKAGE 8-LEAD METAL CAN <b>OBSOLETE PACKAGE</b> Consider the N8 or S8 Package for Alternate Source</p>	<p>ORDER PART NUMBER</p> <p>LT1057AMH LT1057MH LT1057ACH LT1057CH</p>
<p>TOP VIEW</p> <p>N14 PACKAGE 14-LEAD PDIP <math>T_{JMAX} = 110^{\circ}\text{C}</math>, <math>\theta_{JA} = 130^{\circ}\text{C/W}</math></p> <p>J14 PACKAGE 14-LEAD CERDIP <math>T_{JMAX} = 150^{\circ}\text{C}</math>, <math>\theta_{JA} = 100^{\circ}\text{C/W}</math></p>	<p>ORDER PART NUMBER</p> <p>LT1058ACN LT1058CN</p> <p>LT1058AMJ LT1058MJ LT1058ACJ LT1058CJ</p> <p><b>OBSOLETE PACKAGES</b> Consider the N8, S8 or N14 Package for Alternate Source</p>	<p>ORDER PART NUMBER</p> <p>LT1057ACN8 LT1057CN8</p> <p>LT1057ACJ8 LT1057CJ8 LT1057AMJ8 LT1057MJ8</p>	<p>TOP VIEW</p> <p>N8 PACKAGE 8-LEAD PDIP <math>T_{JMAX} = 100^{\circ}\text{C}</math>, <math>\theta_{JA} = 130^{\circ}\text{C/W}</math></p> <p>J8 PACKAGE 8-LEAD CERDIP <math>T_{JMAX} = 150^{\circ}\text{C}</math>, <math>\theta_{JA} = 100^{\circ}\text{C/W}</math></p>

Consult LTC Marketing for parts specified with wider operating temperature ranges.

**ELECTRICAL CHARACTERISTICS**  $V_S = \pm 15V$ ,  $T_A = 25^\circ C$ ,  $V_{CM} = 0V$  unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS	LT1057AM/LT1058AM LT1057AC/LT1058AC			LT1057M/LT1058M LT1057C/LT1058C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{OS}$	Input Offset Voltage	LT1057 LT1057 (S8 Package) LT1058		150 180	450 600		200 220 250	800 1200 1000	$\mu V$ $\mu V$ $\mu V$
$I_{OS}$	Input Offset Current	Fully Warmed Up		3	40		4	50	pA
$I_B$	Input Bias Current	Fully Warmed Up		$\pm 5$	$\pm 50$		$\pm 7$	$\pm 75$	pA
	Input Resistance	Differential Common Mode $V_{CM} = -11V$ to $8V$ Common Mode $V_{CM} = 8V$ to $11V$		$10^{12}$ $10^{12}$ $10^{11}$			$10^{12}$ $10^{12}$ $10^{11}$		$\Omega$ $\Omega$ $\Omega$
	Input Capacitance			4			4		pF
$e_n$	Input Noise Voltage	0.1Hz to 10Hz, LT1057 LT1058			2.0 2.4			2.1 2.5	$\mu V_{P-P}$ $\mu V_{P-P}$
$e_n$	Input Noise Voltage Density	$f_0 = 10Hz$ $f_0 = 1kHz$ (Note 3)		26 13	22		28 14	24	$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
$i_n$	Input Noise Current Density	$f_0 = 10Hz, 1kHz$ (Note 4)		1.5	4		1.8	6	$fA/\sqrt{Hz}$
$A_{VOL}$	Large-Signal Voltage Gain	$V_O = \pm 10V$ , $R_L = 2k$ $V_O = \pm 10V$ , $R_L = 1k$	150 120	350 250		100 80	300 220		V/mV V/mV
	Input Voltage Range		$\pm 10.5$	14.3 $-11.5$		$\pm 10.5$	14.3 $-11.5$		V V
CMRR	Common Mode Rejection Ratio	LT1057 LT1058		86 84	100 98		82 80	98 96	dB dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 18V$	88	103		86	102		dB
$V_{OUT}$	Output Voltage Swing	$R_L = 2k$	$\pm 12$	$\pm 13$		$\pm 12$	$\pm 13$		V
SR	Slew Rate		10	14		8	13		V/ $\mu s$
GBW	Gain-Bandwidth Product	$f = 1MHz$ (Note 6)	3.5	5		3	5		MHz
$I_S$	Supply Current Per Amplifier			1.6	2.5		1.7	2.8	mA
	Channel Separation	DC to 5kHz, $V_{IN} = \pm 10V$		132			130		dB

(LT1057/LT1058 SW Package Only),  $V_S = \pm 15V$ ,  $T_A = 25^\circ C$ ,  $V_{CM} = 0V$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{OS}$	Input Offset Voltage	LT1057 LT1058		0.3 0.35	2 2.5	mV
$I_{OS}$	Input Offset Current	Fully Warmed Up		5	50	pA
$I_B$	Input Bias Current	Fully Warmed Up		$\pm 10$	$\pm 100$	pA
	Input Resistance –Differential –Common-Mode	$V_{CM} = -11V$ to $8V$ $V_{CM} = 8V$ to $11V$		0.4 0.4 0.05		$T\Omega$
	Input Capacitance			4		pF
$e_n$	Input Noise Voltage	0.1Hz to 10Hz LT1057 LT1058		2.1 2.5		$\mu V_{P-P}$
$e_n$	Input Noise Voltage Density	$f_0 = 10Hz$ $f_0 = 1kHz$		26 13		$nV/\sqrt{Hz}$

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# LT1057/LT1058

## ELECTRICAL CHARACTERISTICS

(LT1057/LT1058 SW Package Only),  $V_S = \pm 15V$ ,  $T_A = 25^\circ C$ ,  $V_{CM} = 0V$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$i_n$	Input Noise Current Density	$f_0 = 10Hz, 1kHz$		1.8		fA/ $\sqrt{Hz}$
$A_{VOL}$	Large-Signal Voltage Gain	$V_0 = \pm 10V$ $R_L = 2k$ $R_L = 1k$	100 50	300 220		V/mV
	Input Voltage Range		$\pm 10.5$	14.3 – 11.5		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 15V$ LT1057 LT1058	82 80	98 98		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 18V$	86	102		dB
$V_{OUT}$	Output Voltage Swing	$R_L = 2k$	$\pm 12$	$\pm 13$		V
SR	Slew Rate		8	13		V/ $\mu s$
GBW	Gain-Bandwidth Product	$f = 1MHz$ (Note 6)	3	5		MHz
$I_S$	Supply Current Per Amplifier			1.7	2.8	mA
	Channel Separation	DC to 5kHz, $V_{IN} = \pm 10V$		130		dB

The ● denotes the specifications which apply over the temperature range of  $0^\circ C \leq T_A \leq 70^\circ C$  or  $-40^\circ C \leq T_A \leq 85^\circ C$  (LT1057IS8), otherwise specifications are  $T_A = 25^\circ C$ .  $V_S = \pm 15V$ ,  $V_{CM} = 0V$ , unless noted.

SYMBOL	PARAMETER	CONDITIONS		LT1057AC LT1058AC			LT1057C LT1058C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
$V_{OS}$	Input Offset Voltage	LT1057	●		250	800		330	1400	$\mu V$
		LT1057IS8	●					500	2300	$\mu V$
		LT1057S8	●					400	1900	$\mu V$
		LT1058	●		300	1200		400	1800	$\mu V$
	Average Temperature Coefficient of Input (Offset Voltage)	LT1057 H/J8 Package	●		1.8	7		2.3	12	$\mu V/^\circ C$
		N8 Package	●		3	10		4	16	$\mu V/^\circ C$
		LT1057S8 (Note 5)	●					4	16	$\mu V/^\circ C$
		LT1057IS8 (Note 5)	●					4.5	16	$\mu V/^\circ C$
		LT1058 J Package (Note 5)	●		2.5	10		3	15	$\mu V/^\circ C$
		N Package (Note 5)	●		4	15		5	22	$\mu V/^\circ C$
$I_{OS}$	Input Offset Current	Warmed Up, $T_A = 70^\circ C$ LT1057IS8	●		18	150		20 35	250 600	pA
$I_B$	Input Bias Current	Warmed Up, $T_A = 70^\circ C$ LT1057IS8	●		$\pm 50$	$\pm 250$		$\pm 60$ $\pm 100$	$\pm 350$ $\pm 900$	pA
$A_{VOL}$	Large-Signal Voltage Gain	$V_0 = \pm 10V$ , $R_L = 2k$	●	70	220		50	200		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10.4V$	●	85	98		80	96		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 18V$	●	87	102		84	100		dB
$V_{OUT}$	Output Voltage Swing	$R_L = 2k$	●	$\pm 12$	$\pm 12.8$		$\pm 12$	$\pm 12.8$		V
$I_S$	Supply Current Per Amplifier		●			2.8			3.2	mA
		$T_A = 70^\circ C$			1.4			1.5		mA

# ELECTRICAL CHARACTERISTICS (LT1057/LT1058 SW Package Only.) The ● denotes specifications which apply over the temperature range of $V_S = \pm 15V$ , $V_{CM} = 0V$ , $0^\circ C \leq T_A \leq 70^\circ C$ (LT1057SW, LT1058SW) or $-40^\circ C \leq T_A \leq 85^\circ C$ (LT1057ISW, LT1058ISW), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{OS}$	Input Offset Voltage	LT1057 LT1058S LT1058IS	● ● ●	0.5 0.6 0.7	2.5 3.0 4.0	mV
	Average Temperature Coefficient of Input Offset Voltage		●	5		$\mu V/^\circ C$
$I_{OS}$	Input Offset Current	Warmed Up, $T_A = 70^\circ C$ Warmed Up, $T_A = 85^\circ C$		20 35	250 400	pA
$I_B$	Input Bias Current	Warmed Up, $T_A = 70^\circ C$ Warmed Up, $T_A = 85^\circ C$		$\pm 60$ $\pm 100$	$\pm 400$ $\pm 700$	pA
$A_{VOL}$	Large Signal Voltage Gain	$V_O = \pm 10V$ , $R_L = 2k$ LT1057 LT1058	● ●	50 40	200 200	mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.5V$ LT1057 LT1058	● ●	80 78	96 96	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 18V$ LT1057 LT1058	● ●	84 82	100 100	dB
$V_{OUT}$	Output Voltage Swing	$R_L = 2k$	●	$\pm 12$	$\pm 12.8$	V

The ● denotes specifications which apply over the temperature range of  $-55^\circ C \leq T_A \leq 125^\circ C$ ,  $V_S = \pm 15V$ ,  $V_{CM} = 0V$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1057AM LT1058AM			LT1057M LT1058M			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
$V_{OS}$	Input Offset Voltage	LT1057 LT1058	● ●		300 380	1100 1600		400 550	2000 2500	$\mu V$ $\mu V$
	Average Temperature Coefficient of Input Offset Voltage	LT1057 LT1058 (Note 5)	● ●		2.0 2.5	7 10		2.5 3	12 15	$\mu V/^\circ C$ $\mu V/^\circ C$
$I_{OS}$	Input Offset Current	Warmed Up, $T_A = 125^\circ C$			0.15	2		0.2	3	nA
$I_B$	Input Bias Current	Warmed Up, $T_A = 125^\circ C$			$\pm 0.6$	$\pm 4.5$		$\pm 0.7$	$\pm 6$	nA
$A_{VOL}$	Large-Signal Voltage Gain	$V_O = \pm 10V$ , $R_L = 2k$	●	40	120		30	110		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10.4V$	●	84	97		80	95		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 17V$	●	86	100		83	98		dB
$V_{OUT}$	Output Voltage Swing	$R_L = 2k$	●	$\pm 12$	$\pm 12.7$		$\pm 12$	$\pm 12.6$		V
$I_S$	Supply Current Per Amplifier	$T_A = 125^\circ C$			1.25	1.9		1.3	2.2	mA

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** Typical parameters are defined as the 60% yield of distributions of individual amplifiers; (i.e., out of 100 LT1058s or, 100 LT1057s, typically 240 op amps, or 120 for the LT1057, will be better than the indicated specification).

**Note 3:** This parameter is tested on a sample basis only.

**Note 4:** Current noise is calculated from the formula:

$$i_n = (2qI_b)^{1/2}$$

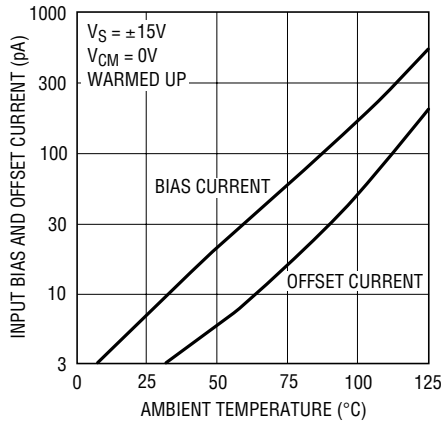
where  $q = 1.6 \cdot 10^{-19}$  coulomb. The noise of source resistors up to 1G swamps the contribution of current noise.

**Note 5:** This parameter is not 100% tested.

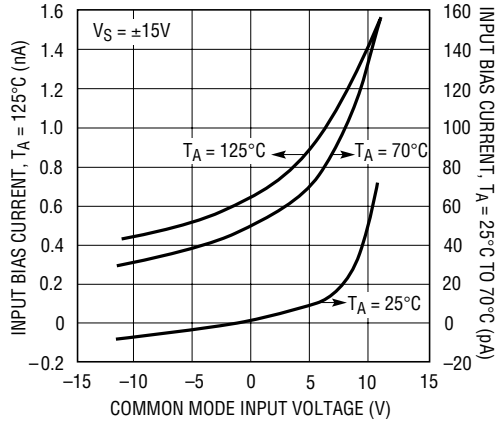
**Note 6:** Gain-bandwidth product is not tested. It is guaranteed by design and by inference from the slew rate measurement.

## TYPICAL PERFORMANCE CHARACTERISTICS

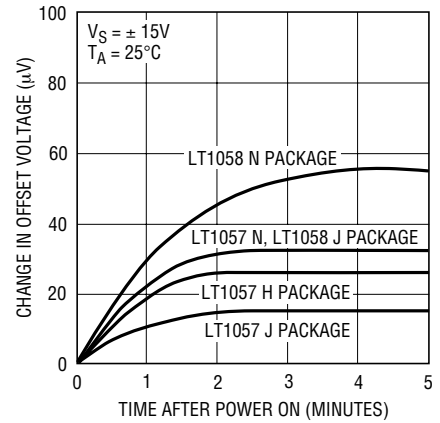
**Input Bias and Offset Currents vs Temperature**



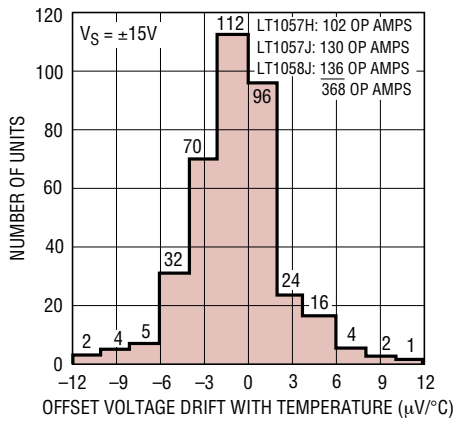
**Input Bias Current Over the Common-Mode Range**



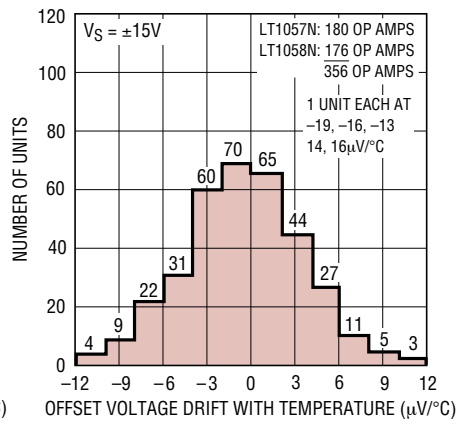
**Warm-Up Drift**



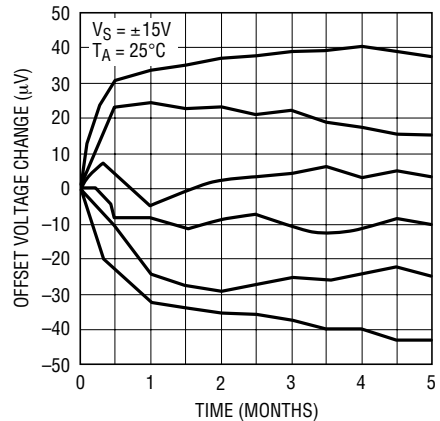
**Distribution of Offset Voltage Drift with Temperature (H and J Package)**



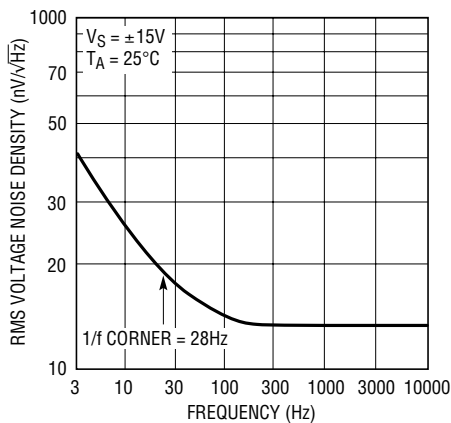
**Distribution of Offset Voltage Drift with Temperature (Plastic N Package)**



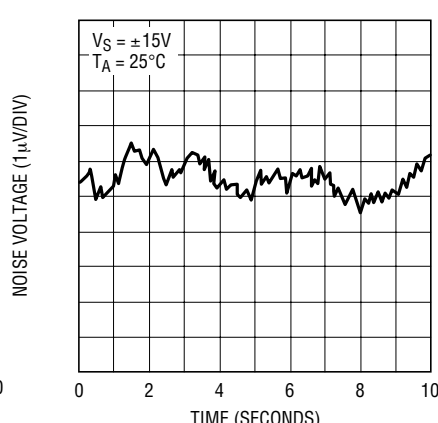
**Long-Term Drift of Representative Units**



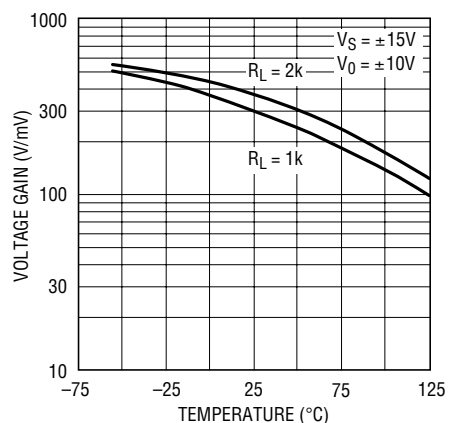
**Voltage Noise vs Frequency**



**0.1Hz to 10Hz Noise**

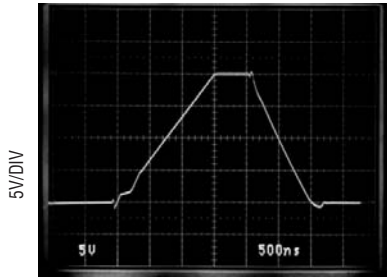


**Voltage Gain vs Temperature**



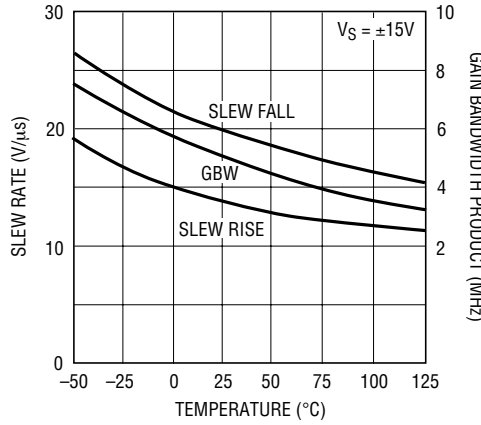
# TYPICAL PERFORMANCE CHARACTERISTICS

Large-Signal Response



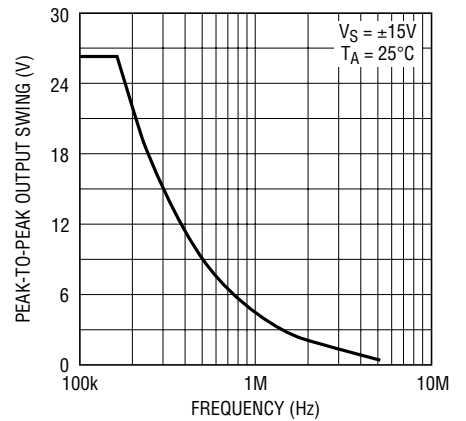
$A_V = +1$   
 $C_L = 100\text{pF}$   
 $0.5\mu\text{s}/\text{DIV}$

Slew Rate, Gain-Bandwidth Product vs Temperature



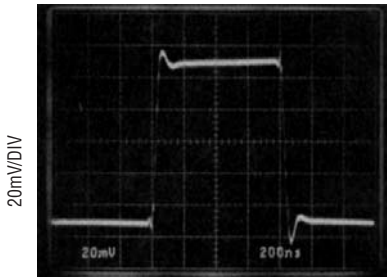
LT1057/1058 • TPC10

Undistorted Output Swing vs Frequency



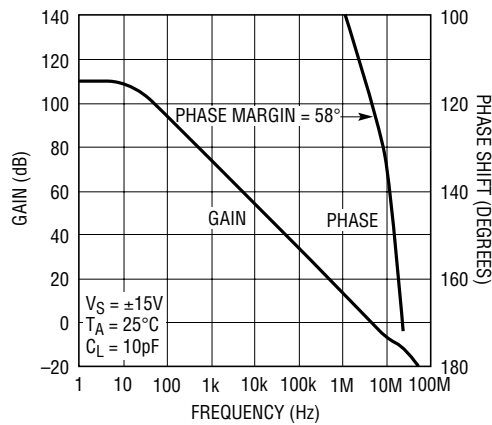
LT1057/1058 • TPC11

Small-Signal Response



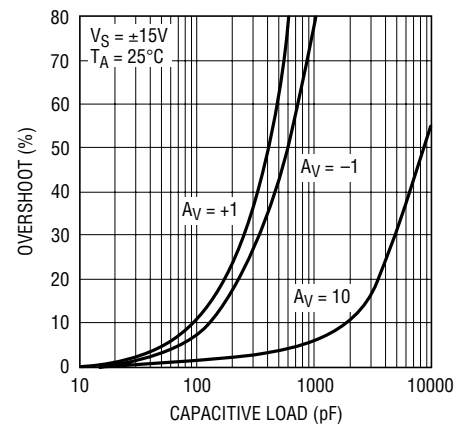
$A_V = +1$   
 $C_L = 100\text{pF}$   
 $0.2\mu\text{s}/\text{DIV}$

Gain, Phase Shift vs Frequency



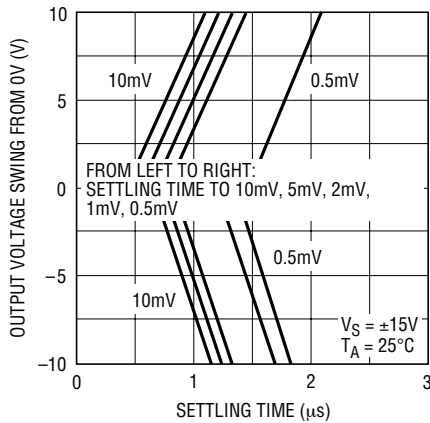
LT1057/1058 • TPC12

Capacitive Load Handling



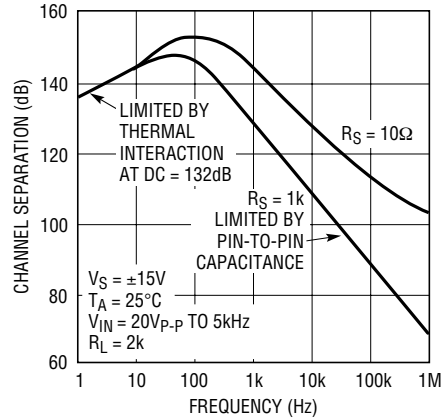
LT1057/1058 • TPC13

Settling Time



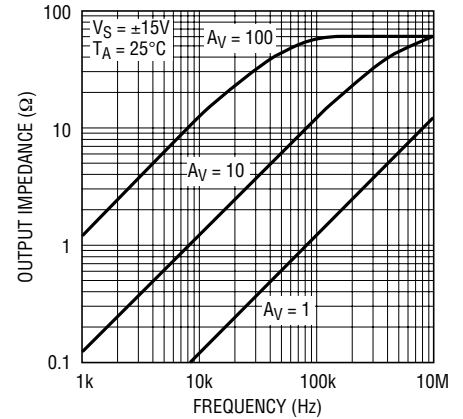
LT1057/1058 • TPC14

Channel Separation vs Frequency



LT1057/1058 • TPC15

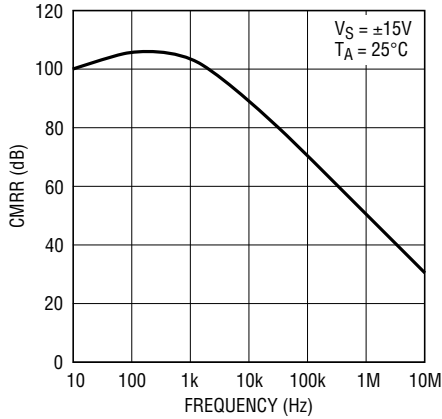
Output Impedance vs Frequency



LT1057/1058 • TPC16

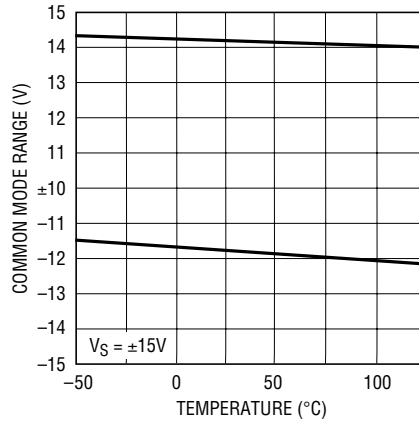
## TYPICAL PERFORMANCE CHARACTERISTICS

**Common Mode Rejection Ratio vs Frequency**



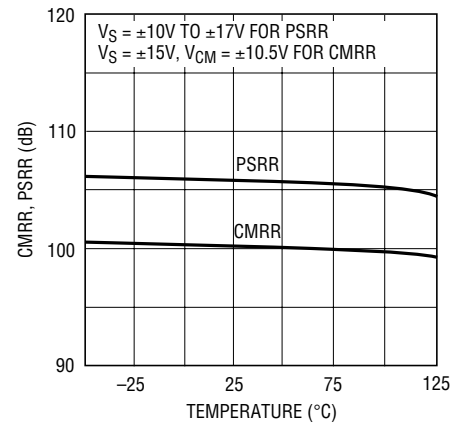
LT1057/1058 • TPC17

**Common Mode Range vs Temperature**



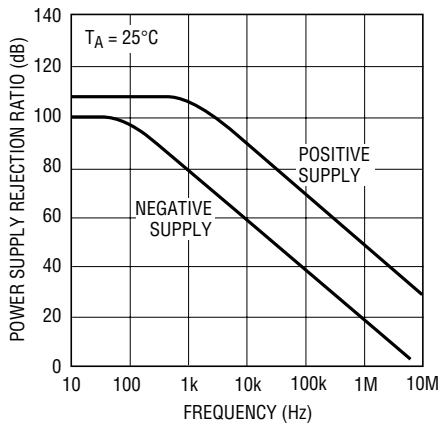
LT1057/1058 • TPC18

**Common Mode and Power Supply Rejections vs Temperature**



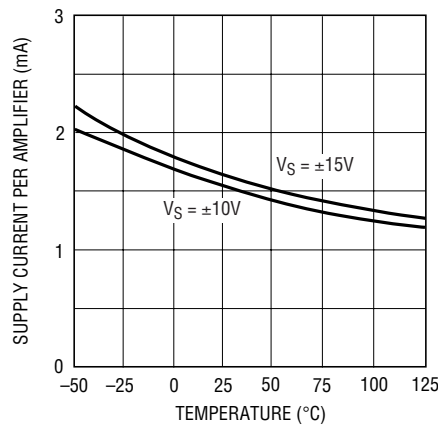
LT1057/1058 • TPC19

**Power Supply Rejection Ratio vs Frequency**



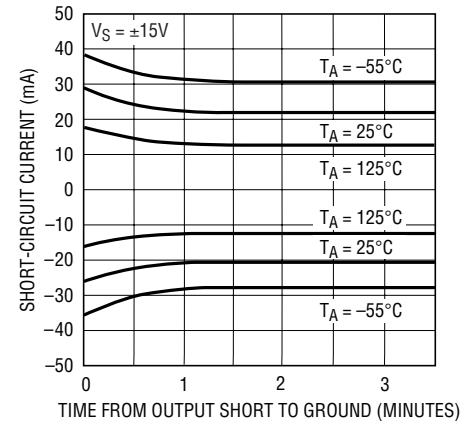
LT1057/1058 • TPC20

**Supply Current vs Temperature**



LT1057/1058 • TPC21

**Short-Circuit Current vs Time (One Output Shorted to Ground)**



LT1057/1058 • TPC22

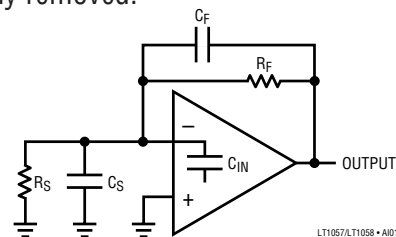
## APPLICATIONS INFORMATION

The LT1057 may be inserted directly in LF353, LF412, LF442, TL072, TL082 and OP-215 sockets. The LT1058 plugs into LF347, LF444, TL074 and TL084 sockets. Of course, all standard dual and quad bipolar op amps can also be replaced by these devices.

### High Speed Operation

When the feedback around the op amp is resistive ( $R_F$ ) a pole will be created with  $R_F$ , the source resistance and capacitance ( $R_S$ ,  $C_S$ ), and the amplifier input capacitance ( $C_{IN} \approx 4\text{pF}$ ). In low closed loop gain configurations and

with  $R_S$  and  $R_F$  in the kilohm range, this pole can create excess phase shift and even oscillation. A small capacitor ( $C_F$ ) in parallel with  $R_F$  eliminates this problem. With  $R_S(C_S + C_{IN}) = R_FC_F$ , the effect of the feedback pole is completely removed.



LT1057/LT1058 • A01



## APPLICATIONS INFORMATION

Settling time is measured in a test circuit which can be found in the LT1055/LT1056 data sheet and in Application Note 10.

### Achieving Picoampere/Microvolt Performance

In order to realize the picoampere/microvolt level accuracy of the LT1057/LT1058, proper care must be exercised. For example, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation should be used (e.g., Teflon™, Kel-F); cleaning of all insulating surfaces to remove fluxes and other residues will probably be required. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Board leakage can be minimized by encircling the input circuitry with a guard ring operated at a potential close to that of the inputs; in inverting configurations, the guard ring should be tied to ground, in noninverting connections, to the inverting input. Guarding both sides of the printed circuit board is required. Bulk leakage reduction depends on the guard ring width.

The LT1057/LT1058 have the lowest offset voltage of any dual and quad JFET input op amps available today. However, the offset voltage and its drift with time and temperature are still not as good as on the best bipolar amplifiers (because the transconductance of FETs is considerably lower than that of bipolar transistors). Conversely, this lower transconductance is the main cause of the significantly faster speed performance of FET input op amps.

Offset voltage also changes somewhat with temperature cycling. The AM grades show a typical  $40\mu\text{V}$  hysteresis ( $50\mu\text{V}$  on the M grades) when cycled over the  $-55^\circ\text{C}$  to  $125^\circ\text{C}$  temperature range. Temperature cycling from  $0^\circ\text{C}$  to  $70^\circ\text{C}$  has a negligible (less than  $20\mu\text{V}$ ) hysteresis effect.

The offset voltage and drift performance are also affected by packaging. In the plastic N package, the molding compound is in direct contact with the chip, exerting pressure on the surface. While NPN input transistors are largely unaffected by this pressure, JFET device drift is degraded. Consequently for best drift performance, as shown in the Typical Performance Characteristics distribution plots, the J or H packages are recommended.

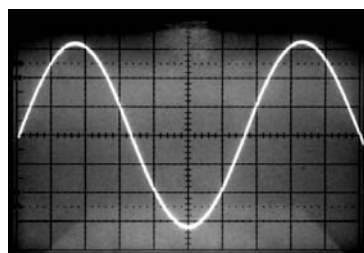
In applications where speed and picoampere bias currents are not necessary, Linear Technology offers the bipolar input, pin compatible LT1013 and LT1014 dual and quad op amps. These devices have significantly better DC specifications than any JFET input device.

### Phase Reversal Protection

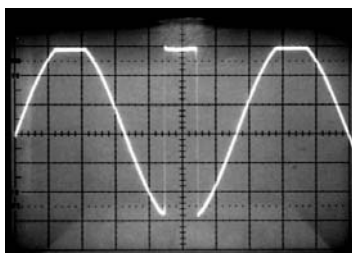
Most industry standard JFET input single, dual and quad op amps (e.g., LF156, LF351, LF353, LF411, LF412, OP-15, OP-16, OP-215, TL084) exhibit phase reversal at the output when the negative common mode limit at the input is exceeded (i.e., below  $-12\text{V}$  with  $\pm 15\text{V}$  supplies). The photos below show a  $\pm 16\text{V}$  sine wave input (A), the response of an LF412A in the unity gain follower mode (B), and the response of the LT1057/LT1058 (C).

The phase reversal of photo (B) can cause lock-up in servo systems. The LT1057/LT1058 does not phase-reverse due to a unique phase reversal protection circuit.

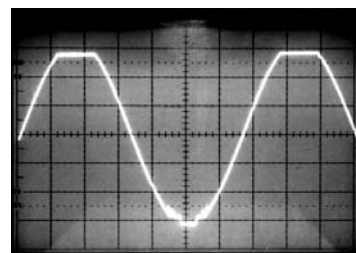
Teflon is a trademark of DuPont.



(A)  $\pm 16\text{V}$  Sine Wave Input



(B) LF412A Output

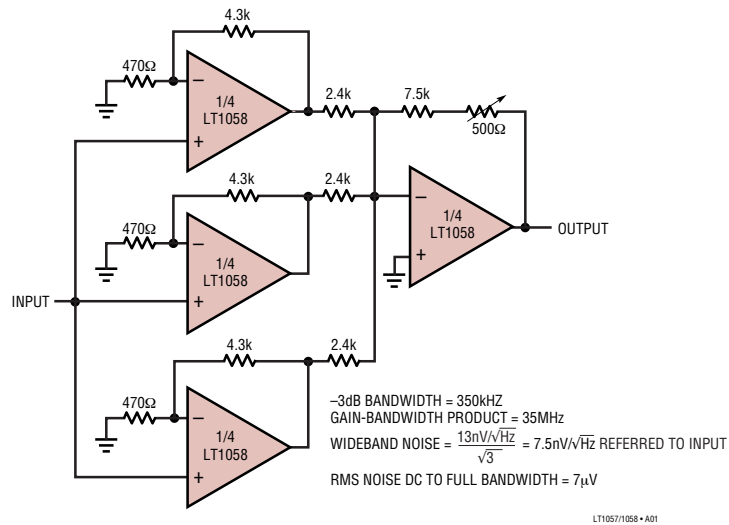


(C) LT1057/LT1058 Output

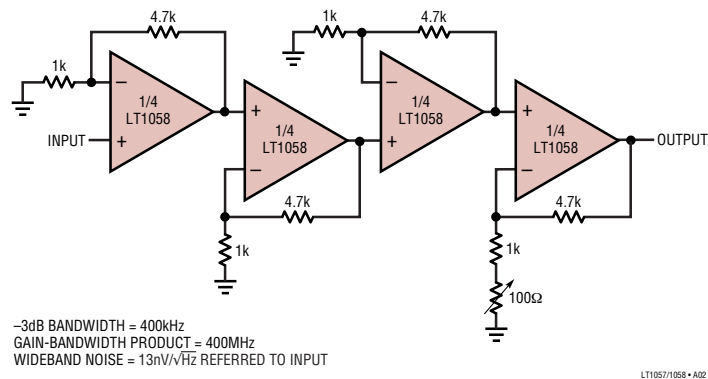
All Photos 5V/Div Vertical Scale,  $50\mu\text{s}/\text{Div}$  Horizontal Scale

## TYPICAL APPLICATIONS

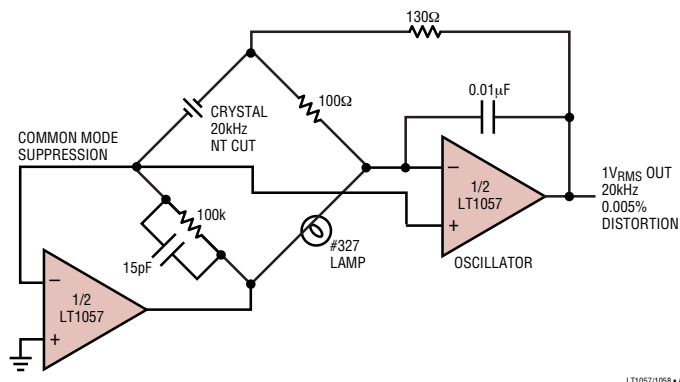
**Low Noise, Wideband, Gain = 100 Amplifier with High Input Impedance**



**Wideband, High Input Impedance, Gain = 1000 Amplifier**



**Low Distortion, Crystal Stabilized Oscillator**



IT1057/1058 • A04

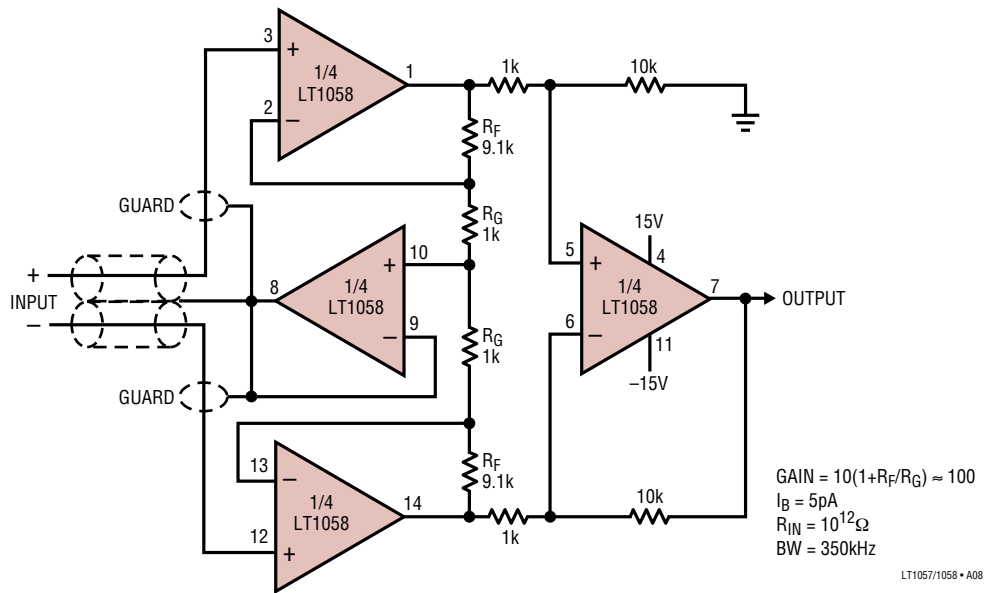
LT1057/1058 • A05

10578fa

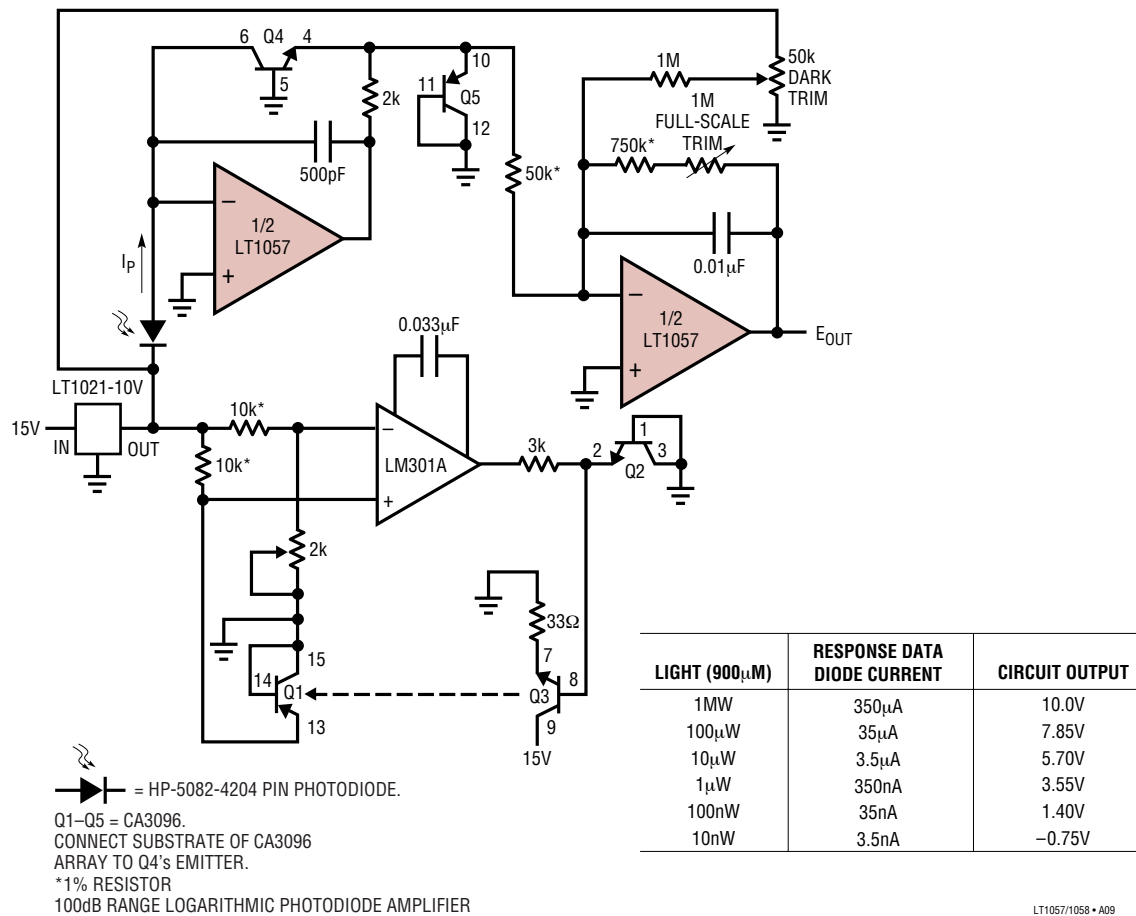
[illegible][illegible]

TYPICAL APPLICATIONS

Instrumentation Amplifier with Shield Driver

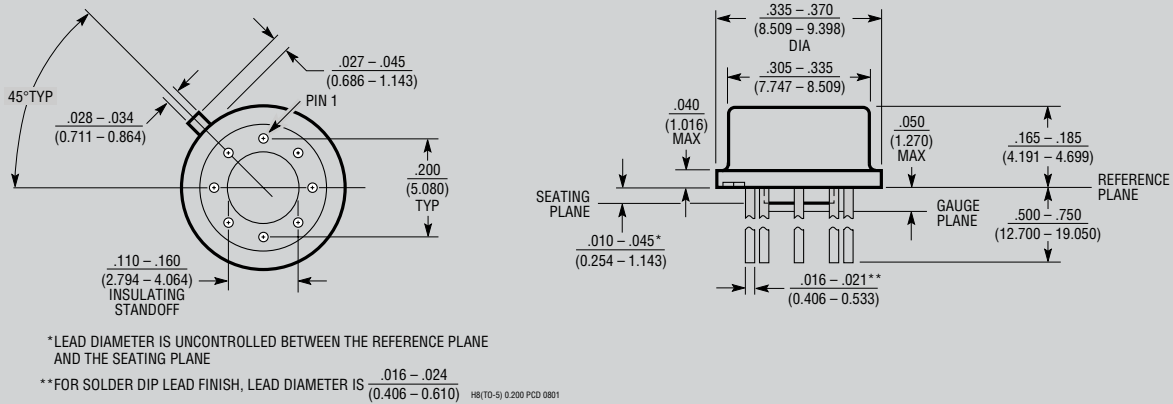


100dB Range Logarithmic Photodiode Amplifier

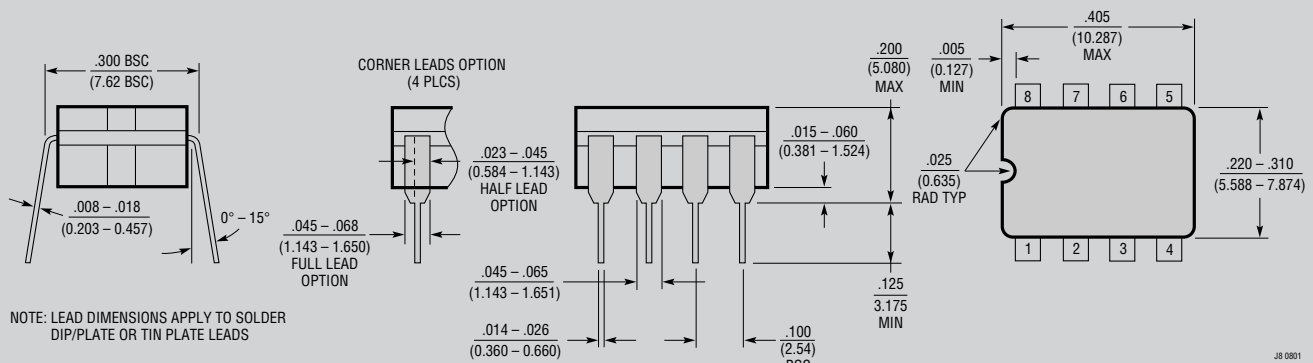


## PACKAGE DESCRIPTION

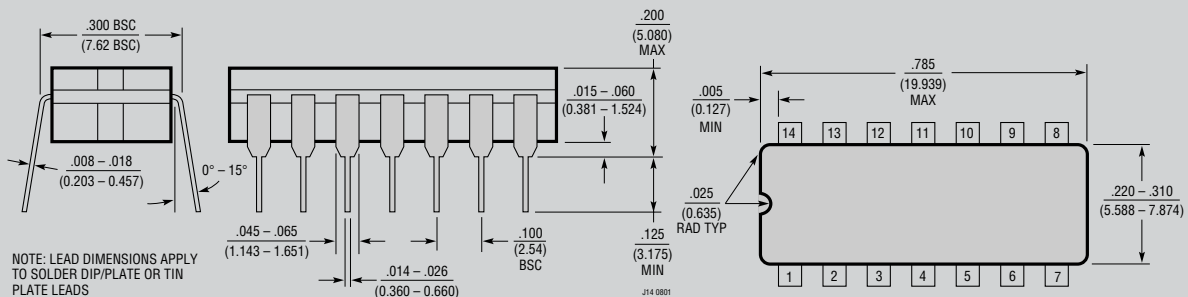
### H Package 8-Lead TO-5 Metal Can (.200 Inch PCD) (Reference LTC DWG # 05-08-1320)



### J8 Package 8-Lead Cerdip (Narrow .300 Inch, Hermetic) (Reference LTC DWG # 05-08-1110)



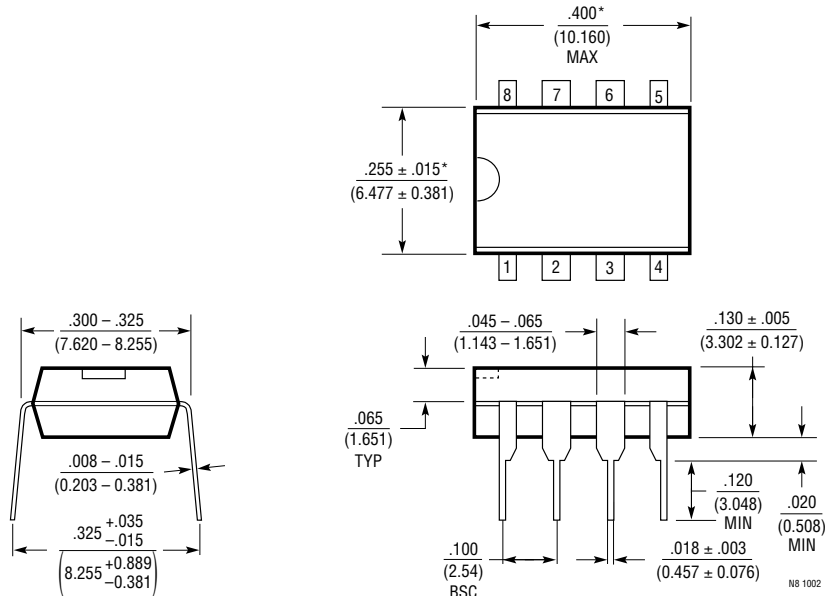
### J Package 14-Lead Cerdip (Narrow .300 Inch, Hermetic) (Reference LTC DWG # 05-08-1110)



**OBSOLETE PACKAGES**

# PACKAGE DESCRIPTION

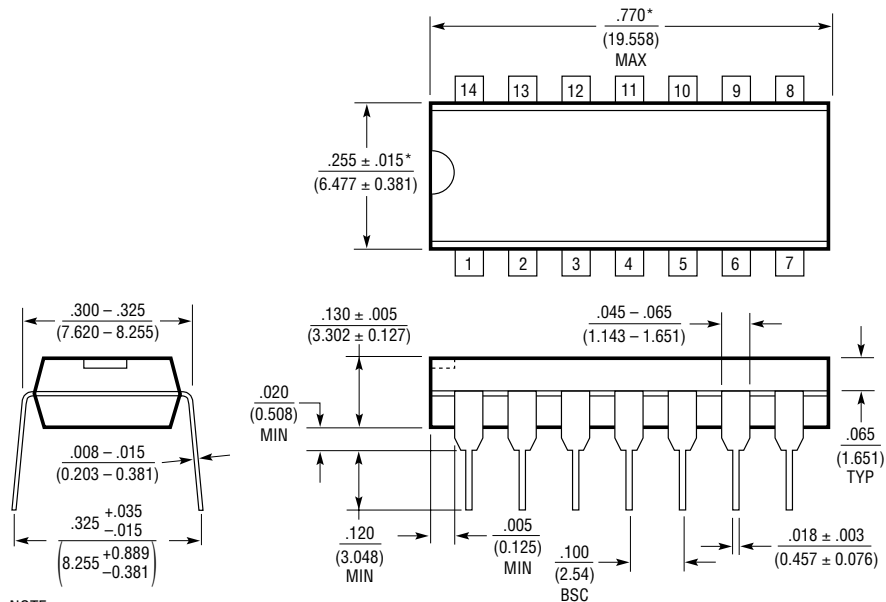
## N8 Package 8-Lead PDIP (Narrow .300 Inch) (Reference LTC DWG # 05-08-1510)



NOTE:

1. DIMENSIONS ARE  $\frac{\text{INCHES}}{\text{MILLIMETERS}}$ \*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.  
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

## N Package 14-Lead PDIP (Narrow .300 Inch) (Reference LTC DWG # 05-08-1510)



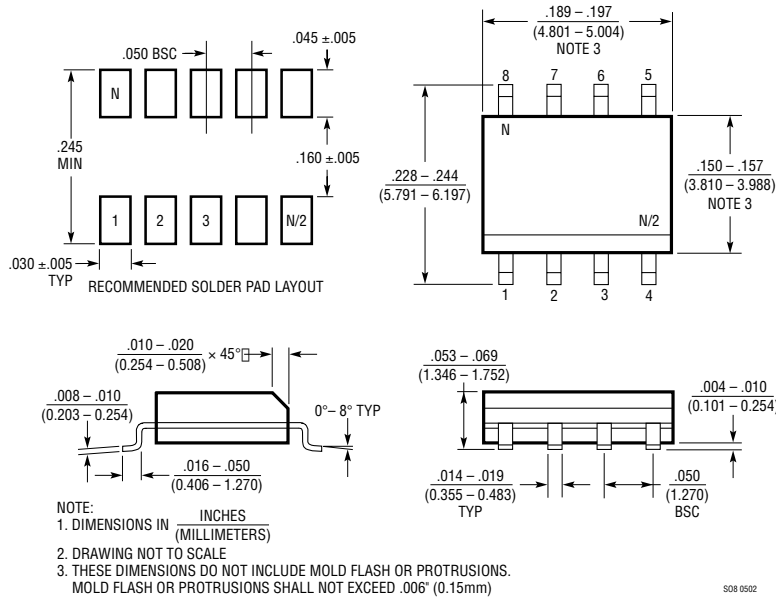
NOTE:

1. DIMENSIONS ARE  $\frac{\text{INCHES}}{\text{MILLIMETERS}}$ \*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.  
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

N14 1002

# PACKAGE DESCRIPTION

## S8 Package 8-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610)



## SW Package 16-Lead Plastic Small Outline (Wide .300 Inch) (Reference LTC DWG # 05-08-1620)

