

FEATURES

- Fully Enhances N-Channel Power MOSFETs
- 8 μ A I_Q Standby Current
- 85 μ A I_Q ON Current
- No External Charge Pump Capacitors
- 4.5V to 18V Supply Range
- Short-Circuit Protection
- Thermal Shutdown via PTC Thermistor
- Status Output Indicates Shutdown
- Available in 8-Pin SOIC

APPLICATIONS

- Laptop Computer Power Switching
- SCSI Termination Power Switching
- Cellular Telephone Power Management
- Battery Charging and Management
- High-Side Industrial and Automotive Switching
- Stepper Motor and DC Motor Control

DESCRIPTION

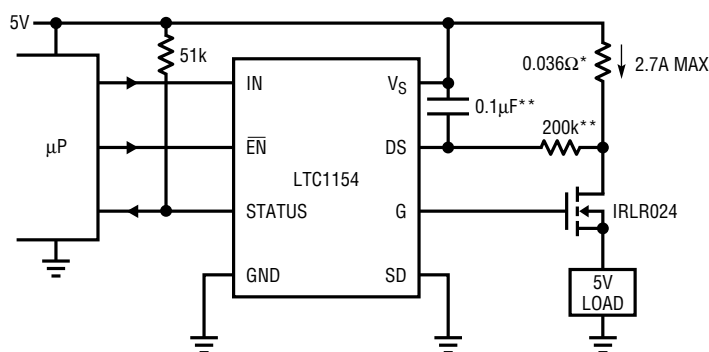
The LTC1154 single high-side gate driver allows using low cost N-channel FETs for high-side switching applications. An internal charge pump boosts the gate drive voltage above the positive rail, fully enhancing an N-channel MOS switch with no external components. Micropower operation, with 8 μ A standby current and 85 μ A operating current, allows use in virtually all systems with maximum efficiency.

Included on chip is programmable over-current sensing. A time delay can be added to prevent false triggering on high in-rush current loads. An active high shutdown input is also provided and interfaces directly to a standard PTC thermistor for thermal shutdown. An open-drain output is provided to report switch status to the μ P. An active low enable input is provided to control multiple switches in banks.

The LTC1154 is available in both 8-pin DIP and 8-pin SOIC packages.

TYPICAL APPLICATION

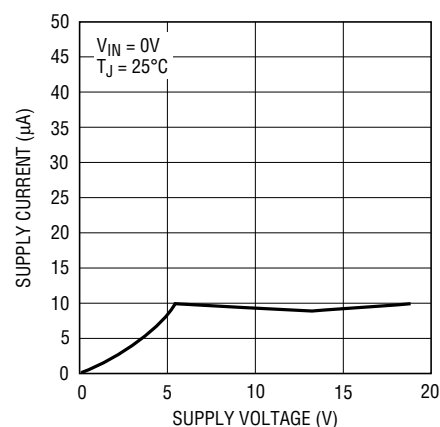
**Ultra-Low Voltage Drop High-Side Switch
with Short-Circuit Protection**



ALL COMPONENTS SHOWN ARE SURFACE MOUNT.
* IMS026 INTERNATIONAL MANUFACTURING SERVICE, INC. (401) 683-9700
** NOT REQUIRED IF LOAD IS RESISTIVE OR INDUCTIVE.

LTC1154 • TA01

Standby Supply Current

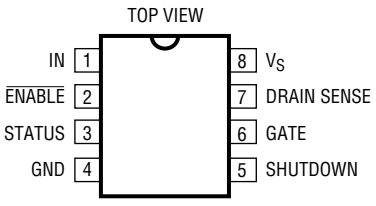
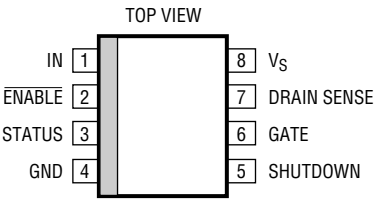


LTC1153 • TA02

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	22V	Current (Any Pin)	50mA
Input Voltage	($V_S + 0.3V$) to ($GND - 0.3V$)	Operating Temperature	
Enable Input Voltage	($V_S + 0.3V$) to ($GND - 0.3V$)	LTC1154C	0°C to 70°C
Gate Voltage	($V_S + 24V$) to ($GND - 0.3V$)	Storage Temperature Range	-65°C to 150°C
Status Output Voltage	15V	Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

 <p>TOP VIEW</p> <p>IN 1, 8 V_S</p> <p>ENABLE 2, 7 DRAIN SENSE</p> <p>STATUS 3, 6 GATE</p> <p>GND 4, 5 SHUTDOWN</p> <p>N8 PACKAGE 8-LEAD PLASTIC DIP</p> <p>LTC1154 • P001</p> <p>$T_{JMAX} = 100^{\circ}C$, $\theta_{JA} = 130^{\circ}C/W$ (N8)</p>	ORDER PART NUMBER	 <p>TOP VIEW</p> <p>IN 1, 8 V_S</p> <p>ENABLE 2, 7 DRAIN SENSE</p> <p>STATUS 3, 6 GATE</p> <p>GND 4, 5 SHUTDOWN</p> <p>S8 PACKAGE 8-LEAD PLASTIC SOIC</p> <p>LTC1154 • P002</p> <p>$T_{JMAX} = 100^{\circ}C$, $\theta_{JA} = 150^{\circ}C/W$</p>	ORDER PART NUMBER
	LTC1154CN8		LTC1154CS8
		S8 PART MARKING	
		1154	

ELECTRICAL CHARACTERISTICS $V_S = 4.5V$ to $18V$, $T_A = 25^{\circ}C$, $V_{\overline{EN}} = 0V$, $V_{SD} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LTC1154C			UNITS
			MIN	TYP	MAX	
V_S	Supply Voltage	●	4.5		18.0	V
I_Q	Quiescent Current OFF	$V_S = 5V$, $V_{IN} = 0V$		8	20	μA
I_Q	Quiescent Current ON	$V_S = 5V$, $V_{IN} = 5V$		85	120	μA
I_Q	Quiescent Current ON	$V_S = 12V$, $V_{IN} = 5V$		180	400	μA
V_{INH}	Input High Voltage	●	2			V
V_{INL}	Input Low Voltage	●			0.8	V
I_{IN}	Input Current	$0V < V_{IN} < V_S$	●		± 1	μA
C_{IN}	Input Capacitance			5		pF
$V_{\overline{EN}H}$	\overline{ENABLE} Input High Voltage	●	3.5	2.6		V
$V_{\overline{EN}L}$	\overline{ENABLE} Input Low Voltage	●		1.0	0.6	V
$I_{\overline{EN}}$	\overline{ENABLE} Input Current	$0V < V_{IN} < V_S$	●		± 1	μA
V_{SDH}	Shutdown Input High Voltage	●	2			V
V_{SDL}	Shutdown Input Low Voltage	●			0.8	V
I_{SD}	Shutdown Input Current	$0V < V_{IN} < V_S$	●		± 1	μA
V_{SEN}	Drain Sense Threshold Voltage	●	80 75	100 100	120 125	mV mV
I_{SEN}	Drain Sense Input Current	$0V < V_{SEN} < V_S$	●		± 0.1	μA

ELECTRICAL CHARACTERISTICS

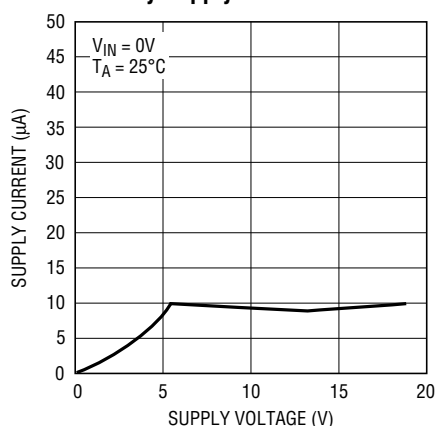
$V_S = 4.5V$ to $18V$, $T_A = 25^\circ C$, $V_{EN} = 0V$, $V_{SD} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1154C			UNITS
				MIN	TYP	MAX	
$V_{GATE} - V_S$	Gate Voltage Above Supply	$V_S = 5V$	●	6.0	7.0	9.0	V
		$V_S = 6V$	●	7.5	8.3	15.0	V
		$V_S = 12V$	●	15.0	18.0	25.0	V
V_{STAT}	Status Output Low Voltage	$I_{STAT} = 400\mu A$	●		0.05	0.4	V
I_{STAT}	Status Output Leakage Current	$V_{STAT} = 12V$	●			1	μA
t_{ON}	Turn-ON Time	$V_S = 5V$, $C_{GATE} = 1000pF$					
		Time for $V_{GATE} > V_S + 2V$		30	110	300	μs
		Time for $V_{GATE} > V_S + 5V$		100	450	1000	μs
		$V_S = 12V$, $C_{GATE} = 1000pF$					
t_{OFF}	Turn-OFF Time	Time for $V_{GATE} > V_S + 5V$					
		Time for $V_{GATE} > V_S + 10V$		20	80	200	μs
				50	160	500	μs
		$V_S = 5V$, $C_{GATE} = 1000pF$					
t_{SC}	Short-Circuit Turn-OFF Time	Time for $V_{GATE} < 1V$		10	36	60	μs
		$V_S = 12V$, $C_{GATE} = 1000pF$					
		Time for $V_{GATE} < 1V$		10	28	60	μs
		$V_S = 5V$, $C_{GATE} = 1000pF$					
t_{SD}	Shutdown Turn-OFF Time	Time for $V_{GATE} < 1V$		5	25	40	μs
		$V_S = 12V$, $C_{GATE} = 1000pF$					
		Time for $V_{GATE} < 1V$		5	23	40	μs
		$V_S = 5V$, $C_{GATE} = 1000pF$					
		Time for $V_{GATE} < 1V$			17	40	μs
		$V_S = 12V$, $C_{GATE} = 1000pF$			13	35	μs

The ● denotes specifications which apply over the operating temperature range.

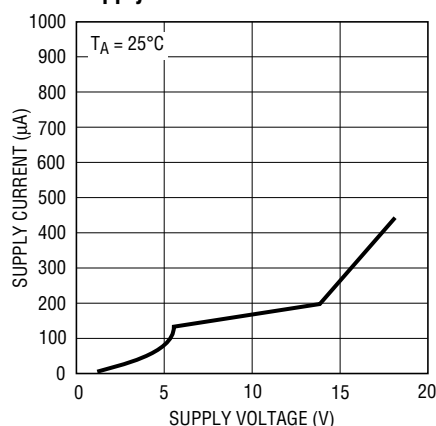
TYPICAL PERFORMANCE CHARACTERISTICS

Standby Supply Current



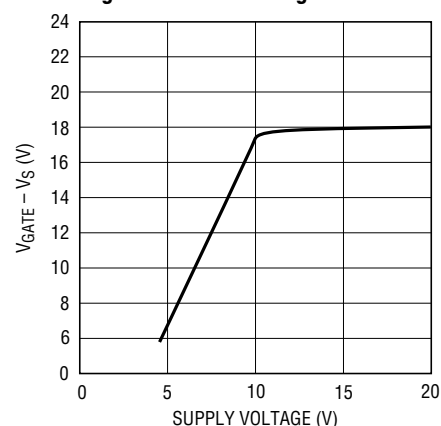
LTC1154 • TPC01

Supply Current ON



LTC1154 • TPC02

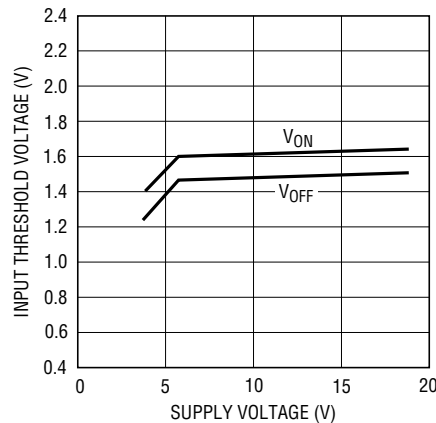
High-Side Gate Voltage



LTC1154 • TPC03

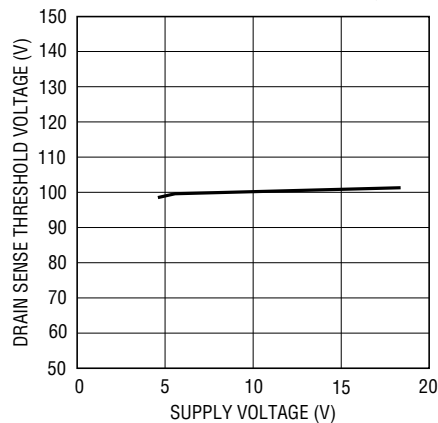
TYPICAL PERFORMANCE CHARACTERISTICS

Input Threshold Voltage



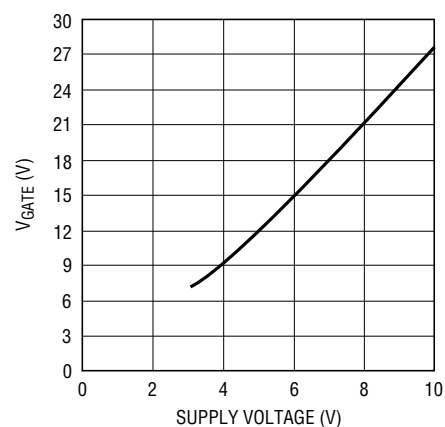
LTC1154 • TPC04

Drain Sense Threshold Voltage



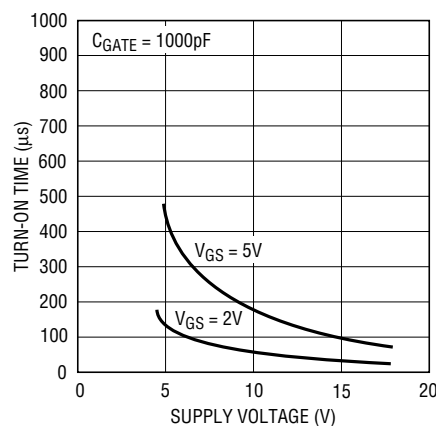
LTC1154 • TPC05

Low-Side Gate Voltage



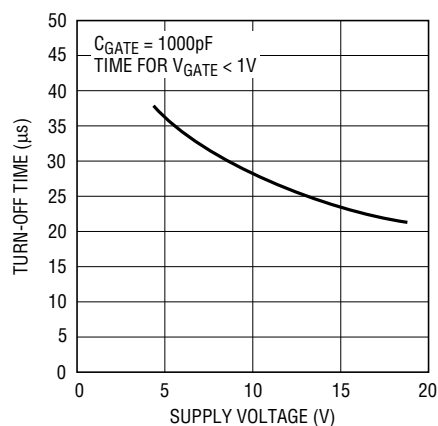
LTC1154 • TPC06

Turn-ON Time



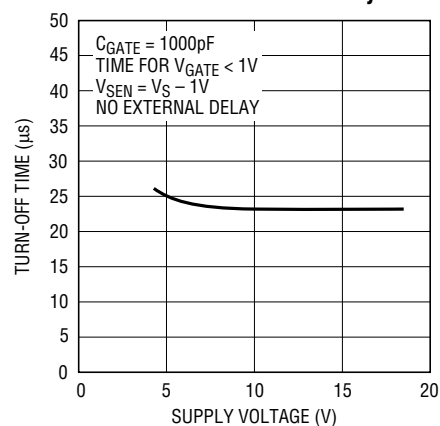
LTC1154 • TPC07

Turn-OFF Time



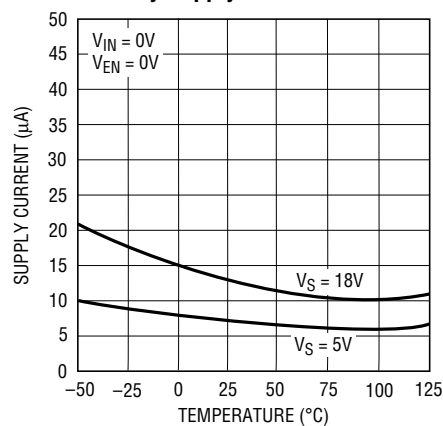
LTC1154 • TPC08

Short-Circuit Turn-OFF Delay Time



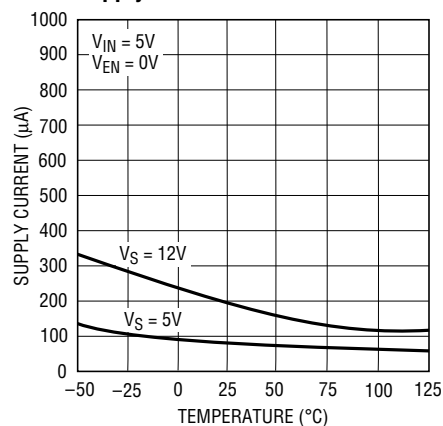
LTC1154 • TPC09

Standby Supply Current



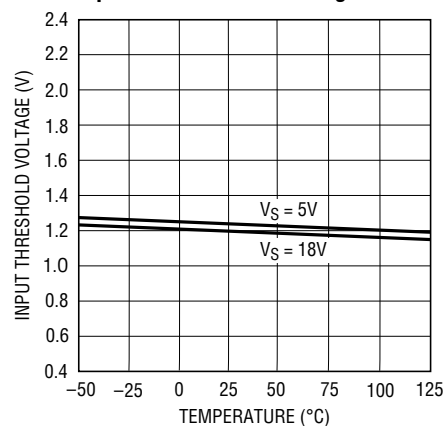
LTC1154 • TPC10

Supply Current ON



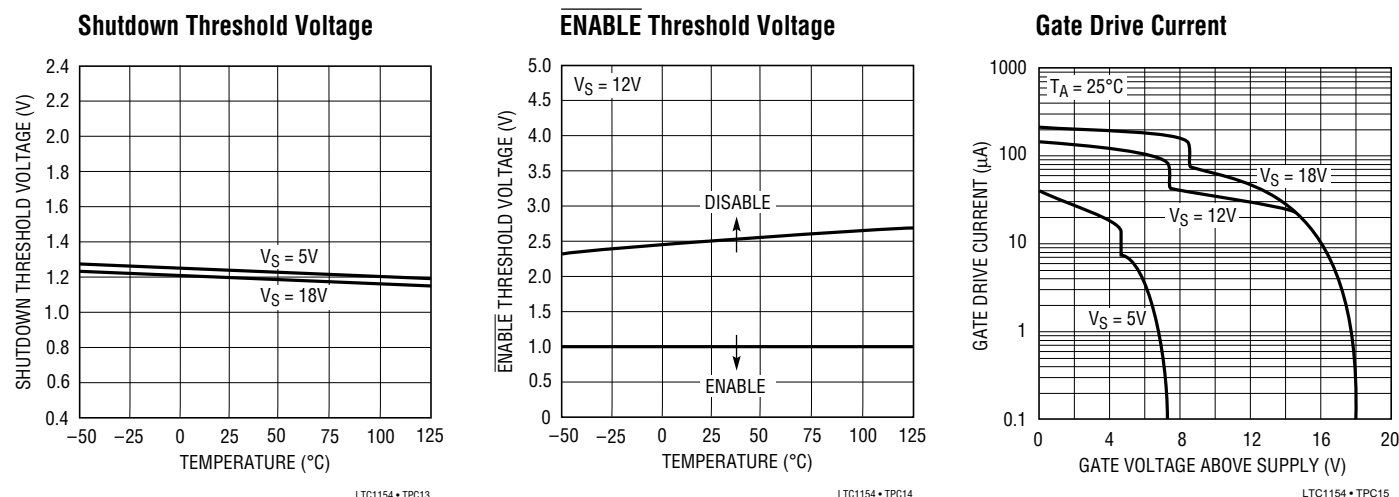
LTC1154 • TPC11

Input ON Threshold Voltage



LTC1154 • TPC12

TYPICAL PERFORMANCE CHARACTERISTICS



PIN FUNCTIONS

Input and Shutdown Pins

The LTC1154 input pin is active high and activates all of the protection and charge pump circuitry when switched ON. The shutdown pin is designed to immediately disable the switch if a secondary fault condition (over temperature, etc.) is detected. The LTC1154 logic and shutdown inputs are high impedance CMOS gates with ESD protection diodes to ground and supply and therefore should not be forced beyond the power supply rails. The shutdown pin should be connected to ground when not in use.

ENABLE Input Pin

The $\overline{\text{ENABLE}}$ input can be used to enable a number of LTC1154 high-side switches in banks or to provide a secondary means of control. It can also act as an inverting input. The $\overline{\text{ENABLE}}$ input is a high impedance CMOS gate with ESD clamp diodes to ground and supply and therefore should not be forced beyond the power supply rails. This pin should be grounded when not in use.

Gate Drive Pin

The gate drive pin is either driven to ground when the switch is turned OFF or driven above the supply rail when the switch is turned ON. This pin is a relatively high impedance when driven above the rail (the equivalent of a

few hundred k Ω). Care should be taken to minimize any loading of this pin by parasitic resistance to ground or supply.

Supply Pin

The supply pin of the LTC1154 serves two vital purposes. The first is obvious: it powers the input, gate drive, regulation and protection circuitry. The second purpose is less obvious: it provides a Kelvin connection to the top of the drain sense resistor for the internal 100mV reference.

The LTC1154 is designed to be continuously powered so that the gate of the MOSFET is actively driven at all times. If it is necessary to remove power from the supply pin and then re-apply it, the input pin (or enable pin) should be cycled a few milliseconds *after* the power is re-applied to reset the input latch and protection circuitry. Also, the input and enable pins should be isolated with 10k resistors to limit the current flowing through the ESD protection diodes to the supply pin.

The supply pin of the LTC1154 should never be forced below ground as this may result in permanent damage to the device. A 300 Ω resistor should be inserted in series with the ground pin if negative supply voltage transients are anticipated.

PIN FUNCTIONS

Drain Sense Pin

The drain sense pin is compared against the supply pin voltage. If the voltage at this pin is more than 100mV below the supply pin, the input latch will be reset and the MOSFET gate will be quickly discharged. Cycle the input, or $\overline{\text{ENABLE}}$ input, to reset the short-circuit latch and turn the MOSFET back on.

This pin is also a high impedance CMOS gate with ESD protection and therefore should not be forced beyond the power supply rails. To defeat the over current protection, short the drain sense to supply.

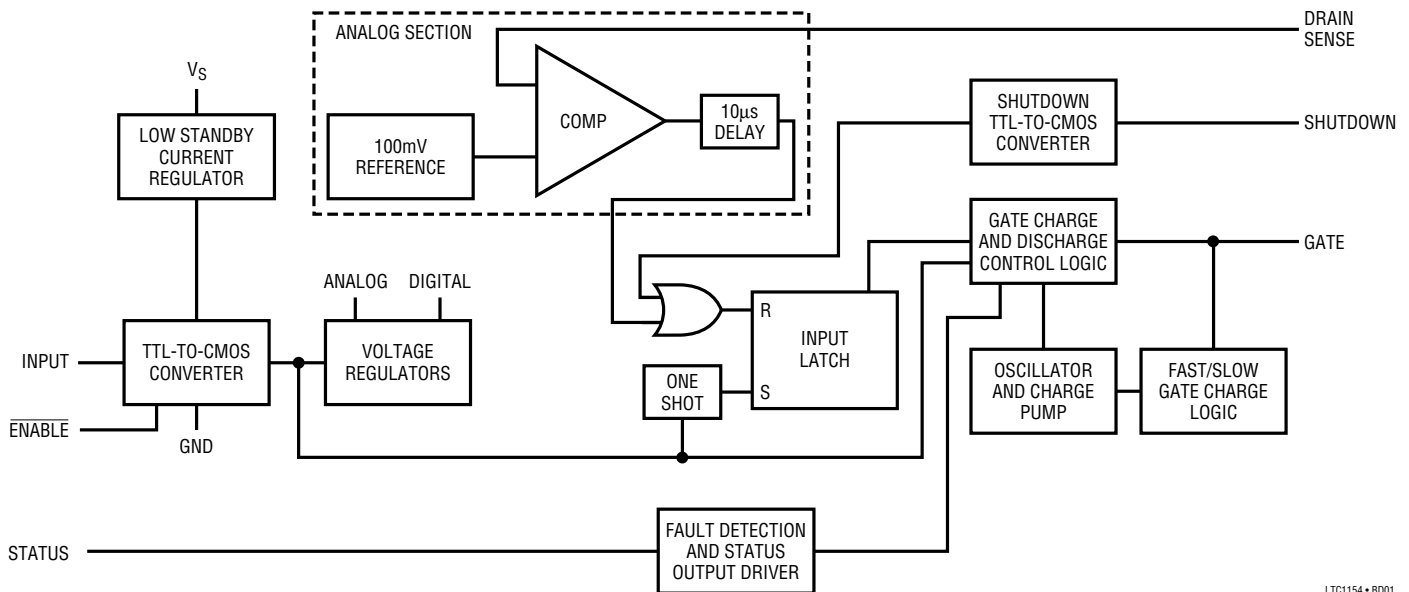
Some loads, such as large supply capacitors, lamps, or motors require high in-rush currents. An RC time delay can be added between the sense resistor and the drain

sense pin to ensure that the drain sense circuitry does not false-trigger during start-up. This time constant can be set from a few microseconds to many seconds. However, very long delays may put the MOSFET in risk of being destroyed by a short-circuit condition. (see Applications Information Section).

Status Pin


The status pin is an open-drain output which is driven low whenever a fault condition is detected. A 51k pull-up resistor should be connected between this output and a logic supply. The status pins of multiple LTC1154s can be OR'd together if independent fault sensing is not required. No connection is required to this pin when not in use.

BLOCK DIAGRAM




LTC1154 • BD01

TRUTH TABLE

INPUTS			OUTPUTS		SWITCH CONDITION
IN	EN	SD	GATE	STATUS	
X	H	X	L	H	SWITCH OFF
L	X	X	L	H	SWITCH OFF
H	L	L	H	H	SWITCH ON
H	L	L	L	L	SWITCH LATCHED OFF (OVER CURRENT)
H	L		L	L	SWITCH LATCHED OFF (SHUTDOWN)

L = LOGIC LOW
H = LOGIC HIGH
X = IRRELEVANT

 = EDGE TRIGGERED

The Truth Table demonstrates how the LTC1154 receives inputs and returns status information to the μ P. The ENABLE and input signal from the μ P controls the switch in its normal operating mode, where the rise and fall time of the gate drive are controlled to limit EMI and RFI emissions. The shutdown and over-current detection circuitry however, switch the gate off at a much higher rate to limit the exposure of the MOSFET switch and the load to dangerous conditions. The status pin remains high as long as the switch is operating normally, and is driven low only when a fault condition is detected. Note that the shutdown pin is edge-sensitive and latches the output off even if the shutdown pin returns to a low state.

LTC1154 OPERATION

The LTC1154 is a single micropower MOSFET driver with built-in protection, status feedback and gate charge pump. The LTC1154 consists of the following functional blocks:

TTL and CMOS Compatible Inputs

The LTC1154 input and shutdown input have been designed to accommodate a wide range of logic families. Both input thresholds are set at about 1.3V with approximately 100mV of hysteresis.

A low standby current voltage regulator provides continuous bias for the TTL-to-CMOS converter. The TTL-to-CMOS converter output enables the rest of the circuitry. In this way the power consumption is kept to a minimum in the standby mode.

ENABLE Input

The ENABLE input is CMOS compatible and inhibits the input signal whenever it is held logic high. This input should be grounded when not in use.

Internal Voltage Regulation

The output of the TTL-to-CMOS converter drives two regulated supplies which power the low voltage CMOS logic and analog blocks. The regulator outputs are isolated from each other so that the noise generated by the charge

pump logic is not coupled into the 100mV reference or the analog comparator.

Gate Charge Pump

Gate drive for the MOSFET switch is produced by an adaptive charge pump circuit which generates a gate voltage substantially higher than the power supply voltage. The charge pump capacitors are included on chip and therefore no external components are required to generate the gate drive.

Drain Current Sense

The LTC1154 is configured to sense the current flowing into the drain of the power MOSFET in a high-side application. An internal 100mV reference is compared to the drop across a sense resistor (typically 0.002Ω to 0.10Ω) in series with the drain lead. If the drop across this resistor exceeds the internal 100mV threshold, the input latch is reset and the gate is quickly discharged via a large N-channel transistor.

Controlled Gate Rise and Fall Times

When the input is switched ON and OFF, the gate is charged by the internal charge pump and discharged in a controlled manner. The charge and discharge rates have

LTC1154 OPERATION

been set to minimize RFI and EMI emissions in normal operation. If a short-circuit or current overload condition is encountered, the gate is discharged very quickly (typically a few microseconds) by a large N-channel transistor.

Status Output Driver

The status circuitry continuously monitors the fault detection logic. This open-drain output is driven low when the

gate of the MOSFET is driven low by the protection circuitry. The status circuitry is reset along with the input latch when the input, or ENABLE input, is cycled.

APPLICATIONS INFORMATION

MOSFET and Load Protection

The LTC1154 protects the power MOSFET switch by removing drive from the gate as soon as an over-current condition is detected. Resistive and inductive loads can be protected with no external time delay in series with the drain sense pin. Lamp loads, however, require that the over-current protection be delayed long enough to start the lamp but short enough to ensure the safety of the MOSFET.

Resistive Loads

Loads that are primarily resistive should be protected with as short a delay as possible to minimize the amount of time that the MOSFET is subjected to an overload condition. The drain sense circuitry has a built-in delay of approximately 10 μ s to eliminate false triggering by power supply or load transient conditions. This delay is sufficient to “mask” short load current transients and the starting of a small capacitor (<1 μ F) in parallel with the load. The drain sense pin can therefore be connected directly to the drain current sense resistor as shown in Figure 1.

Inductive Loads

Loads that are primarily inductive, such as relays, solenoids and stepper motor windings should be protected with as short a delay as possible to minimize the amount of time that the MOSFET is subjected to an overload condition. The built-in 10 μ s delay will ensure that the over-current protection is not false-triggered by a supply or load transient. No external delay components are required as shown in Figure 2.

Large inductive loads (>0.1mH) may require diodes connected directly across the inductor to safely divert the

stored energy to ground. Many inductive loads have these diodes included. If not, a diode of the proper current rating should be connected across the load, as shown in Figure 2, to safely divert the stored energy.

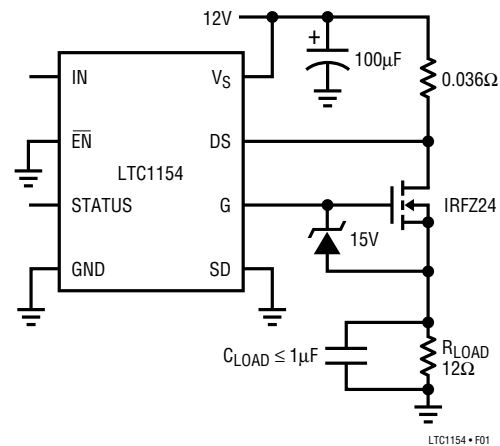


Figure 1. Protecting Resistive Loads

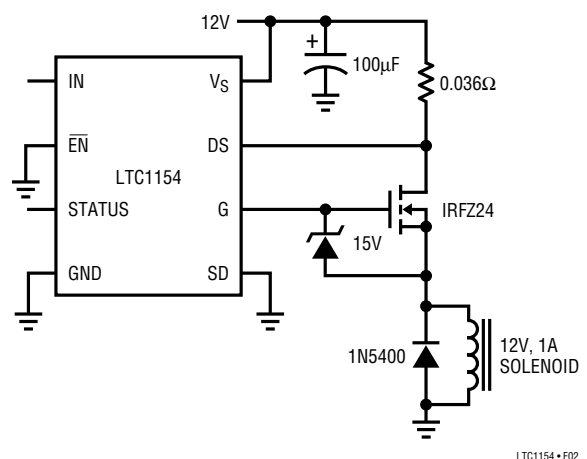


Figure 2. Protecting Inductive Loads

APPLICATIONS INFORMATION

Capacitive Loads

Large capacitive loads, such as complex electrical systems with large bypass capacitors, should be powered using the circuit shown in Figure 3. The gate drive to the power MOSFET is passed through an RC delay network, R1 and C1, which greatly reduces the turn-on ramp rate of the switch. And since the MOSFET source voltage follows the gate voltage, the load is powered smoothly and slowly from ground. This dramatically reduces the start-up current flowing into the supply capacitor(s) which, in turn, reduces supply transients and allows for slower activation of sensitive electrical loads. (Diode, D1, provides a direct path for the LTC1154 protection circuitry to quickly discharge the gate in the event of an over-current condition).

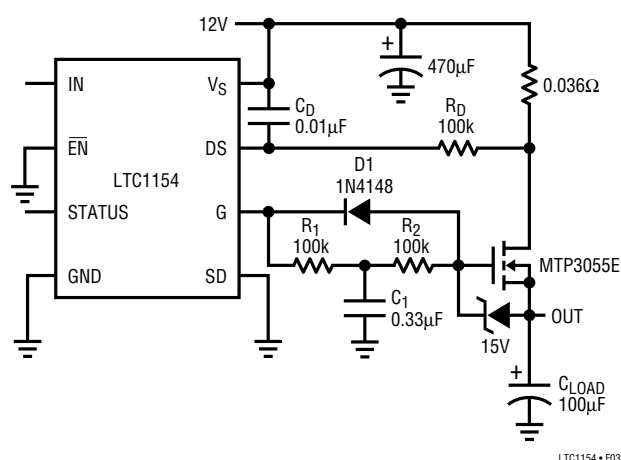


Figure 3. Powering Large Capacitive Loads

The RC network, R_D and C_D, in series with the drain sense input should be set to trip based on the expected characteristics of the load *after* start-up. With this circuit, it is possible to power a large capacitive load and still react quickly to an over-current condition. The ramp rate at the output of the switch as it lifts off ground is approximately:

$$dV/dt = (V_{GATE} - V_{TH}) / (R1 \times C1)$$

And therefore the current flowing into the capacitor during start-up is approximately:

$$I_{START-UP} = C_{LOAD} \times dV/dt$$

Using the values shown in Figure 3, the start-up current is less than 100mA and does not false-trigger the drain sense circuitry which is set at 2.7A with a 1ms delay.

Lamp Loads

The in-rush current created by a lamp during turn-on can be 10 to 20 times greater than the rated operating current. The circuit shown in Figure 4 shifts the current limit threshold up by a factor of 11:1 (to 30A) for 100ms when the bulb is first turned on. The current limit then drops down to 2.7A after the in-rush current has subsided.

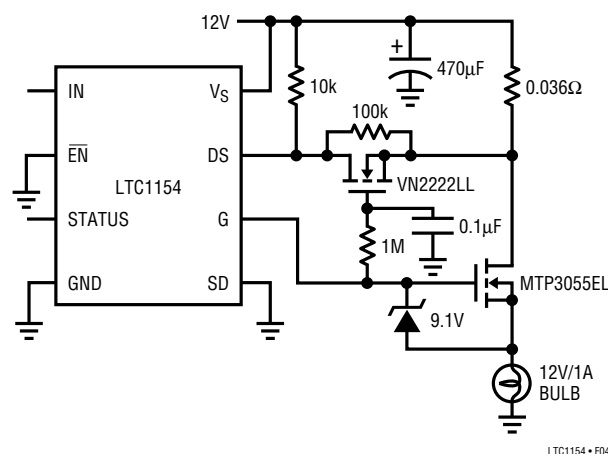


Figure 4. Lamp Driver with Delayed Protection

Selecting R_D and C_D

Figure 5 is a graph of normalized over-current shutdown time versus normalized MOSFET current. This graph is used to select the two delay components, R_D and C_D, which make up a simple RC delay between the drain sense resistor and the drain sense input.

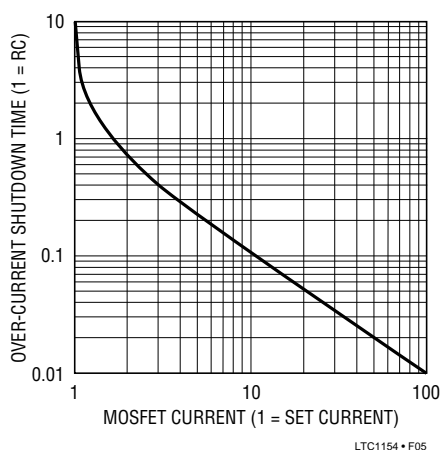


Figure 5. Over-Current Shutdown Time vs MOSFET Current

APPLICATIONS INFORMATION

The Y axis of the graph is normalized to one RC time constant. The X axis is normalized to the current. (The set current is defined as the current required to develop 100mV across the drain sense resistor).

Note that the shutdown time is shorter for increasing levels of MOSFET current. This ensures that the total energy dissipated by the MOSFET is always within the bounds established by the manufacturer for safe operation. (See MOSFET data sheet for further information).

Using a Speed-Up Diode

To reduce the amount of time that the power MOSFET is in a short-circuit condition, “bypass” the delay resistor with a small signal diode as shown in Figure 6. The diode will engage when the drop across the drain sense resistor exceeds about 0.7V, providing a direct path to the sense pin and dramatically reducing the amount of time the

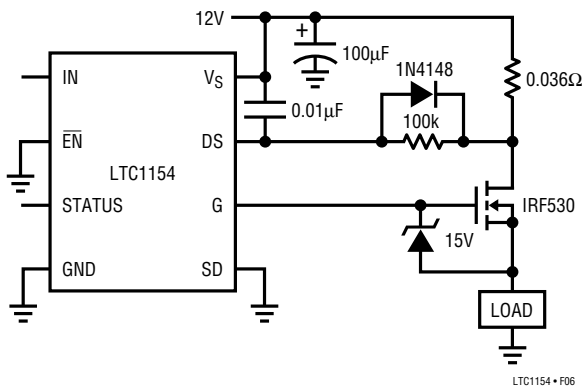


Figure 6. Using a Speed-Up Diode

MOSFET is in an overload condition. The drain sense resistor value is selected to limit the maximum DC current to 2.8A. The diode conducts when the drain current exceeds 20A and reduces the turn-off time to 15µs.

Reverse Battery Protection

The LTC1154 can be protected against reverse battery conditions by connecting a resistor in series with the ground lead as shown in Figure 7. The resistor limits the supply current to less than 50mA with –12V applied.

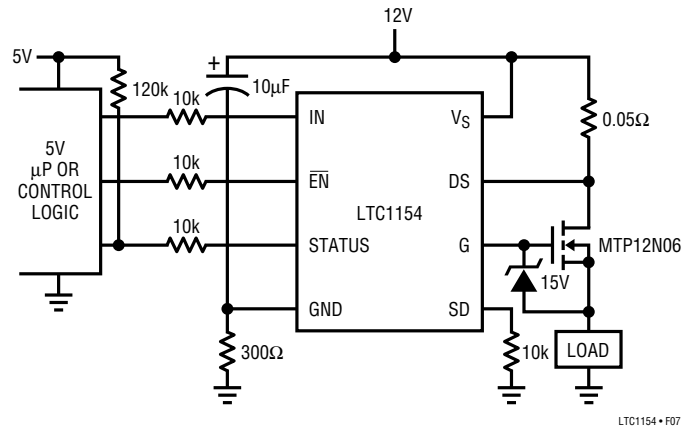


Figure 7. Reverse Battery Protection

Since the LTC1154 draws very little current while in normal operation, the drop across the ground resistor is minimal. The 5V µP (or control logic) is protected by the 10k resistors in series with the input and status pins.

Current Limited Power Supplies

The LTC1154 requires at least 3.5V at the supply pin to ensure proper operation. It is therefore necessary that the supply to the LTC1154 be held higher than 3.5V at all times, even when the output of the switch is short circuited to ground. The output voltage of a current limited regulator may drop very quickly during short circuit and pull the supply pin of the LTC1154 below 3.5V before the shutdown circuitry has had time to respond and remove drive from the gate of the power MOSFET. A supply filter should

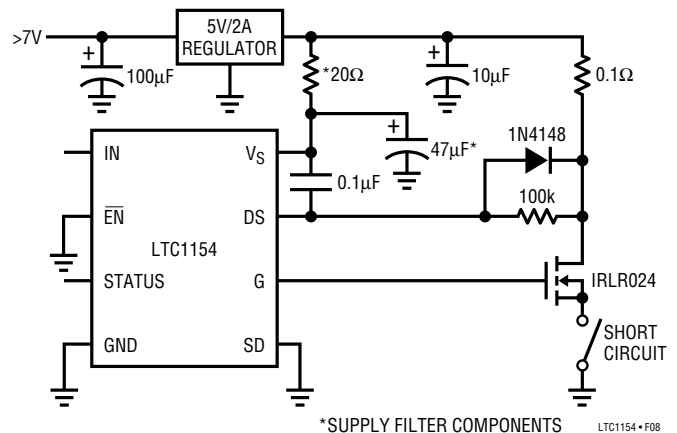


Figure 8. Supply Filter for Current Limited Supplies

APPLICATIONS INFORMATION

be added as shown in Figure 8 which holds the supply pin of the LTC1154 high long enough for the over-current shutdown circuitry to respond and fully discharge the gate.

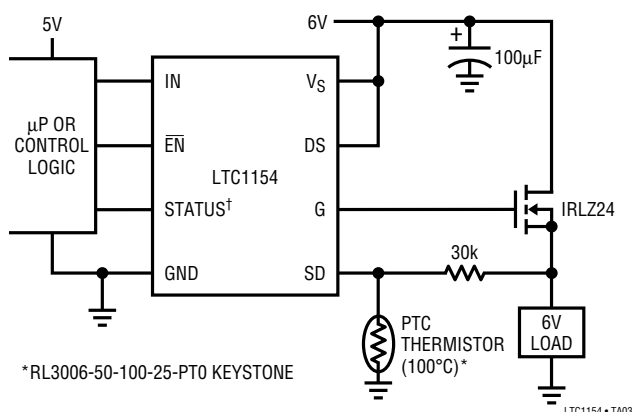
Five volt linear regulators with small output capacitors are the most difficult to protect as they can “switch” from a voltage mode to a current limited mode very quickly. The

large output capacitors on many switching regulators may be able to hold the supply pin of the LTC1154 above 3.5V sufficiently long that this extra filtering is not required.

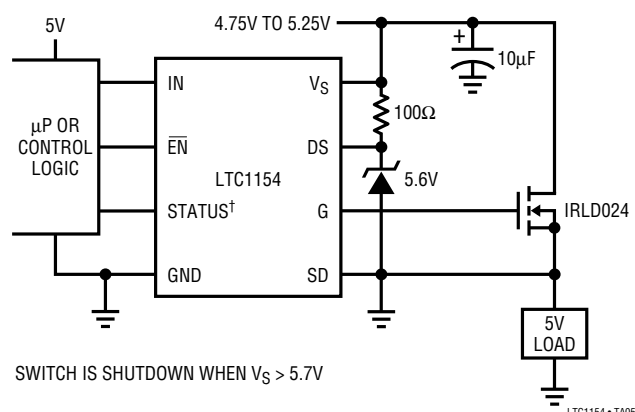
Because the LTC1154 is micropower in both the standby and ON state, the voltage drop across the supply filter is less than 2mV, and does not significantly alter the accuracy of the 100mV drain sense threshold voltage.

TYPICAL APPLICATIONS

High-Side Driver with Thermal Shutdown

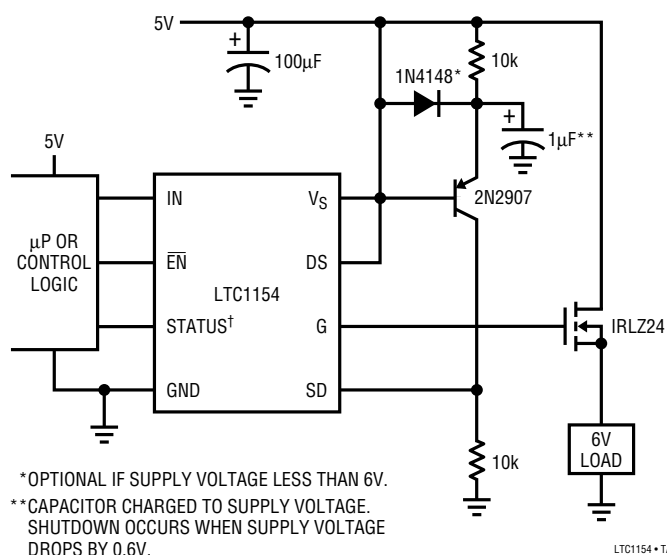


High-Side Driver with Over-Voltage Shutdown

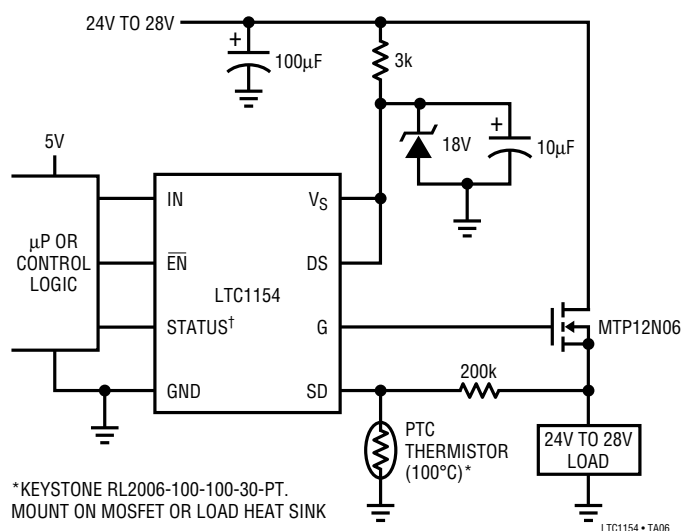


†A 51k pullup resistor should be connected between Status Output and 5V Logic Supply.

High-Side Driver with Under-Voltage Shutdown

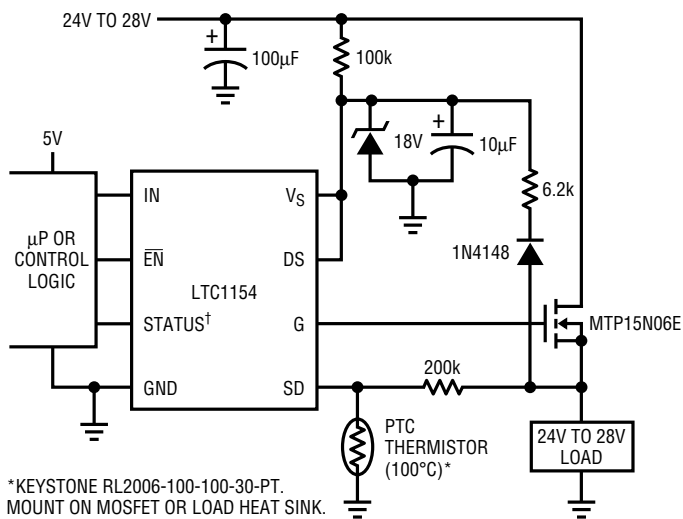


24V to 28V High-Side Switch with Thermal Shutdown



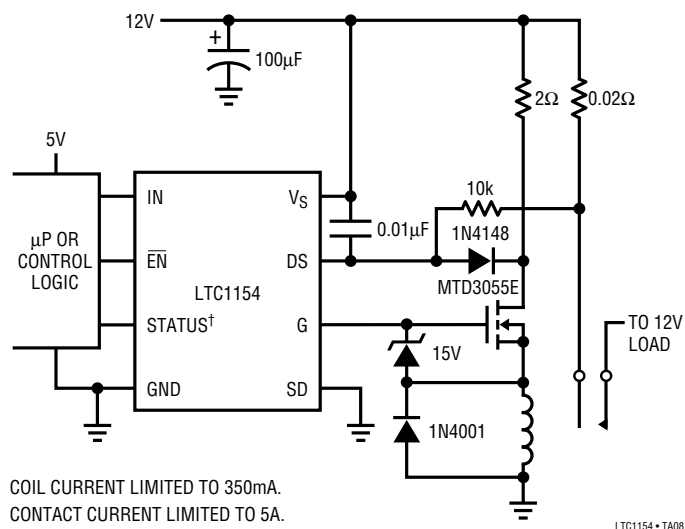
TYPICAL APPLICATIONS

24V to 28V Switch with Bootstrapped Supply

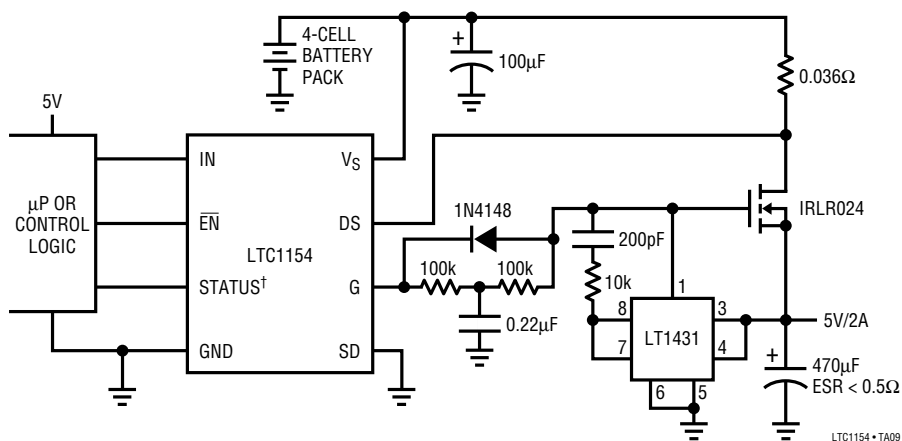


†A 51k pullup resistor should be connected between Status Output and 5V Logic Supply.

High-Side Relay Driver with Over-Current Protection and Status Feedback

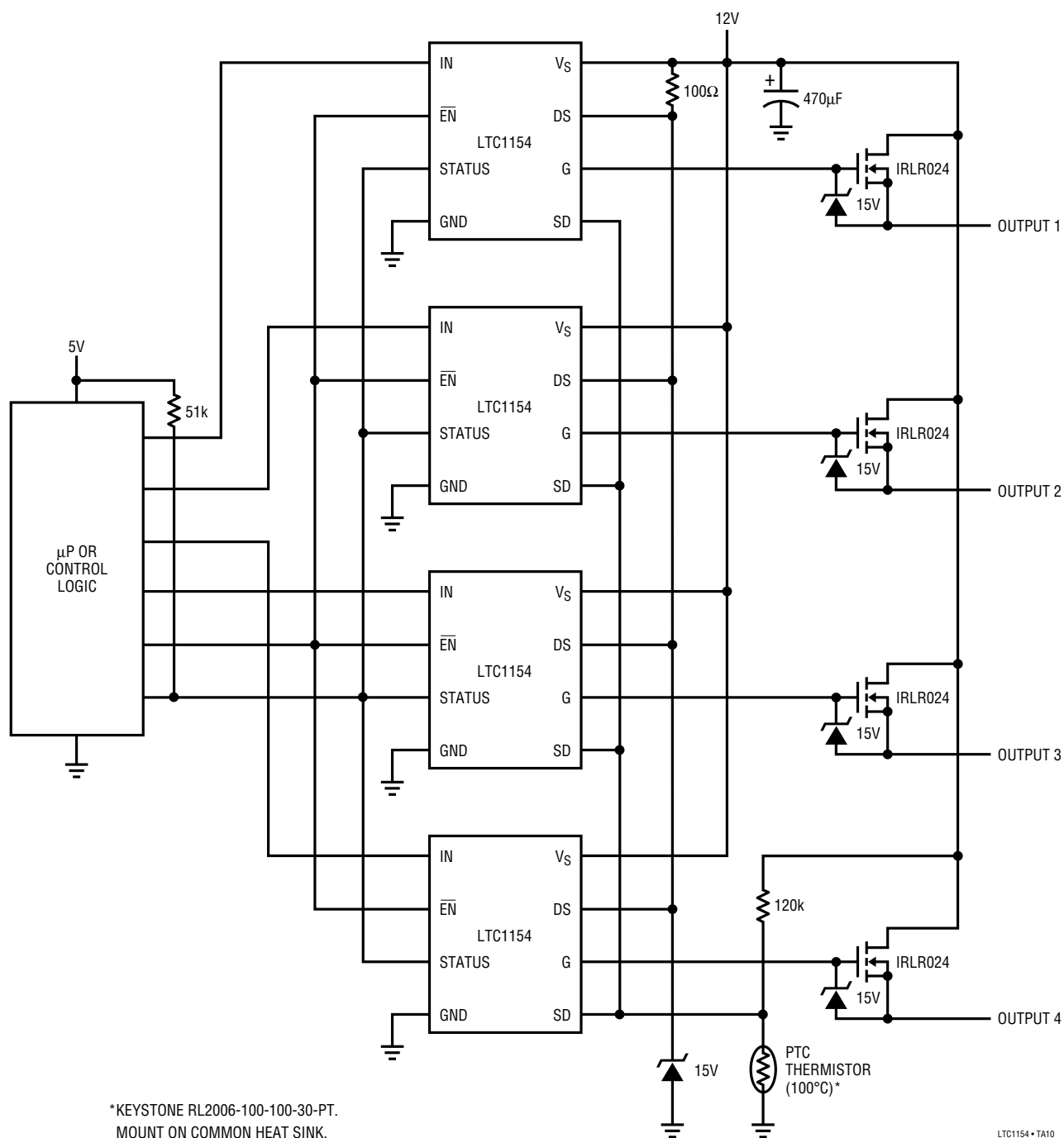


“4-Cell-to-5V” Extremely Low Voltage Drop Regulator with Over-Current Shutdown, Status Feedback, Ramped Turn-ON and 8µA Standby Current



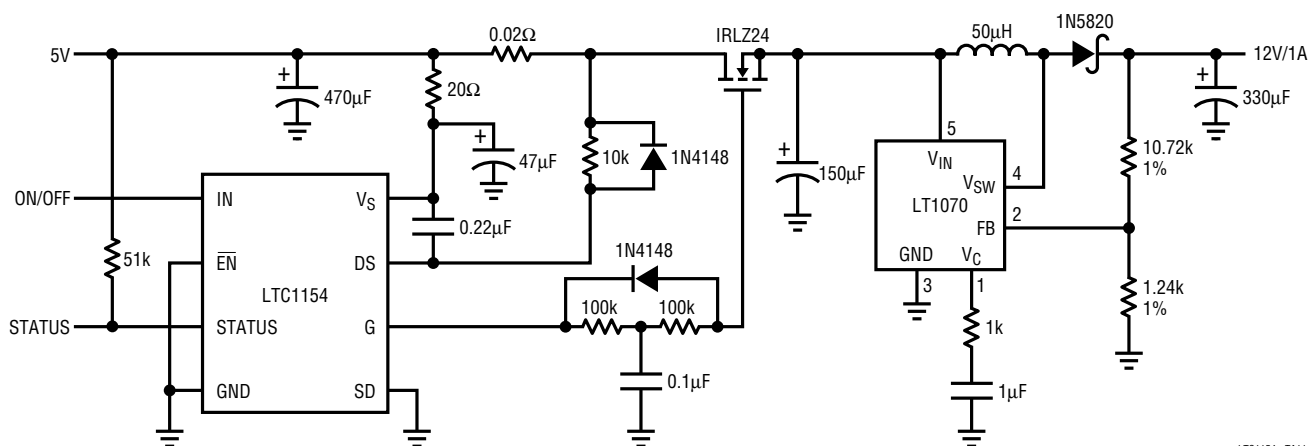
TYPICAL APPLICATIONS

Bank Controlled High-Side Switches with “Global” Thermal and Over-Voltage Shutdown



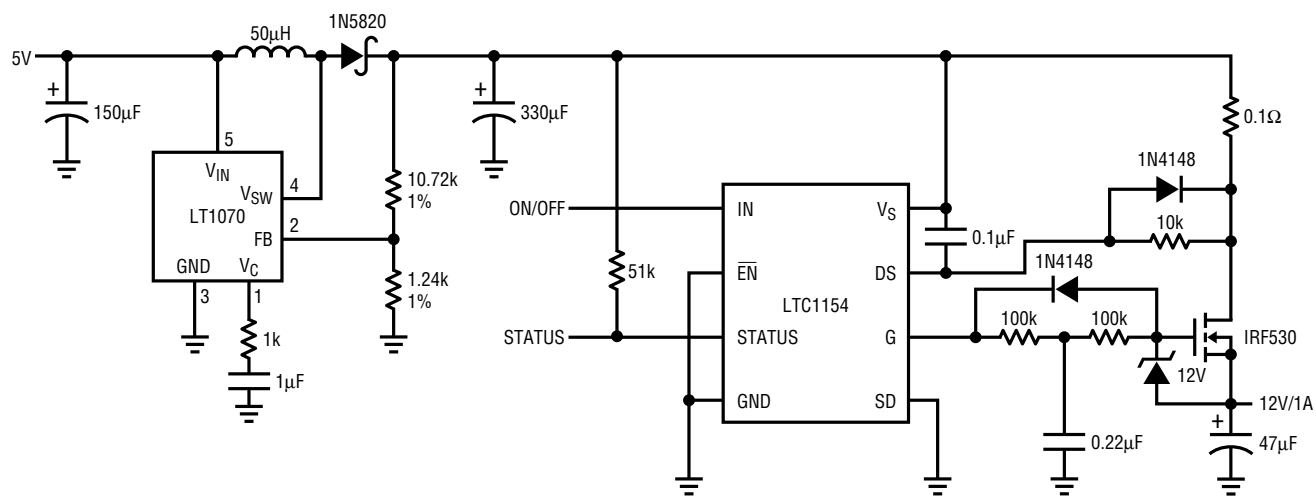
TYPICAL APPLICATIONS

**12V Step-Up Regulator with Ultra-Low Standby Current,
Over-Current Protection and Status Feedback**



LTC1154 • TA11

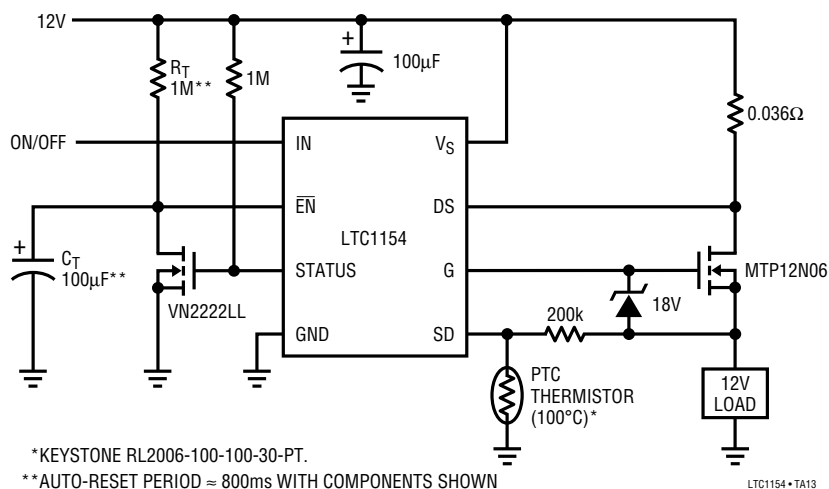
**12V Step-Up Regulator with 1A Over-Current Protection,
Switch Status Feedback and Ramped Output**



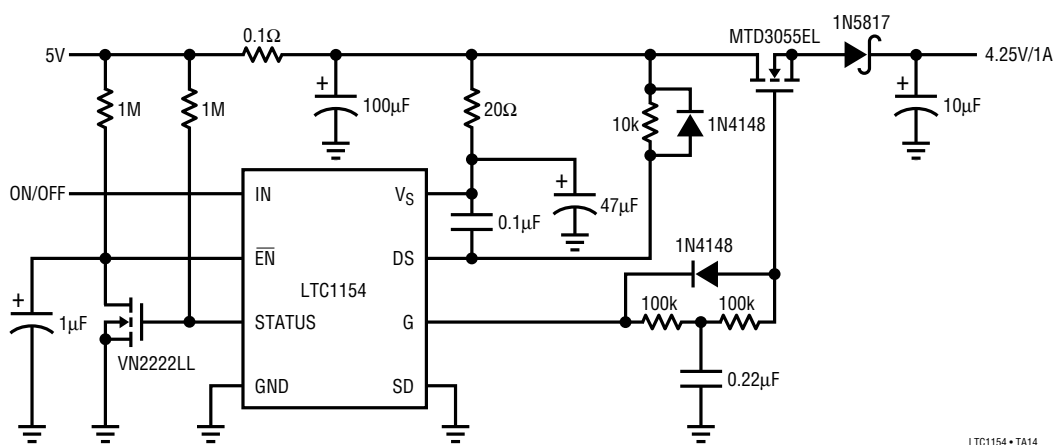
LTC1154 • TA12

TYPICAL APPLICATIONS

Auto-Reset High-Side Switch with Over-Current and Over-Temperature Shutdown

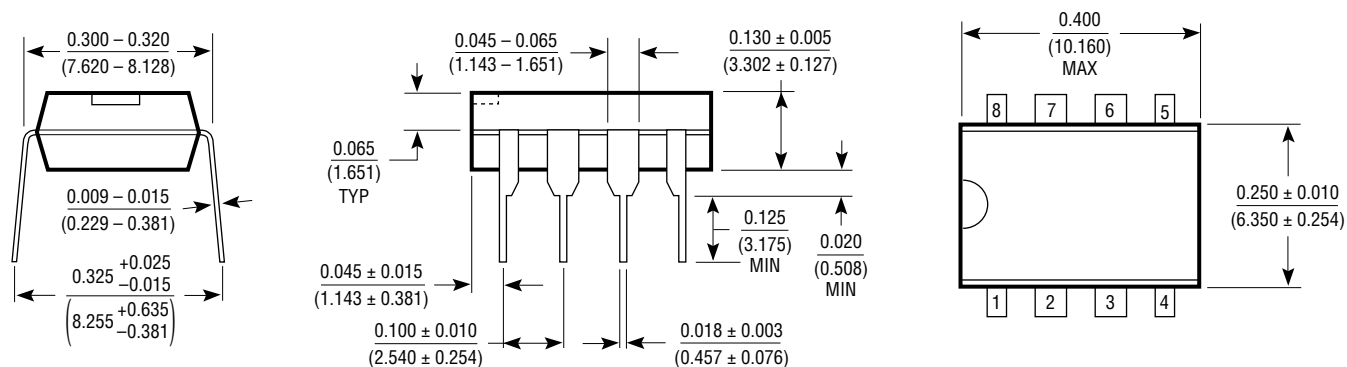


SCSI Termination Power Switch with 1A Over-Current Shutdown, Auto-Reset and Load Soft-Start



PACKAGE DESCRIPTION

N8 Package
8-Lead Plastic Lead



S8 Package
8-Lead Plastic SOIC

