

# Quad 12-Bit Rail-to-Rail Micropower DACs

## FEATURES

- Quad 12-Bit DAC
- Buffered True Rail-to-Rail Voltage Output
- Maximum DNL Error: 0.5LSB
- 5V Operation,  $I_{CC}$ : 1.1mA Typ (LTC1458)
- 3V Operation,  $I_{CC}$ : 800 $\mu$ A Typ (LTC1458L)
- Internal or External Reference Operation
- Settling Time: 14 $\mu$ s to  $\pm 0.5$ LSB
- Schmitt Trigger On Clock Input Allows Direct Optocoupler Interface
- Power-On Reset and  $\overline{CLR}$  Pin
- SSOP-28 Package
- 3-Wire Cascadable Serial Interface with 250kHz Update Rate
- Low Cost

## APPLICATIONS

- Digital Calibration
- Industrial Process Control
- Automatic Test Equipment
- Low Power Systems


## DESCRIPTION

The LTC<sup>®</sup>1458/LTC1458L are complete single supply, quad rail-to-rail voltage output, 12-bit digital-to-analog converters (DACs) in SO-28 and SSOP-28 packages. They include an output buffer amplifier with variable gain ( $\times 1$  or  $\times 2$ ) and an easy-to-use 3-wire cascadable serial interface.

The LTC1458 has an onboard reference of 2.048V and a full-scale output of 4.095V in a  $\times 2$  gain configuration. It operates from a single 4.5V to 5.5V supply dissipating only 5.5mW ( $I_{CC} = 1.1$ mA typ).

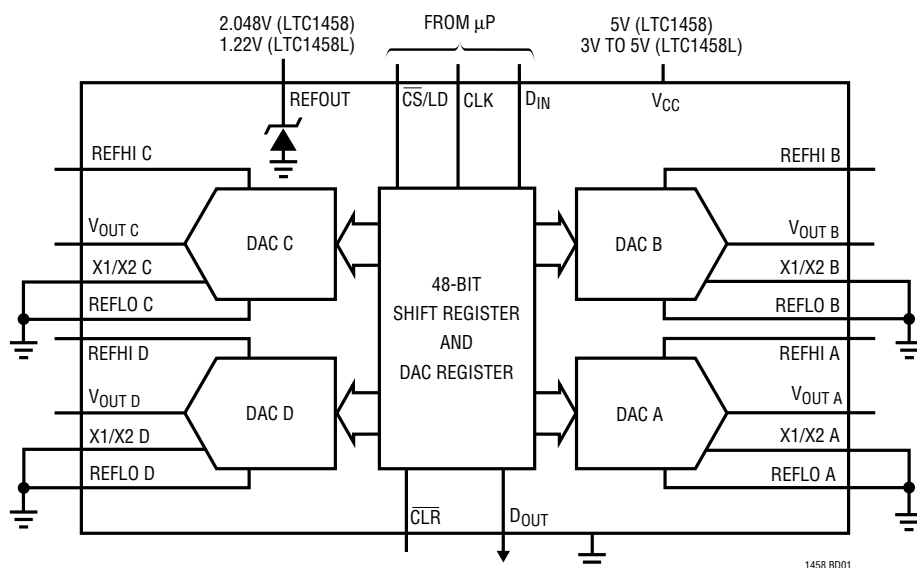
The LTC1458L has an onboard 1.22V reference and a full-scale output of 2.5V in a  $\times 2$  gain configuration. It operates from a single supply of 2.7V to 5.5V dissipating 2.4mW.

Excellent DNL, low supply current and a wide range of built-in functions allow these parts to be used in a host of applications when flexibility, power and single supply operation are important.

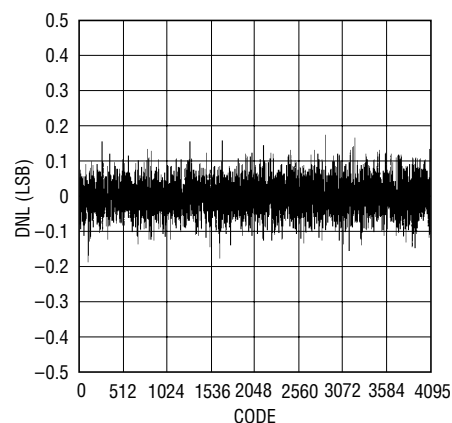
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## TYPICAL APPLICATION

Functional Block Diagram: Quad 12-Bit Rail-to-Rail DAC



Differential Nonlinearity vs Input Code



1458 G09

# LTC1458/LTC1458L

## ABSOLUTE MAXIMUM RATINGS

(Note 1)

$V_{CC}$ to GND .....	–0.5V to 7.5V
Logic Inputs to GND .....	–0.5V to 7.5V
$V_{OUT A}$ , $V_{OUT B}$ , $V_{OUT C}$ , $V_{OUT D}$ , X1/X2 A, X1/X2 B, X1/X2 C, X1/X2 D .....	–0.5V to $V_{CC} + 0.5V$
REFHI A, REFHI B, REFHI C, REFHI D, REFLO A, REFLO B, REFLO C, REFLO D .....	–0.5V to $V_{CC} + 0.5V$
Maximum Junction Temperature .....	125°C
Operating Temperature Range	
LTC1458C/LTC1458LC .....	0°C to 70°C
LTC1458I/LTC1458LI .....	–40°C to 85°C
Storage Temperature Range .....	–65°C to 150°C
Lead Temperature (Soldering, 10 sec) .....	300°C

## PACKAGE/ORDER INFORMATION

<p>TOP VIEW</p> <p>G PACKAGE 28-LEAD PLASTIC SSOP</p> <p>SW PACKAGE 28-LEAD PLASTIC SO</p> <p><math>T_{JMAX} = 125^{\circ}C</math>, <math>\theta_{JA} = 100^{\circ}C/W</math> (G)  <math>T_{JMAX} = 125^{\circ}C</math>, <math>\theta_{JA} = 150^{\circ}C/W</math> (SW)</p>		<p>ORDER PART NUMBER</p> <p>LTC1458CG LTC1458CSW LTC1458LCG LTC1458LCSW LTC1458IG LTC1458ISW LTC1458LIG LTC1458LISW</p>
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Consult factory for Military grade parts.

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = T_{MIN}$  to  $T_{MAX}$ .  $V_{CC} = 4.5V$  to  $5.5V$  (LTC1458),  $2.7V$  to  $5.5V$  (LTC1458L), X1/X2 = REFLO = GND, REFHI = REFOUT,  $V_{OUT}$  unloaded, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DAC</b>						
	Resolution	●	12			Bits
DNL	Differential Nonlinearity	Guaranteed Monotonic (Note 2) ●			±0.5	LSB
INL	Integral Nonlinearity	$T_A = 25^{\circ}C$ (Note 2) ●		±1.75 ±2.25	±4.0 ±4.5	LSB LSB
$V_{OS}$	Offset Error	$T_A = 25^{\circ}C$ ●		±3.0 ±6.0	±12 ±18	mV mV
$V_{OS}TC$	Offset Error Temperature Coefficient			±15		μV/°C
$V_{FS}$	Full-Scale Voltage	When Using Internal Reference, LTC1458, $T_A = 25^{\circ}C$ LTC1458 ●	4.065 4.045	4.095 4.095	4.125 4.145	V V
		When Using Internal Reference, LTC1458L, $T_A = 25^{\circ}C$ LTC1458L ●	2.470 2.460	2.500 2.500	2.530 2.540	V V
$V_{FS}TC$	Full-Scale Voltage Temperature Coefficient	When Using Internal Reference		±24		ppm/°C
<b>Reference</b>						
	Reference Output Voltage	LTC1458 ●	2.008 1.195	2.048 1.220	2.088 1.245	V V
		LTC1458L				
	Reference Output Temperature Coefficient			±20		ppm/°C
	Reference Line Regulation	●		0.7	±2.0	LSB/V
	Reference Load Regulation	0 ≤ $I_{OUT}$ ≤ 100μA, LTC1458 ●		0.2	1.5	LSB
		LTC1458L ●		0.6	3.0	LSB
	Reference Input Range	$V_{REFHI} \leq V_{CC} - 1.5V$		$V_{CC}/2$		V
	Reference Input Resistance	●	15	24	40	kΩ

**ELECTRICAL CHARACTERISTICS**

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = T_{MIN}$  to  $T_{MAX}$ .  $V_{CC} = 4.5V$  to  $5.5V$  (LTC1458),  $2.7V$  to  $5.5V$  (LTC1458L),  $X1/X2 = REFO = GND$ ,  $REFHI = REFOUT$ ,  $V_{OUT}$  unloaded, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Reference Input Capacitance			15		pF
	Short-Circuit Current	REFOUT Shorted to GND	●	45	120	mA

**Power Supply**

$V_{CC}$	Positive Supply Voltage	For Specified Performance, LTC1458 LTC1458L	●	4.5 2.7	5.5 5.5	V V
$I_{CC}$	Supply Current	$4.5V \leq V_{CC} \leq 5.5V$ (Note 5), LTC1458 $2.7V \leq V_{CC} \leq 5.5V$ (Note 5), LTC1458L	●	1100 800	2400 2000	$\mu A$ $\mu A$

**Op Amp DC Performance**

	Short-Circuit Current Low	$V_{OUT}$ Shorted to GND	●	60	120	mA
	Short-Circuit Current High	$V_{OUT}$ Shorted to $V_{CC}$	●	70	120	mA
	Output Impedance to GND	Input Code = 0	●	40	160	$\Omega$

**AC Performance**

	Voltage Output Slew Rate	(Note 3)	●	0.5	1.0	V/ $\mu s$
	Voltage Output Settling Time	(Notes 3, 4) to $\pm 0.5LSB$		14		$\mu s$
	Digital Feedthrough			0.3		nV•s
	AC Feedthrough	REFHI = 1kHz, 2V <sub>p-p</sub> , (Code: All 0s)		-95		dB
SINAD	Signal-to-Noise + Distortion	REFHI = 1kHz, 2V <sub>p-p</sub> , (Code: All 1s)		85		dB

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = T_{MIN}$  to  $T_{MAX}$ .  $V_{CC} = 5V$  (LTC1458),  $3V$  (LTC1458L), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LTC1458			LTC1458L			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IH}$	Digital Input High Voltage		●	2.4		2.0			V
$V_{IL}$	Digital Input Low Voltage		●		0.8			0.6	V
$V_{OH}$	Digital Output High Voltage	$I_{OUT} = -1mA$	●	$V_{CC} - 1.0$		$V_{CC} - 0.7$			V
$V_{OL}$	Digital Output Low Voltage	$I_{OUT} = 1mA$	●		0.4			0.4	V
$I_{LEAK}$	Digital Input Leakage	$V_{IN} = GND$ to $V_{CC}$	●		$\pm 10$			$\pm 10$	$\mu A$
$C_{IN}$	Digital Input Capacitance	Guaranteed by Design, Not Subject to Test	●		10			10	pF

**Switching**

$t_1$	$D_{IN}$ Valid to CLK Setup		●	40		60			ns
$t_2$	$D_{IN}$ Valid to CLK Hold		●	0		0			ns
$t_3$	CLK High Time		●	40		60			ns
$t_4$	CLK Low Time		●	40		60			ns
$t_5$	$\overline{CS}/LD$ Pulse Width		●	50		80			ns
$t_6$	LSB CLK to $\overline{CS}/LD$		●	40		60			ns
$t_7$	$\overline{CS}/LD$ Low to CLK		●	20		30			ns
$t_8$	$D_{OUT}$ Output Delay	$C_{LOAD} = 15pF$	●		150			220	ns
$t_9$	CLK Low to $\overline{CS}/LD$ Low		●	20		30			ns

## ELECTRICAL CHARACTERISTICS

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** Nonlinearity is defined from the first code that is greater than or equal to the maximum offset specification to code 4095 (full scale).

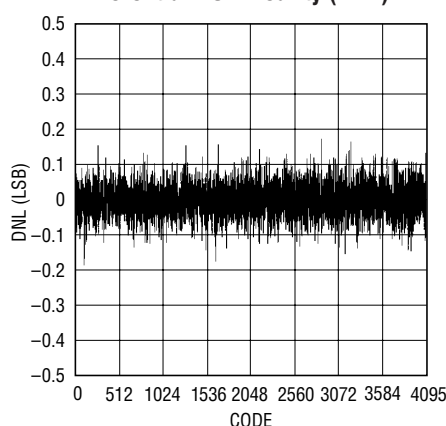
**Note 3:** Load is 5k $\Omega$  in parallel with 100pF.

**Note 4:** DAC switched between all 1s and the code corresponding to  $V_{OS}$  for the part.

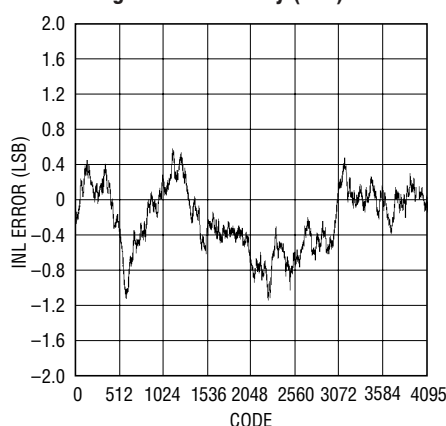
**Note 5:** Digital inputs at 0V or  $V_{CC}$ .

## TYPICAL PERFORMANCE CHARACTERISTICS

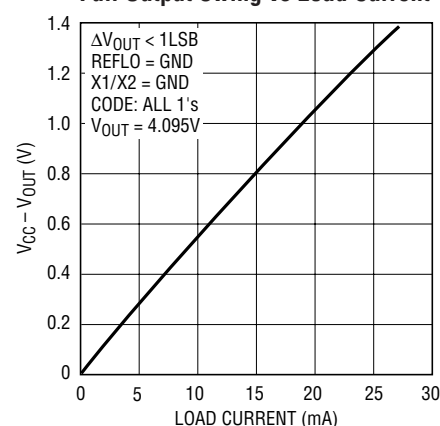
**LTC1458**  
Differential Nonlinearity (DNL)



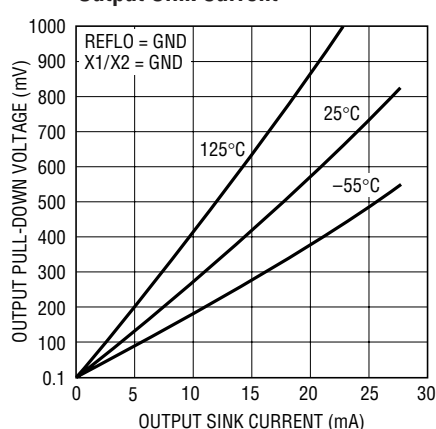
**LTC1458**  
Integral Nonlinearity (INL)



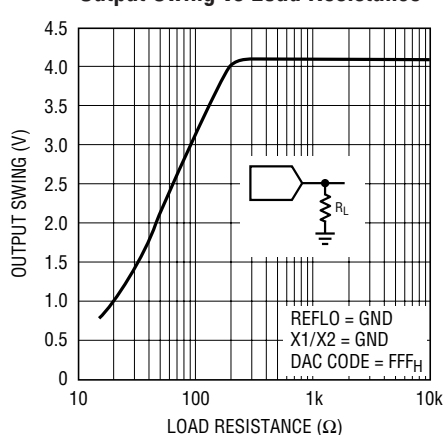
**Minimum Supply Headroom for Full Output Swing vs Load Current**



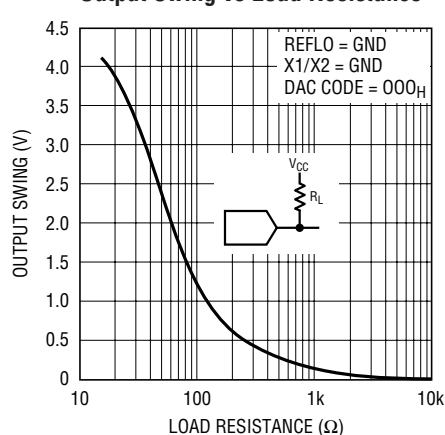
**Minimum Output Voltage vs Output Sink Current**



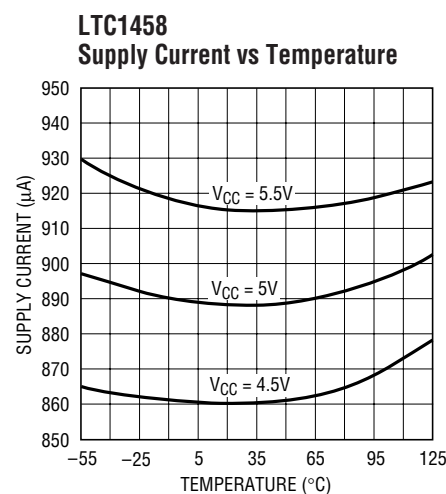
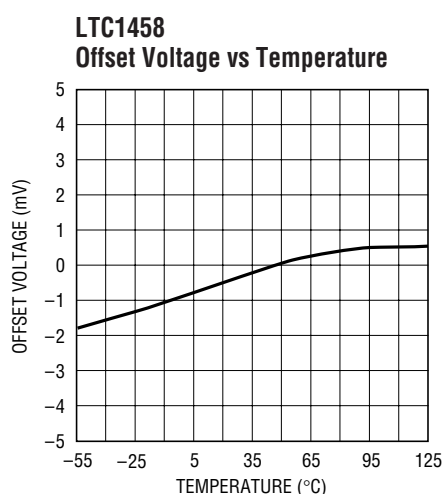
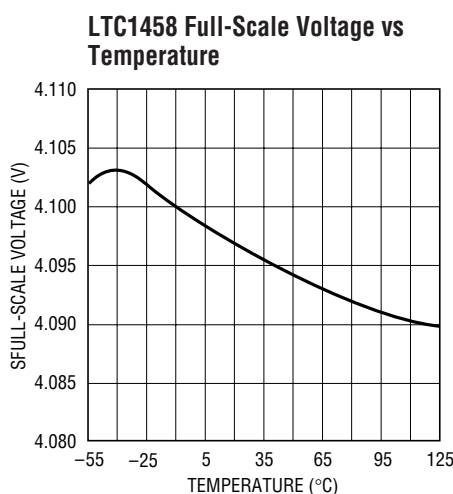
**Output Swing vs Load Resistance**



**Output Swing vs Load Resistance**



## TYPICAL PERFORMANCE CHARACTERISTICS



## PIN FUNCTIONS

**X1/X2 C, X1/X2 D, X1/X2 A, X1/X2 B (Pins 1, 14, 16, 27):** The Input Pin that Sets the Gain for DAC C/D/A/B. When grounded the gain will be 2, i.e., output full-scale will be 2 • REFHI. When connected to V<sub>OUT</sub> the gain will be 1, i.e., output full-scale will be equal to REFHI.

**V<sub>OUT C</sub>, V<sub>OUT D</sub>, V<sub>OUT A</sub>, V<sub>OUT B</sub> (Pins 2, 13, 17, 26):** The Buffered DAC Outputs.

**CS/LD (Pin 3):** The Serial Interface Enable and Load Control Input.

**D<sub>IN</sub> (Pin 4):** The Serial Data Input.

**REFHI C, REFHI D, REFHI A, REFHI B, (Pins 5, 9, 20, 24):** The Inputs to the DAC Resistor Ladder for DAC C/D/A/B.

**GND (Pins 6, 23):** Ground.

**REFLO C, REFLO D, REFLO A, REFLO B, (Pins 7, 8, 21, 22):** The Bottom of the DAC Resistor Ladders for the DACs. These can be used to offset zero-scale above ground. REFLO should be connected to ground when no offset is required.

**D<sub>OUT</sub> (Pin 10):** The Output of the Shift Register which Becomes Valid on the Rising Edge of the Serial Clock.

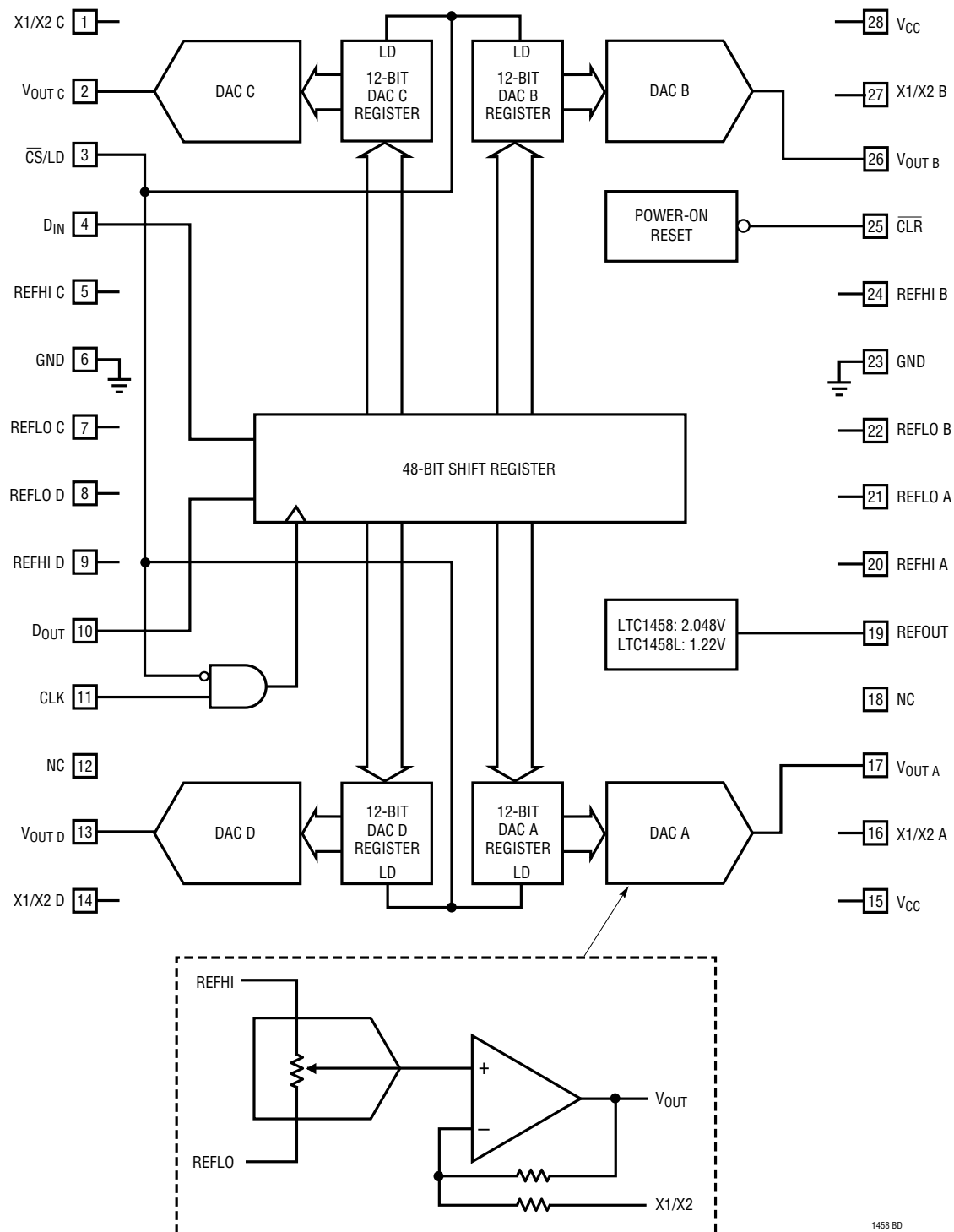
**CLK (Pin 11):** The Serial Interface Clock Input.

**V<sub>CC</sub> (Pins 15, 28):** The Positive Supply Input. 4.5V ≤ V<sub>CC</sub> ≤ 5.5V (LTC1458), 2.7V ≤ V<sub>CC</sub> ≤ 5.5V (LTC1458L). Requires a 0.1µF bypass capacitor to ground.

**REFOUT (Pin 19):** The Output of the Internal Reference.

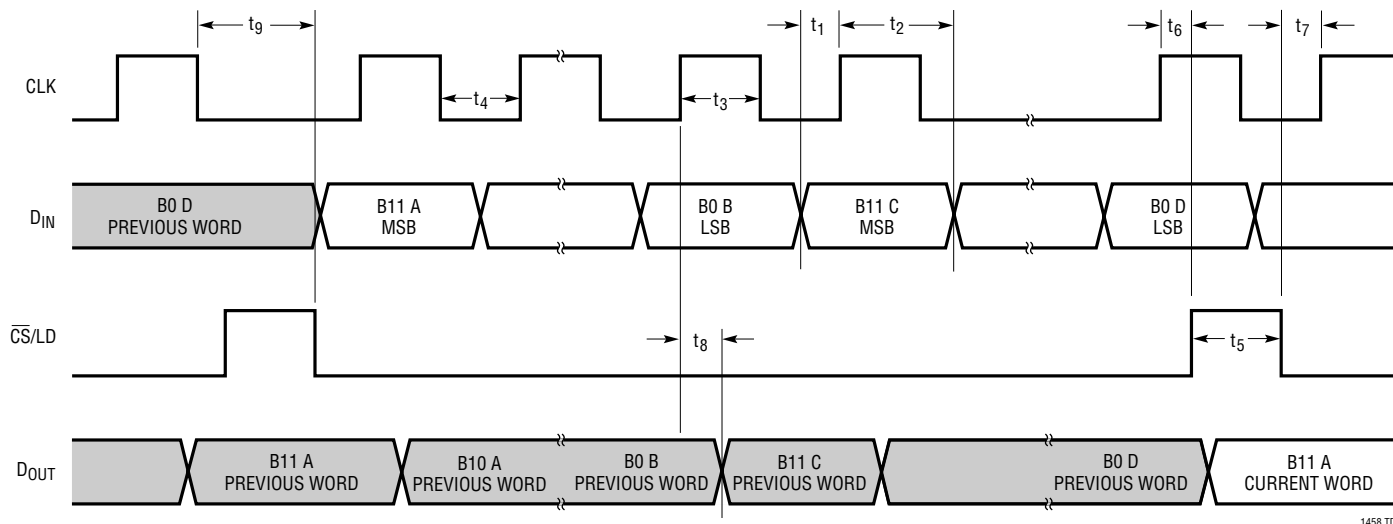
**CLR (Pin 25):** The Clear Pin. Clears all DACs to zero-scale when pulled low.

BLOCK DIAGRAM



1458 BD

## TIMING DIAGRAM



## DEFINITIONS

**Resolution (n):** Resolution is defined as the number of digital input bits, n. It defines the number of DAC output states ( $2^n$ ) that divide the full-scale range. The resolution does not imply linearity.

**Full-Scale Voltage ( $V_{FS}$ ):** This is the output of the DAC when all bits are set to 1.

**Voltage Offset Error ( $V_{OS}$ ):** The theoretical voltage at the output when the DAC is loaded with all zeros. The output amplifier can have a true negative offset, but because the part is operated from a single supply, the output cannot go below zero. If the offset is negative, the output will remain near 0V resulting in the transfer curve shown in Figure 1.

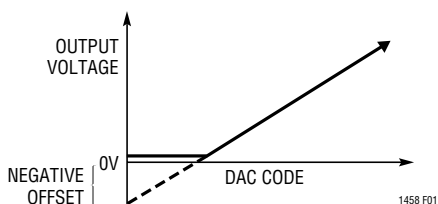


Figure 1. Effect of Negative Offset

The offset of the part is measured at the code that corresponds to the maximum offset specification:

$$V_{OS} = V_{OUT} - [(Code)(V_{FS})/(2^n - 1)]$$

**Least Significant Bit (LSB):** One LSB is the ideal voltage difference between two successive codes.

$$LSB = (V_{FS} - V_{OS})/(2^n - 1) = (V_{FS} - V_{OS})/4095$$

Nominal LSBs:

LTC1458	$LSB = 4.095V/4095 = 1mV$
LTC1458L	$LSB = 2.5V/4095 = 0.610mV$

**Integral Nonlinearity (INL):** End-point INL is the maximum deviation from a straight line passing through the end-points of the DAC transfer curve. Because the part operates from a single supply and the output cannot go below zero, the linearity is measured between full scale and the code corresponding to the maximum offset specification. The INL error at a given input code is calculated as follows:

$$INL = [V_{OUT} - V_{OS} - (V_{FS} - V_{OS})(code/4095)]/LSB$$

$V_{OUT}$  = The output voltage of the DAC measured at the given input code

## DEFINITIONS

**Differential Nonlinearity (DNL):** DNL is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. The DNL error between any two codes is calculated as follows:

$$\text{DNL} = (\Delta V_{\text{OUT}} - \text{LSB}) / \text{LSB}$$

$\Delta V_{\text{OUT}}$  = The measured voltage difference between two adjacent codes

**Digital Feedthrough:** The glitch that appears at the analog output caused by AC coupling from the digital inputs when they change state. The area of the glitch is specified in (nV)(sec).

## OPERATION

### Serial Interface

The data on the  $D_{\text{IN}}$  input is loaded into the shift register on the rising edge of the clock. Data is loaded as one 48-bit word, DAC A first, then DAC B, DAC C and DAC D. The MSB is loaded first for each DAC. The DAC registers load the data from the shift register when  $\overline{\text{CS}}/\text{LD}$  is pulled high. The CLK is disabled internally when  $\overline{\text{CS}}/\text{LD}$  is high. Note: CLK must be low before  $\overline{\text{CS}}/\text{LD}$  is pulled low to avoid an extra internal clock pulse.

The buffered output of the 48-bit shift register is available on the  $D_{\text{OUT}}$  pin which swings from ground to  $V_{\text{CC}}$ .

Multiple LTC1458/LTC1458Ls may be daisy-chained together by connecting the  $D_{\text{OUT}}$  pin to the  $D_{\text{IN}}$  pin of the next chip, while the CLK and  $\overline{\text{CS}}/\text{LD}$  signals remain common to all chips in the daisy-chain. The serial data is clocked to all of the chips, then the  $\overline{\text{CS}}/\text{LD}$  signal is pulled high to update all of them simultaneously.

### Reference

The LTC1458L has an internal reference of 1.22V with a full scale of 2.5V (gain of 2 configuration). The LTC1458 includes an internal 2.048V reference, making 1LSB equal to 1mV (gain of 2 configuration). When the buffer gain is 2, the external reference must be less than  $V_{\text{CC}}/2$  and be capable of driving the 15k minimum DAC resistor ladder. The external reference must always be less than  $V_{\text{CC}} - 1.5\text{V}$ . The reference output voltage noise spectral density at 1kHz is  $300\text{nV}/\sqrt{\text{Hz}}$ .

### Voltage Output

The rail-to-rail buffered output of the LTC1458 family can source or sink 5mA when operating with a 5V supply over the entire operating temperature range while pulling to within 300mV of the positive supply voltage or ground. The output swings to within a few millivolts of either supply rail when unloaded and has an equivalent output resistance of  $40\Omega$  when driving a load to the rails. The output can drive 1000pF without going into oscillation. The output voltage noise spectral density at 1kHz is  $600\text{nV}/\sqrt{\text{Hz}}$ .



## APPLICATIONS INFORMATION

### Using Two DACs to Digitally Program the Full Scale and Offset of a Third

Figure 2 shows how to use one LTC1458 to make a 12-bit DAC with a digitally programmable full scale and offset. DAC A and DAC B are used to control the offset and full scale of DAC C. DAC A is connected in a  $\times 1$  configuration and controls the offset of DAC C by moving REFLO C above ground. The minimum value to which this offset can be programmed is 10mV. DAC B is connected in a  $\times 2$  configuration and controls the full scale of DAC C by driving REFHI C. Note that the voltage at REFHI C must be less than or equal to  $V_{CC}/2$ , corresponding to DAC B's code

$\leq 2,500$  for  $V_{CC} = 5V$ , since DAC C is being operated in  $\times 2$  mode for full rail-to-rail output swing.

The transfer characteristic is:

$$V_{OUTC} = 2 \cdot [D_C \cdot (2 \cdot D_B - D_A) + D_A] \cdot REFOUT$$

where REFOUT = The Reference Output

$D_A = (\text{DAC A Digital Code})/4096$   
This sets the offset.

$D_B = (\text{DAC B Digital Code})/4096$   
This sets the full scale.

$D_C = (\text{DAC C Digital Code})/4096$

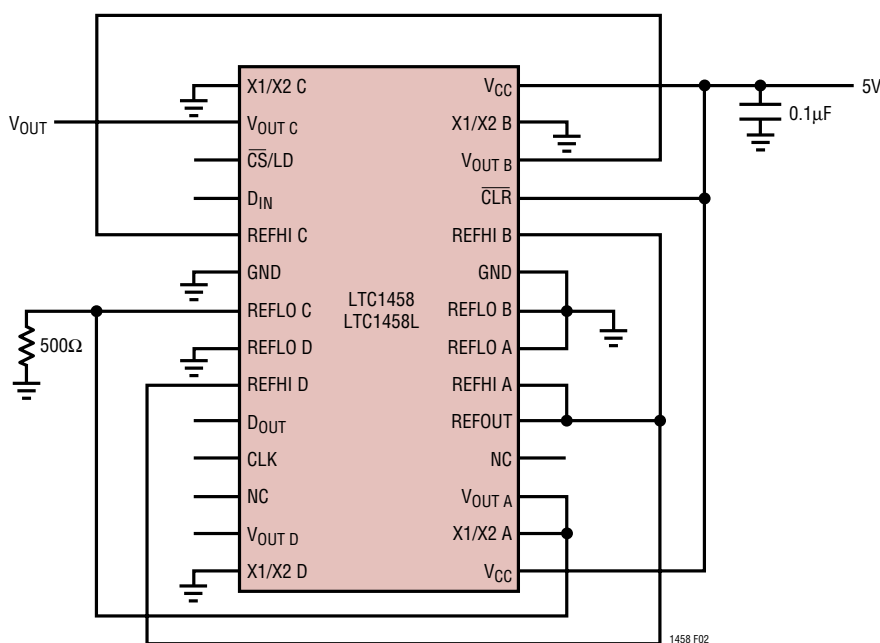
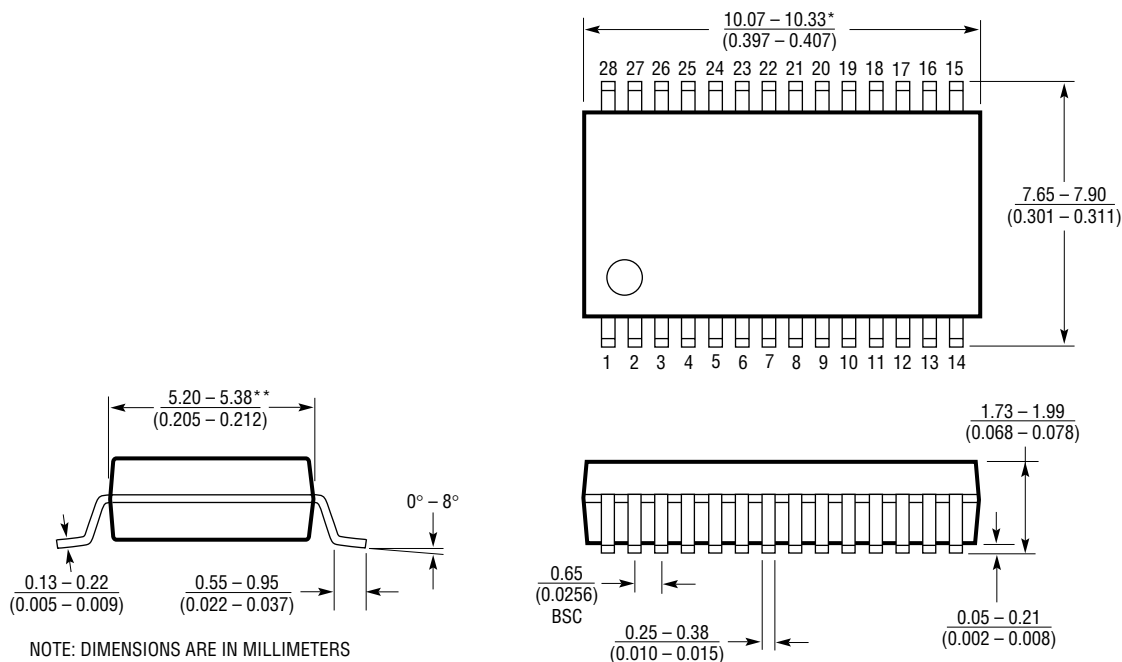


Figure 2

# PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

## G Package 28-Lead Plastic SSOP (0.209) (LTC DWG # 05-08-1640)



NOTE: DIMENSIONS ARE IN MILLIMETERS

\*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.152mm (0.006") PER SIDE

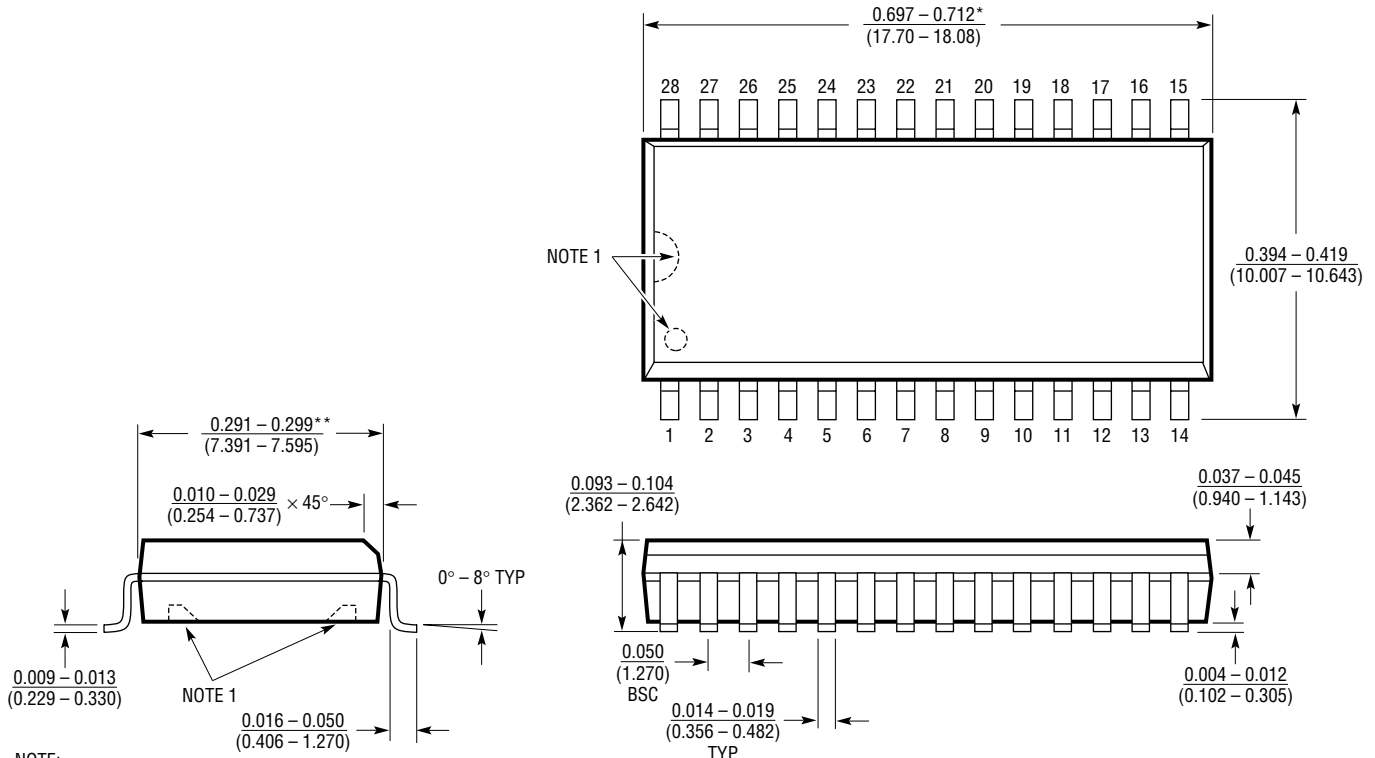
\*\*DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.254mm (0.010") PER SIDE

G28 SSOP 1098

# PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

## SW Package 28-Lead Plastic Small Outline (Wide 0.300) (LTC DWG # 05-08-1620)



## NOTE:

1. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS.  
THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS

\*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

\*\*DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S28 (WIDE) 1098

