

Low Glitch 16-Bit Voltage Output DAC

FEATURES

- **16-Bit Monotonic Over Temperature**
- **Low Glitch Impulse: 2nV-s**
- **Low Noise: 30nV/√Hz**
- **Buffered Rail-to-Rail Voltage Output**
- Low Power: 50mW from $\pm 5V$ Supplies
- Unipolar or Bipolar Output (0V to V_{REF} or $\pm V_{REF}$)
- 4-Quadrant Multiplying Capability
- Asynchronous Clear to User-Defined Voltage
- Power-On Reset
- Three-Wire SPI and MICROWIRE™ Compatible Serial Interface
- Schmitt Trigger On CLK Input Allows Direct Optocoupler Interface
- 16-Pin Narrow SO Package

APPLICATIONS

- Industrial Process Control
- Precision Industrial Equipment
- Waveform Generation
- Automatic Test Equipment
- High Resolution Offset and Gain Adjustment

DESCRIPTION

The LTC[®]1650 is a deglitched rail-to-rail voltage output 16-bit digital-to-analog converter (DAC) available in a 16-pin narrow SO package. It has 16-bit monotonicity over temperature and includes a rail-to-rail output buffer amplifier and an easy to use three-wire cascadable serial interface. The LTC1650 operates with dual $\pm 5V$ supplies.

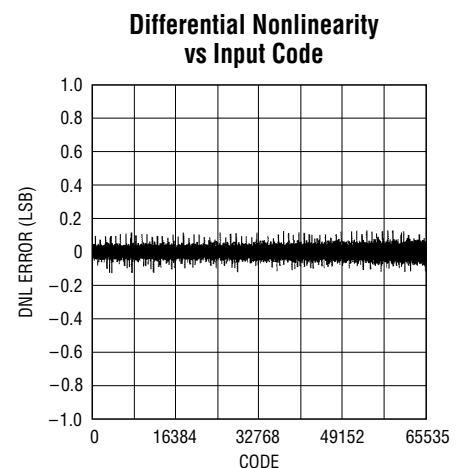
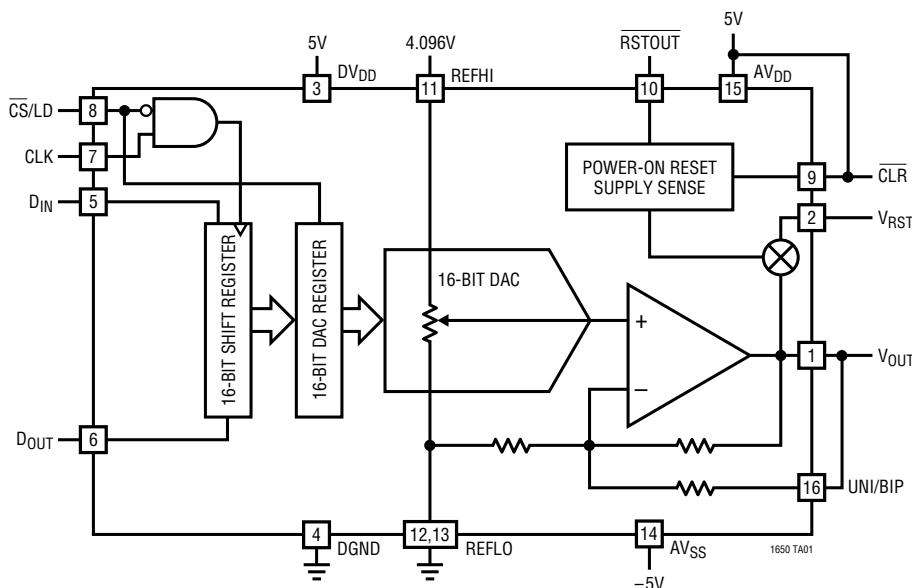
With $REFLO = 0V$ and $REFHI = V_{REF}$, the output will swing from 0V to V_{REF} in unipolar mode or $\pm V_{REF}$ in bipolar mode.

The LTC1650 has excellent accuracy over its full operating temperature range along with very low power dissipation of 50mW with dual $\pm 5V$ supplies. This, along with the small outline package, makes it the most flexible high resolution digital-to-analog converter available today.

The LTC1650 has a fast settling time of 4 μ s to 16 bits and a low midscale glitch of under 2nV-s. This makes the LTC1650 ideal for waveform generation or other applications where output dynamic performance is important.

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TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS

(Note 1)

AV_{DD} , DV_{DD} to DGND	–0.5V to 7.5V
TTL Input Voltage	–0.5V to 7.5V
V_{OUT} , V_{RST}	–0.5V to (AV_{DD} + 0.5V)
AV_{SS}	0.5V to –7.5V
Operating Temperature Range	
LTC1650C	0°C to 70°C
LTC1650I	–40°C to 85°C
Maximum Junction Temperature	125°C
Storage Temperature Range	–65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

PACKAGE/ORDER INFORMATION

TOP VIEW		ORDER PART NUMBER
V_{OUT} [1]	[16] UNI/BIP	LTC1650ACN LTC1650AIN LTC1650ACS LTC1650AIS LTC1650CN LTC1650IN LTC1650CS LTC1650IS
V_{RST} [2]	[15] AV_{DD}	
DV_{DD} [3]	[14] AV_{SS}	
DGND [4]	[13] REFLO S	
D_{IN} [5]	[12] REFLO F	
D_{OUT} [6]	[11] REFHI	
CLK [7]	[10] \overline{RSTOUT}	
$\overline{CS/LD}$ [8]	[9] \overline{CLR}	
<div><div>N PACKAGE</div><div>16-LEAD PDIP</div></div> <div><div>S PACKAGE</div><div>16-LEAD PLASTIC SO</div></div>		
<div>$T_{JMAX} = 125^{\circ}\text{C}, \theta_{JA} = 85^{\circ}\text{C/W (N)}$</div> <div>$T_{JMAX} = 125^{\circ}\text{C}, \theta_{JA} = 130^{\circ}\text{C/W (S)}$</div>		

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

$AV_{DD} = 4.75\text{V}$ to 5.25V , $AV_{SS} = -4.75\text{V}$ to -5.25V , $DV_{DD} = 4.75\text{V}$ to 5.25V , REFLO = 0V, REFHI = 4.096V, V_{OUT} unloaded,
 $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LTC1650CS/CN LTC1650IS/IN			LTC1650ACS/ACN LTC1650AIS/AIN			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
DAC Characteristics, Unipolar/Bipolar Output Unless Otherwise Noted									
	Resolution		●	16		16			Bits
	Monotonicity		●	16		16			Bits
DNL	Differential Nonlinearity	Guaranteed Monotonic (Note 2)	●	±0.15 ±0.9		±0.15 ±0.5			LSB
INL	Integral Nonlinearity	Integral Nonlinearity (Note 2)	●	±4 ±16		±4 ±8			LSB
	Bipolar Zero Error	T _A = 25°C		±5 ±12		±5 ±12			LSB
	Bipolar Zero Error	T _A = T _{MIN} to T _{MAX}	●	±18		±18			LSB
V _{OS}	Unipolar Offset Error	T _A = T _{MIN} to T _{MAX}	●	±0.5 ±12		±0.5 ±12			LSB
V _{OSTC}	Offset Error Temperature Coefficient			±0.5		±0.5			µV/°C
	Gain Error	T _A = T _{MIN} to T _{MAX}	●	±4 ±18		±4 ±12			LSB
	Gain Error Temperature Coefficient			±0.5		±0.5			ppm/°C
	Bipolar Negative Full-Scale Error	T _A = T _{MIN} to T _{MAX} See Definitions Section	●	±1 ±16		±1 ±12			LSB
	Bipolar Negative Full-Scale Error Tempco	See Definitions Section		±0.75		±0.75			ppm/°C

ELECTRICAL CHARACTERISTICS

$AV_{DD} = 4.75V$ to $5.25V$, $AV_{SS} = -4.75V$ to $-5.25V$, $DV_{DD} = 4.75V$ to $5.25V$, $REFLO = 0V$, $REFHI = 4.096V$, V_{OUT} unloaded, $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply Characteristics							
AV_{DD}	Positive Supply Voltage		●	4.75	5.0	5.25	V
DV_{DD}	Positive Supply Voltage		●	4.75	5.0	5.25	V
AV_{SS}	Negative Supply Voltage		●	-4.75	-5.0	-5.25	V
I_{AVDD}	AV_{DD} Supply Current	$4.75V \leq AV_{DD} \leq 5.25V$ (Note 5)	●		5	7.5	mA
I_{AVSS}	AV_{SS} Supply Current	$-5.25V \leq AV_{SS} \leq -4.75V$ (Note 5)	●	-7.5	-5		mA
I_{DVDD}	DV_{DD} Supply Current	$4.75V \leq DV_{DD} \leq 5.25V$ (Note 5)	●		0.1	0.25	mA
PSRR	AV_{DD} , DV_{DD} Supply Rejection	$4.75V \leq AV_{DD}$, $DV_{DD} \leq 5.25V$	●		0.5	1.5	LSB/V
	AV_{SS} Supply Rejection	$-5.25V \leq AV_{SS} \leq -4.75V$	●		0.5	1.5	LSB/V
Reference Input							
R_{IN}	Reference Input Resistance		●	2.5	5	7.5	k Ω
	REFHI Range		●	-4.0	4.0	4.5	V
	REFLO Range		●	-1.0	0	1.0	V
Op Amp DC Performance							
	Short-Circuit Current Low	V_{OUT} Shorted to GND	●		25	50	mA
	Short-Circuit Current High	V_{OUT} Shorted to V_{CC}	●		25	50	mA
	Output Impedance	Measured at Midscale			0.15		Ω
	DAC Output Range	Unipolar Mode (Note 9) Bipolar Mode (Note 9)			0V to V_{REF} $\pm V_{REF}$		V V
AC Performance							
	Voltage Output Slew Rate		●	0.8	2.0		V/ μ s
	Voltage Output Settling Time	Unloaded (Note 4)			4		μ s
	Midscale Glitch Impulse				1.8		nV-s
	Digital Feedthrough				0.05		nV-s
	Output Noise Voltage Density	1kHz to 100kHz (Note 6)			30		nV/ \sqrt{Hz}
SINAD	Signal-to-Noise + Distortion Ratio	REFHI = 1kHz 4V _{P-P}			96		dB

ELECTRICAL CHARACTERISTICS

$AV_{DD} = 4.75V$ to $5.25V$, $AV_{SS} = -4.75V$ to $-5.25V$, $DV_{DD} = 4.75V$ to $5.25V$, $REFLO = 0V$, $REFHI = 4.096V$, V_{OUT} unloaded, $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Digital I/O Characteristics							
V _{IH}	Digital Input High Voltage		●	2.4			V
V _{IL}	Digital Input Low Voltage		●			0.8	V
V _{OH}	Digital Output High Voltage	I _{OUT} = −1mA, D _{OUT} Only	●	V _{CC} − 1.0			V
V _{OL}	Digital Output Low Voltage	I _{OUT} = 1mA, D _{OUT} Only	●			0.4	V
I _{LK}	Digital Input Leakage	V _{IN} = GND to V _{CC}	●			±10	μA
C _{IN}	Digital Input Capacitance	(Note 3)				10	pF
Reset Characteristics							
R _{ON}	V _{OUT} and V _{RST} Switch Resistance	V _{RST} = 0.5V (Note 7)	●	200		500	Ω
	Threshold Voltage for Reset	AV _{DD} or DV _{DD} (Note 8)	●	1.5	2.5	3.2	V
		AV _{SS} (Note 8)	●	1.5	2.5	3.2	V
Switching Characteristics							
t ₁	D _{IN} Valid to CLK Setup		●	40			ns
t ₂	D _{IN} Valid to CLK Hold		●	0			ns
t ₃	CLK High Time	(Note 3)	●	40			ns
t ₄	CLK Low Time	(Note 3)	●	40			ns
t ₅	\overline{CS}/LD Pulse Width	(Note 3)	●	50			ns
t ₆	LSB CLK to \overline{CS}/LD	(Note 3)	●	40			ns
t ₇	\overline{CS}/LD Low to CLK	(Note 3)	●	20			ns
t ₈	D _{OUT} Output Delay	C _{LOAD} = 100pF	●	5	45	150	ns
t ₉	CLK Low to \overline{CS}/LD Low	(Note 3)	●	20			ns
t ₁₀	CLR Pulse Width		●	50			ns

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Nonlinearity is defined from code 0 to code 65535 (full scale) (end point INL, see Definitions section).

Note 3: Guaranteed by design. Not subject to test.

Note 4: To $\pm 1LSB$. Unipolar mode. DAC switched between all 1s and all 0s.

Note 5: Digital Inputs at 0V or DV_{DD} .

Note 6: Measured at V_{OUT} . $REFHI = REFLO = 0V$, unipolar mode.

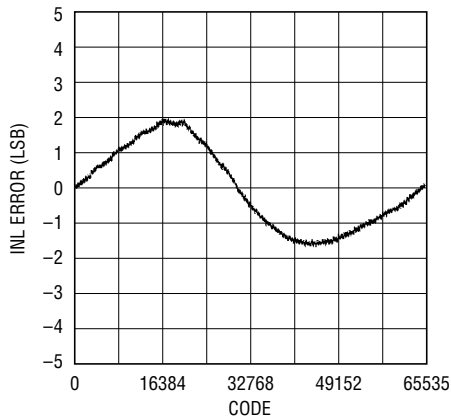
Note 7: When part powers up or when it is reset, the output is connected to V_{RST} through this switch.

Note 8: Reset is active when any supply goes below this threshold.

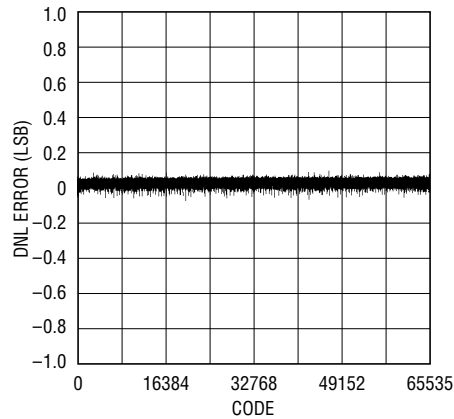
Note 9: $REFLO = 0V$, $REFHI = V_{REF}$. For $REFLO \neq 0V$ see Operation section.

TYPICAL PERFORMANCE CHARACTERISTICS

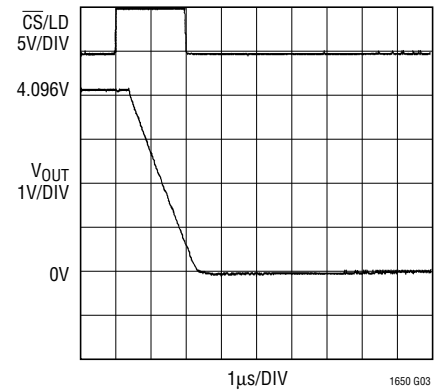
Integral Nonlinearity (INL) vs Input Code



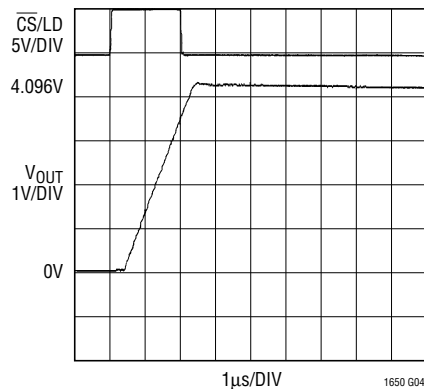
Differential Nonlinearity (DNL) vs Input Code



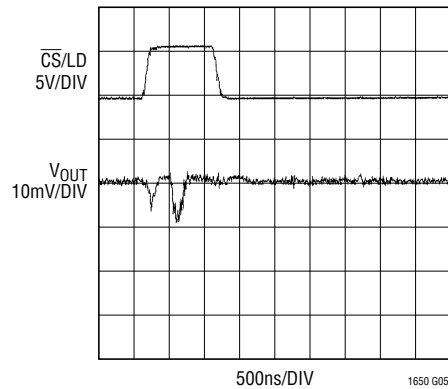
Large Signal Settling Time



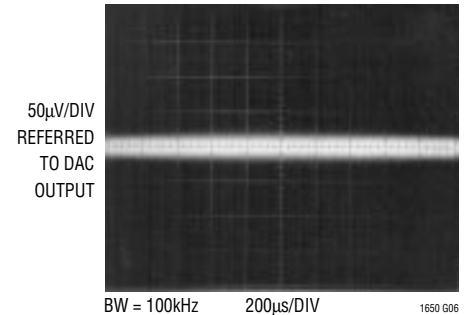
Large Signal Settling Time



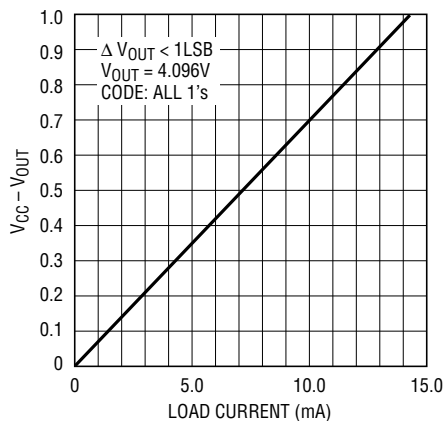
Mid-Scale Glitch



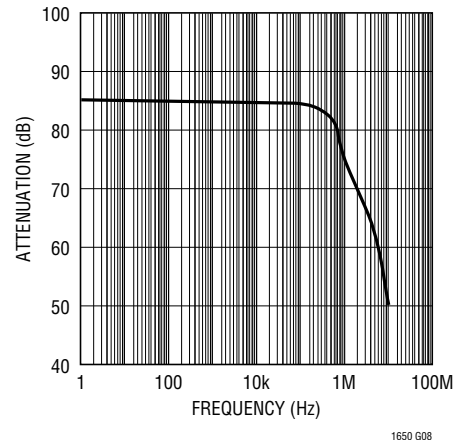
Broadband Noise



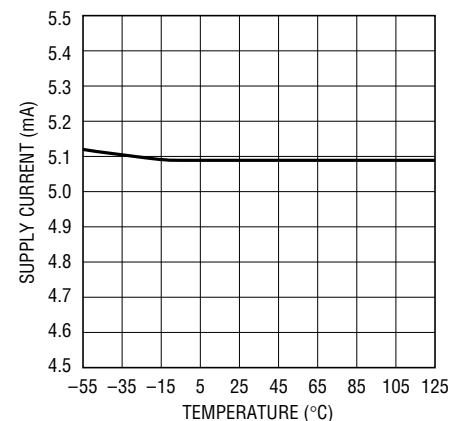
Minimum Supply Headroom for Full Output Swing vs Load Current



Reference Feedthrough

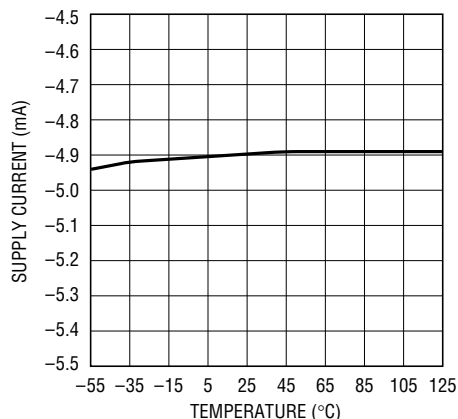


AV_{DD} Supply Current vs Temperature



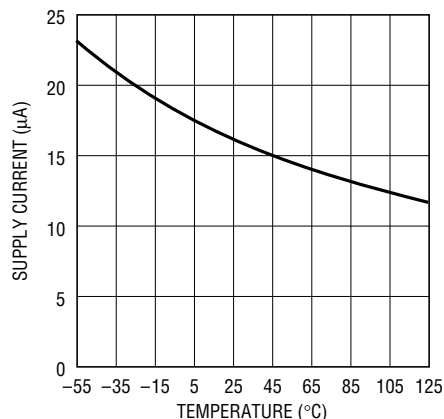
TYPICAL PERFORMANCE CHARACTERISTICS

AV_{SS} Supply Current vs Temperature



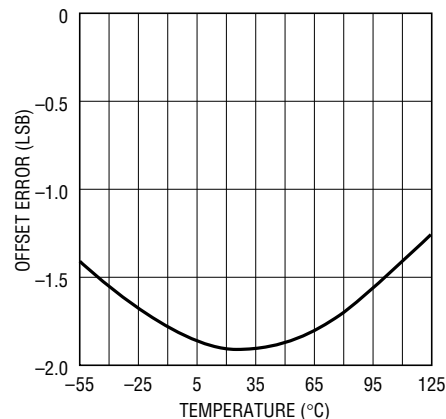
1650 G10

DV_{DD} Supply Current vs Temperature



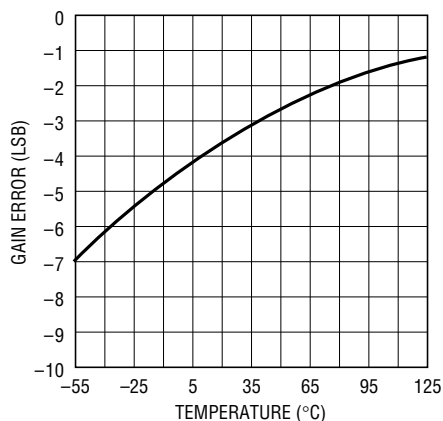
1650 G11

Offset Error vs Temperature



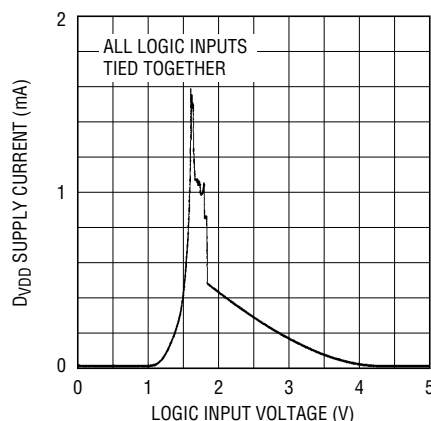
1650 G12

Gain Error vs Temperature



1650 G13

Supply Current vs Logic Input Voltage



1650 G14

PIN FUNCTIONS

V_{OUT} (Pin 1): The Rail-to-Rail Deglitched DAC Output. The output will swing from REFLO to REFHI in unipolar mode and from (2 • REFLO – REFHI) to REFHI in bipolar mode.

V_{RST} (Pin 2): The user-defined voltage to which the output gets reset when CLR is active, when any of the supplies drop below 2.5V or when the part powers-up. The output will stay at this voltage until a new code is loaded into the DAC register.

DV_{DD} (Pin 3): The Digital Positive Supply Input. $4.75V \leq DV_{DD} \leq 5.25V$.

DGND (Pin 4): Digital Ground.

D_{IN} (Pin 5): The TTL Level Input for the Serial Interface Data. Data on the D_{IN} pin is latched into the shift register on the rising edge of the serial clock. Data is loaded as one 16-bit word, MSB first.

D_{OUT} (Pin 6): The output of the shift register that becomes valid on the rising edge of the serial clock.

PIN FUNCTIONS

CLK (Pin 7): The TTL Level Input for the Serial Interface Clock.

$\overline{\text{CS/LD}}$ (Pin 8): The TTL Level Input for the Serial Interface Enable and Load Control. When $\overline{\text{CS/LD}}$ is low, the CLK signal is enabled so the data can be clocked in. When $\overline{\text{CS/LD}}$ is pulled high, data is loaded from the shift register into the DAC register, updating the DAC output.

CLR (Pin 9): The DAC is cleared to V_{RST} when this pin is pulled low. It should be logic high for normal operation.

RSTOUT (Pin 10): The logic output pin that goes active when any of the supplies drop below 2.5V. This pin is active low.

REFHI (Pin 11): The Reference Input Pin. The DAC is capable of 4-quadrant multiplying; this pin can swing from 4.5V to -4V .

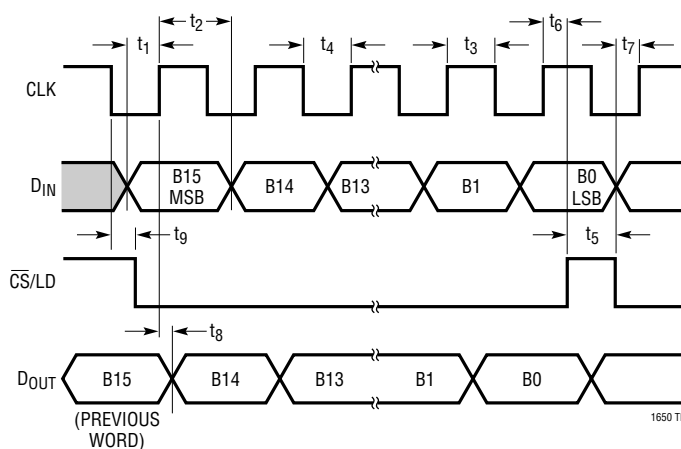
REFLO F/REFLO S (Pins 12, 13): The Force and Sense Pin for the Lower Reference Input. This should nominally be tied to ground. This pin can swing from -1V to 1V .

AV_{SS} (Pin 14): The Analog Negative Supply Input. $-5.25\text{V} \leq \text{AV}_{\text{SS}} \leq -4.75\text{V}$. Requires a bypass capacitor to ground.

AV_{DD} (Pin 15): The Analog Positive Supply Input. $4.75\text{V} \leq \text{AV}_{\text{DD}} \leq 5.25\text{V}$. Requires a bypass capacitor to ground.

UNI/BIP (Pin 16): The Unipolar/Bipolar Selection Pin. For unipolar operation, tie this pin to V_{OUT} and for bipolar operation, tie this pin the REFHI.

TIMING DIAGRAM



DEFINITIONS

Resolution (n)

Resolution is defined as the number of digital input bits, n. It defines the number of DAC output states (2^n) that divide the full-scale range. The resolution does not imply linearity.

Full-Scale Voltage (V_{FS})

This is the output of the DAC when all bits are set to 1. The output will swing from REFLO to REFHI in unipolar mode and from ($2 \cdot \text{REFLO} - \text{REFHI}$) to REFHI when in bipolar mode.

Voltage Offset Error (V_{OS})

This is the voltage at the output when the DAC is loaded with all zeros.

Least Significant Bit (LSB)

One LSB is the ideal voltage difference between two successive codes.

$$\text{LSB} = (V_{FS} - V_{OS}) / (2^n - 1) = (V_{FS} - V_{OS}) / 65535$$

Integral Nonlinearity (INL)

Endpoint INL is the maximum deviation from a straight line passing through the endpoints of the DAC transfer curve. It is measured after adjusting out gain and offset error for the DAC.

Differential Nonlinearity (DNL)

DNL is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. The DNL error between any two codes is calculated as follows:

$$\text{DNL} = (\Delta V_{OUT} - \text{LSB}) / \text{LSB}$$

ΔV_{OUT} = The measured voltage difference between two adjacent codes.

Gain Error (GE)

Gain error is the difference between the full-scale output of a DAC from its ideal full-scale value after offset error has been adjusted for.

Bipolar Zero Error

When configured for bipolar output and with REFLO tied to 0V, the LTC1650 output should be 0V with (100...00) loaded in. Any deviation from 0V at this code is called bipolar zero error.

Bipolar Negative Full-Scale Error

This is the offset error of the LTC1650 in bipolar mode.

OPERATION

Serial Interface

The data on the D_{IN} input is loaded into the shift register on the rising edge of the clock. Data is loaded as one 16-bit word, MSB first. The DAC register loads the data from the shift register when $\overline{CS/LD}$ is pulled high. The clock is disabled internally when $\overline{CS/LD}$ is high. Note: CLK must be low before $\overline{CS/LD}$ is pulled low to avoid an extra internal clock pulse.

The buffered output of the 16-bit shift register is available on the D_{OUT} pin which swings from DGND to DV_{DD} .

Multiple LTC1650s may be daisy-chained together by connecting the D_{OUT} pin to the D_{IN} pin of the next chip while the clock and $\overline{CS/LD}$ signals remain common to all chips in the daisy chain. The serial data is clocked to all of the chips, then the $\overline{CS/LD}$ signal is pulled high to update all of them simultaneously.

When \overline{CLR} is pulled low or when the part powers up, the output connects through an internal pass gate to V_{RST} and will go to whatever voltage is on V_{RST} . When any of three supplies (DV_{DD} , AV_{DD} , $|AV_{SS}|$) goes below 2.5V, the \overline{RSTOUT} pin goes low and stays low as long as the supply is below 2.5V. The power-on reset is also activated when one of the supplies drops below 2.5V and the output is then connected to V_{RST} . The output connects to V_{RST} when any of three conditions occur: \overline{CLR} goes low, the part

powers up or one of the supplies drops below 2.5V. This condition exists as long as $\overline{CS/LD}$ is low. As soon as $\overline{CS/LD}$ goes high, the DAC register is loaded with the data in the shift register and the output will settle to its new value.

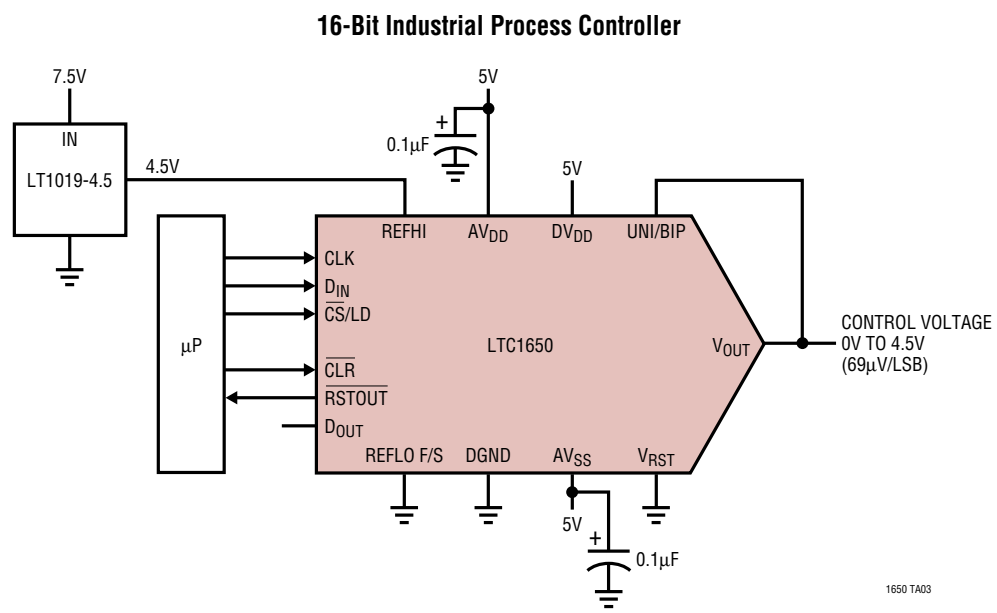
Voltage Output

The LTC1650 rail-to-rail buffered output can source or sink 5mA over the entire operating temperature range. The output can swing to within a few millivolts of either supply rail when unloaded and has an equivalent output resistance of 50 Ω when driving a load to the rails. The buffer amplifier can drive 1000pF without going into oscillation. The LTC1650 has a deglitched voltage output. The midscale glitch is less than 2nV-s. The digital feedthrough is about 0.05nV-s.

Output Ranges

The LTC1650 is capable of unipolar or bipolar output swing. When the UNI/BIP pin is connected to V_{OUT} the part is configured for unipolar operation and the output will swing from REFLO to REFHI. When UNI/BIP is connected to REFHI the part is configured in bipolar mode and the output will swing from $(2 \bullet \text{REFLO} - \text{REFHI})$ to REFHI and will be at REFLO at midscale. With REFLO = 0V the output swing is $\pm \text{REFHI}$ in bipolar mode and 0V to REFHI in unipolar mode.

TYPICAL APPLICATION



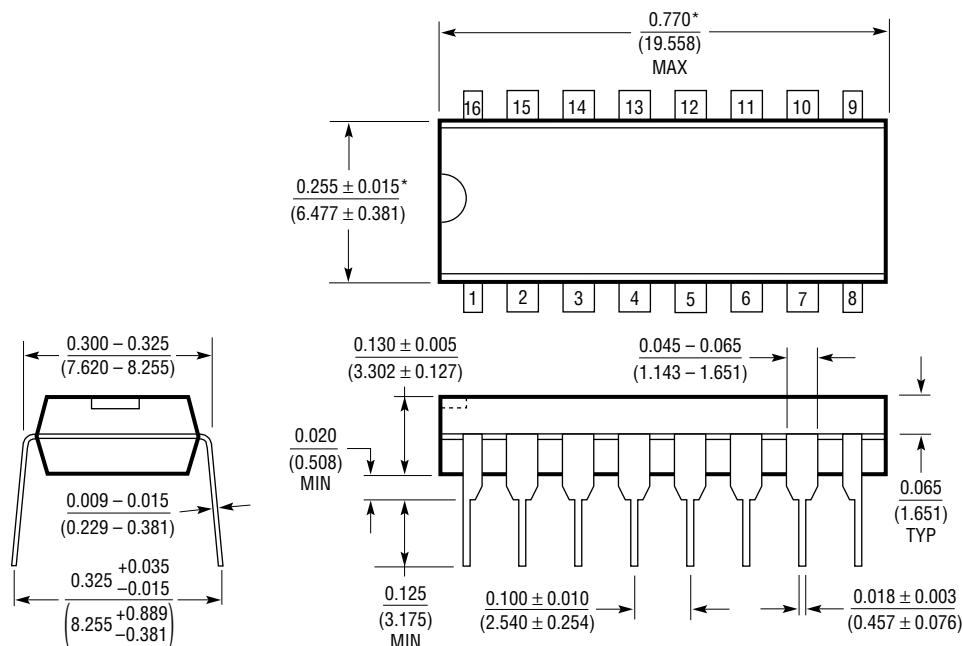
PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

N Package

16-Lead PDIP (Narrow 0.300)

(LTC DWG # 05-08-1510)



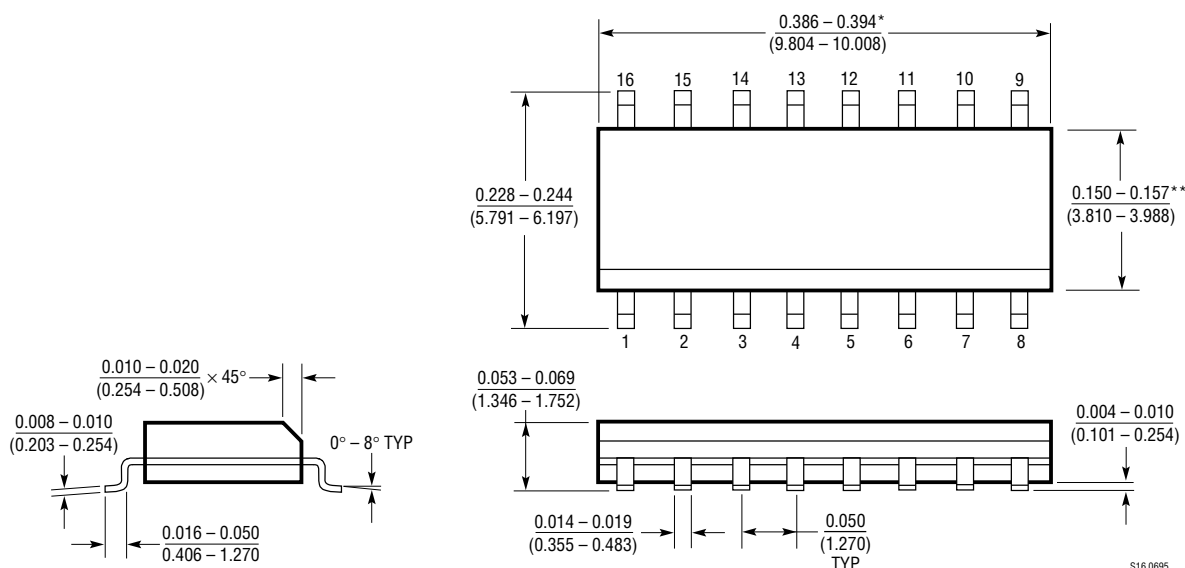
*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

N16 1197

S Package

16-Lead Plastic Small Outline (Narrow 0.150)

(LTC DWG # 05-08-1610)



DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006 (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010* (0.254mm) PER SIDE

S16 0695

