

μPower, 3V, 16-Bit, 150ksps 2-Channel ADC in MSOP

November 2002

FEATURES

- 16-Bit 150ksps ADC in MSOP Package
- Single 3V Supply
- Low Supply Current: 450μA (Typ)
- Auto Shutdown Reduces Supply Current to 10μA at 1ksps
- SPI/MICROWIRE™ Compatible Serial I/O
- 16-Bit Upgrade to 12-Bit LTC1288
- Pin Compatible with 12-Bit LTC1861L

APPLICATIONS

- High Speed Data Acquisition
- Portable or Compact Instrumentation
- Low Power Battery-Operated Instrumentation
- Isolated and/or Remote Data Acquisition

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DESCRIPTION

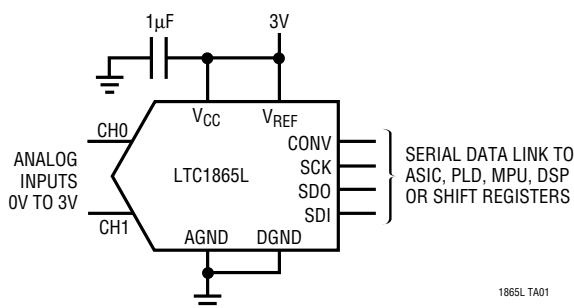
The LTC®1865L is a 16-bit A/D converter that is offered in MSOP and SO-8 packages and operates on a single 3V supply. At 150ksps, the supply current is only 450μA. The supply current drops at lower speeds because the LTC1865L automatically powers down to a typical supply current of 1nA between conversions. This 16-bit switched capacitor successive approximation ADC includes a sample-and-hold. The LTC1865L offers a software-selectable 2-channel MUX. An adjustable reference pin is provided on the MSOP version.

The 4-wire, serial I/O, MSOP or SO-8 package and extremely high sample rate-to-power ratio make this ADC an ideal choice for compact, low power, high speed systems.

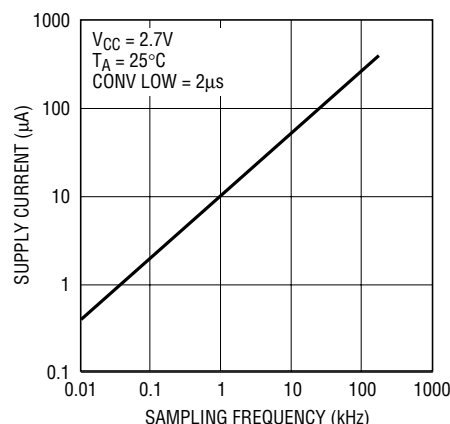
This ADC can be used in ratiometric applications or with external references. The high impedance analog inputs and the ability to operate with reduced spans down to 1V full scale, allow direct connection to signal sources in many applications, eliminating the need for external gain stages.

TYPICAL APPLICATION

Single 3V Supply, 150ksps, 16-Bit Sampling ADC



Supply Current vs Sampling Frequency



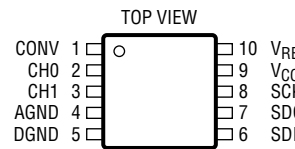
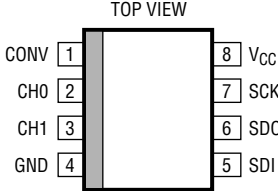
1865 TA02

LTC1865L

ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Supply Voltage (V_{CC})	7V	Power Dissipation	400mW
Ground Voltage Difference		Operating Temperature Range	
AGND, DGND (MSOP Package)	$\pm 0.3V$	LTC1865LC	0°C to 70°C
Analog Input	(GND – 0.3V) to ($V_{CC} + 0.3V$)	LTC1865LI	–40°C to 85°C
Digital Input	(GND – 0.3V) to 7V	Storage Temperature Range	–65°C to 150°C
Digital Output	(GND – 0.3V) to ($V_{CC} + 0.3V$)	Lead Temperature (Soldering, 10 sec)	300°C

PACKAGE/ORDER INFORMATION

 <p>MS PACKAGE 10-LEAD PLASTIC MSOP $T_{JMAX} = 150^{\circ}C$, $\theta_{JA} = 210^{\circ}C/W$</p>	ORDER PART NUMBER	 <p>S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 150^{\circ}C$, $\theta_{JA} = 175^{\circ}C/W$</p>	ORDER PART NUMBER
	LTC1865LCMS LTC1865LIMS LTC1865LACMS LTC1865LAIMS		LTC1865LCS8 LTC1865LIS8 LTC1865LACS8 LTC1865LAIS8
	MS PART MARKING		S8 PART MARKING
	LTJ4 LTJ6 LTJ5 LTJ7		1865L 1865LA 1865LI 865LAI

Consult LTC Marketing for parts specified with wider operating temperature ranges.

CONVERTER AND MULTIPLEXER CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are $T_A = 25^{\circ}C$. $V_{CC} = 2.7V$, $V_{REF} = 2.5V$ (MSOP) or $V_{REF} = V_{CC}$ (SO), $f_{SCK} = f_{SCK(MAX)}$ as defined in Recommended Operating Conditions, unless otherwise noted.

PARAMETER	CONDITIONS		LTC1865L			LTC1865LA			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Resolution		●	16			16			Bits
No Missing Codes Resolution		●	14			15			Bits
INL	(Note 3)	●			± 8			± 6	LSB
Transition Noise				2			2		LSB _{RMS}
Gain Error		●			± 20			± 20	mV
Offset Error		●		± 2	± 5		± 2	± 5	mV
Analog Input Range	+CH – GND or (–CH)	●	0		V_{REF}	0		V_{REF}	V
Absolute Input Range	+CH Input		–0.05		$V_{CC} + 0.05$	–0.05		$V_{CC} + 0.05$	V
	–CH Input		–0.05		$V_{CC}/2$	–0.05		$V_{CC}/2$	V
V_{REF} Input Range	MSOP		1		V_{CC}	1		V_{CC}	V
Analog Input Leakage Current	(Note 4)	●			± 1			± 1	μA
C_{IN} Input Capacitance	In Sample Mode			12			12		pF
	During Conversion			5			5		pF

DYNAMIC ACCURACY The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are $T_A = 25^\circ\text{C}$. $V_{CC} = 3\text{V}$, $V_{REF} = 3\text{V}$, $f_{\text{SAMPLE}} = 150\text{kHz}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SNR	Signal-to-Noise Ratio			82		dB
S/(N + D)	Signal-to-Noise Plus Distortion Ratio	1kHz Input Signal		82		dB
THD	Total Harmonic Distortion Up to 5th Harmonic	1kHz Input Signal		92		dB
	Full Power Bandwidth			10		MHz
	Full Linear Bandwidth	$S/(N + D) \geq 75\text{dB}$		20		kHz

DIGITAL AND DC ELECTRICAL CHARACTERISTICS The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are $T_A = 25^\circ\text{C}$. $V_{CC} = 2.7\text{V}$, $V_{REF} = 2.5\text{V}$ (MSOP) or $V_{REF} = V_{CC}$ (SO), unless otherwise noted.

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	$V_{CC} = 3.3\text{V}$	● 1.9			V
V_{IL}	Low Level Input Voltage	$V_{CC} = 2.7\text{V}$	●		0.45	V
I_{IH}	High Level Input Current	$V_{IN} = V_{CC}$	●		2.5	μA
I_{IL}	Low Level Input Current	$V_{IN} = 0\text{V}$	●		-2.5	μA
V_{OH}	High Level Output Voltage	$V_{CC} = 2.7\text{V}$, $I_O = 10\mu\text{A}$ $V_{CC} = 2.7\text{V}$, $I_O = 360\mu\text{A}$	● 2.3 ● 2.1	2.60 2.45		V V
V_{OL}	Low Level Output Voltage	$V_{CC} = 2.7\text{V}$, $I_O = 400\mu\text{A}$	●		0.3	V
I_{OZ}	Hi-Z Output Leakage	$CONV = V_{CC}$	●		± 3	μA
I_{SOURCE}	Output Source Current	$V_{OUT} = 0\text{V}$		-6.5		mA
I_{SINK}	Output Sink Current	$V_{OUT} = V_{CC}$		6.5		mA
I_{REF}	Reference Current (MSOP)	$CONV = V_{CC}$ $f_{\text{SMPL}} = f_{\text{SMPL}}(\text{MAX})$	● ●	0.001 0.01	3 0.1	μA mA
I_{CC}	Supply Current	$CONV = V_{CC}$ After Conversion $f_{\text{SMPL}} = f_{\text{SMPL}}(\text{MAX})$	● ●	0.5 0.45	10 1	μA mA
P_D	Power Dissipation	$f_{\text{SMPL}} = f_{\text{SMPL}}(\text{MAX})$		1.22		mW

RECOMMENDED OPERATING CONDITIONS The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are $T_A = 25^\circ\text{C}$.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		2.7		3.6	V
f_{SCK}	Clock Frequency	● DC			8	MHz
t_{CYC}	Total Cycle Time		$16 \cdot \text{SCK} + t_{\text{CONV}}$			μs
t_{SMPL}	Analog Input Sampling Time		14			SCK
t_{suCONV}	Setup Time $CONV \downarrow$ Before First $\text{SCK} \uparrow$ (See Figure 1)		60			ns
t_{hDI}	Hold Time SDI After $\text{SCK} \uparrow$		30			ns
t_{suDI}	Setup Time SDI Stable Before $\text{SCK} \uparrow$		30			ns
t_{WHCLK}	SCK High Time	$f_{\text{SCK}} = f_{\text{SCK}}(\text{MAX})$	45%			$1/f_{\text{SCK}}$
t_{WLCLK}	SCK Low Time	$f_{\text{SCK}} = f_{\text{SCK}}(\text{MAX})$	45%			$1/f_{\text{SCK}}$
t_{WHCONV}	$CONV$ High Time Between Data Transfer Cycles		t_{CONV}			μs
t_{WLCONV}	$CONV$ Low Time During Data Transfer		16			SCK
t_{hCONV}	Hold Time $CONV$ Low After Last $\text{SCK} \uparrow$		26			ns

TIMING CHARACTERISTICS The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are $T_A = 25^\circ\text{C}$. $V_{CC} = 2.7\text{V}$, $V_{REF} = 2.5\text{V}$ (MSOP) or $V_{REF} = V_{CC}$ (SO), $f_{SCK} = f_{SCK(MAX)}$ as defined in Recommended Operating Conditions, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{CONV}	Conversion Time (See Figure 1)		●		3.7	4.66	μs
$f_{SMPL(MAX)}$	Maximum Sampling Frequency		●	150			kHz
t_{dDO}	Delay Time, $SCK\downarrow$ to SDO Data Valid	$C_{LOAD} = 20\text{pF}$	●		45	55 60	ns ns
t_{dis}	Delay Time, $CONV\uparrow$ to SDO Hi-Z		●		55	120	ns
t_{en}	Delay Time, $CONV\downarrow$ to SDO Enabled	$C_{LOAD} = 20\text{pF}$	●		35	120	ns
t_{hDO}	Time Output Data Remains Valid After $SCK\downarrow$	$C_{LOAD} = 20\text{pF}$	●	5	15		ns
t_r	SDO Rise Time	$C_{LOAD} = 20\text{pF}$			25		ns
t_f	SDO Fall Time	$C_{LOAD} = 20\text{pF}$			12		ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

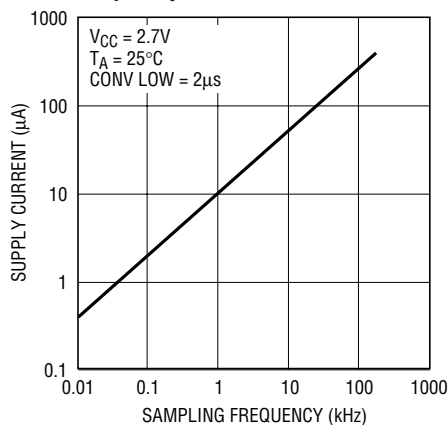
Note 2: All voltage values are with respect to GND.

Note 3: Integral nonlinearity is defined as deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 4: Channel leakage current is measured while the part is in sample mode.

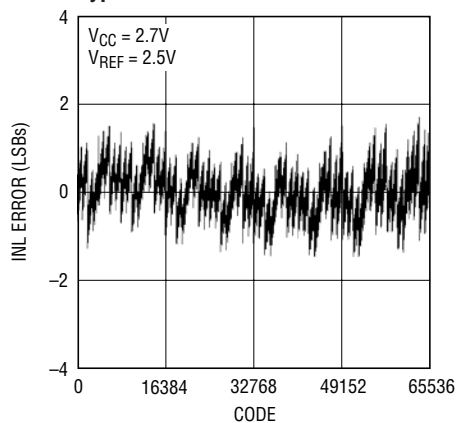
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Sampling Frequency



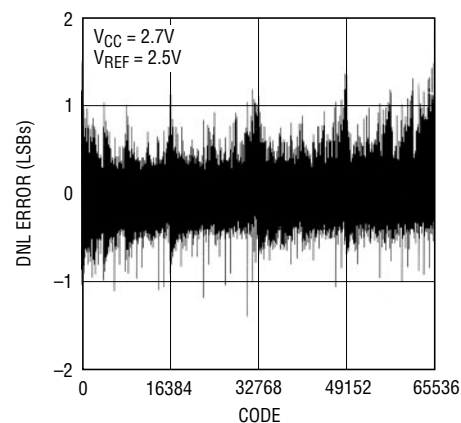
1865 TA02

Typical INL Curve



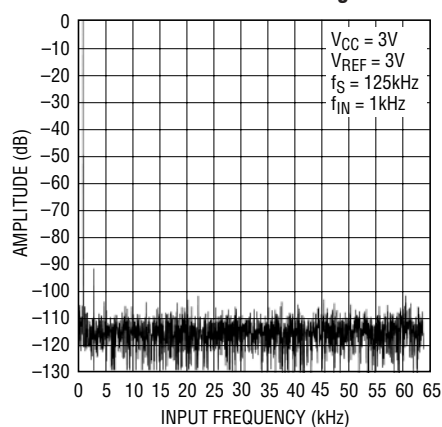
1865 G02

Typical DNL Curve



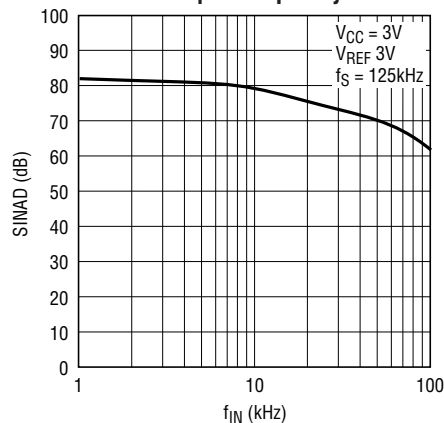
1865 G03

4096 Point FFT Nonaveraged



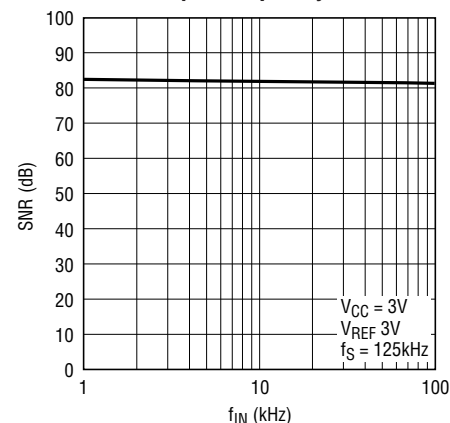
1865 G04

SINAD vs Input Frequency



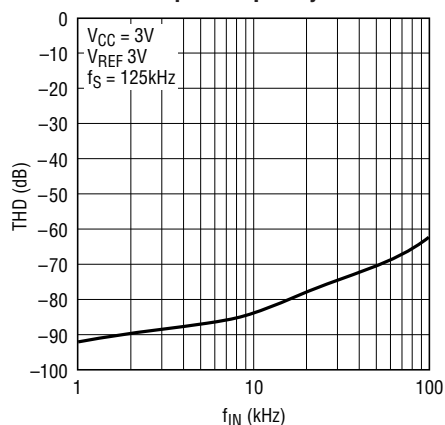
1865 G05

SNR vs Input Frequency



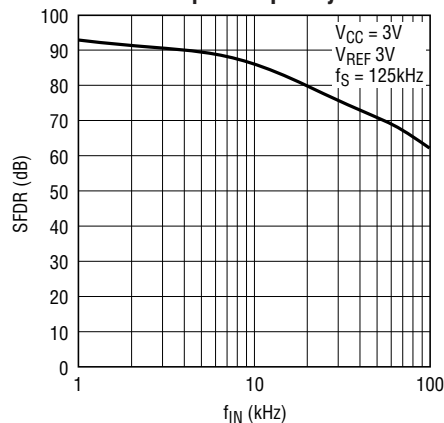
1865 G06

THD vs Input Frequency



1865 G07

SFDR vs Input Frequency



1865 G08

PIN FUNCTIONS

(MSOP Package)

CONV (Pin 1): Convert Input. A logic high on this input starts the A/D conversion process. If the CONV input is left high after the A/D conversion is finished, the part powers down. A logic low on this input enables the SDO pin, allowing the data to be shifted out.

CH0, CH1 (Pins 2, 3): Analog Inputs. These inputs must be free of noise with respect to AGND.

AGND (Pin 4): Analog Ground. AGND should be tied directly to an analog ground plane.

DGND (Pin 5): Digital Ground. DGND should be tied directly to an analog ground plane.

SDI (Pin 6): Digital Data Input. The A/D configuration word is shifted into this input.

SDO (Pin 7): Digital Data Output. The A/D conversion result is shifted out of this output.

SCK (Pin 8): Shift Clock Input. This clock synchronizes the serial data transfer.

V_{CC} (Pin 9): Positive Supply. This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.

V_{REF} (Pin 10): Reference Input. The reference input defines the span of the A/D converter and must be kept free of noise with respect to AGND.

(SO-8 Package)

CONV (Pin 1): Convert Input. A logic high on this input starts the A/D conversion process. If the CONV input is left high after the A/D conversion is finished, the part powers down. A logic low on this input enables the SDO pin, allowing the data to be shifted out.

CH0, CH1 (Pins 2, 3): Analog Inputs. These inputs must be free of noise with respect to GND.

GND (Pin 4): Analog Ground. GND should be tied directly to an analog ground plane.

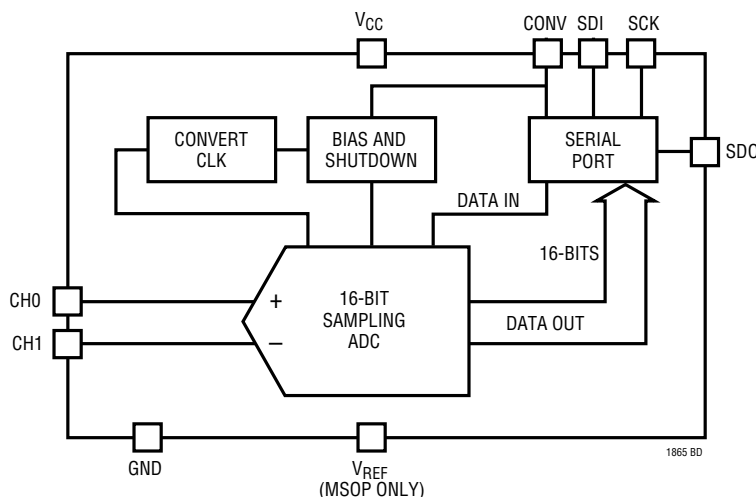
SDI (Pin 5): Digital Data Input. The A/D configuration word is shifted into this input.

SDO (Pin 6): Digital Data Output. The A/D conversion result is shifted out of this output.

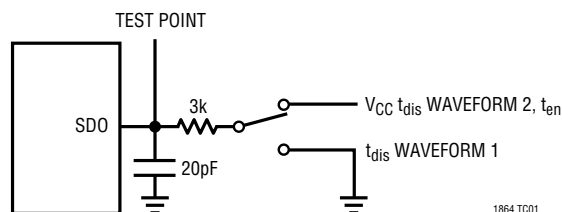
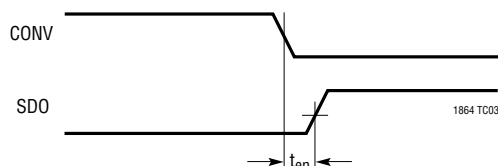
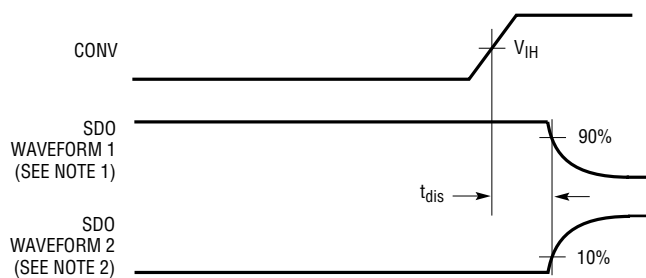
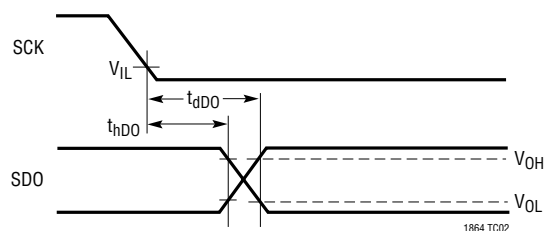
SCK (Pin 7): Shift Clock Input. This clock synchronizes the serial data transfer.

V_{CC} (Pin 8): Positive Supply. This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane. V_{REF} is tied internally to this pin.

BLOCK DIAGRAM



TEST CIRCUITS

Load Circuit for t_{dDO} , t_r , t_f , t_{dis} and t_{en} Voltage Waveforms for SDO Rise and Fall Times, t_r , t_f Voltage Waveforms for t_{en} Voltage Waveforms for t_{dis} Voltage Waveforms for SDO Delay Time, t_{dDO} and t_{hDO} 

APPLICATIONS INFORMATION

Operating Sequence

The LTC1865L conversion cycle begins with the rising edge of CONV. After a period equal to t_{CONV} , the conversion is finished. If CONV is left high after this time, the LTC1865L goes into sleep mode. If CONV goes low before the conversion is finished, it will terminate the conversion and the output data will be invalid. To prepare for the next conversion, it is still necessary to clock in the new data input word and shift out the invalid data output word. The next conversion cycle can then proceed normally. The LTC1865L's 2-bit data word is clocked into the SDI input on the rising edge of SCK after CONV goes low. Additional inputs on the SDI pin are then ignored until the next CONV cycle. The shift clock (SCK) synchronizes the data transfer with each bit being transmitted on the falling SCK edge and captured on the rising SCK edge in both transmitting and receiving systems. The data is transmitted and received simultaneously (full duplex). After completing the data transfer, if further SCK clocks are applied with CONV low, SDO will output zeros indefinitely. See Figure 1.

Analog Inputs

The two bits of the input word (SDI) assign the MUX configuration for the requested conversion. For a given channel selection, the converter will measure the voltage between the two channels indicated by the "+" and "-" signs in the selected row of Table 1. In single-ended mode, all input channels are measured with respect to GND (or AGND). A zero code will occur when the "+" input minus the "-" input equals zero. Full scale occurs when the "+" input minus the "-" input equals V_{REF} minus

1LSB. See Figure 2. Both the "+" and "-" inputs are sampled at the same time so common mode noise is rejected. The input span in the SO-8 package is fixed at $V_{\text{REF}} = V_{\text{CC}}$. If the "-" input in differential mode is grounded, a rail-to-rail input span will result on the "+" input.

Reference Input

The reference input of the LTC1865L SO-8 package is internally tied to V_{CC} . The span of the A/D converter is therefore equal to V_{CC} . The voltage on the reference input of the LTC1865L MSOP package defines the span of the A/D converter. The LTC1865L MSOP package can operate with voltages from 1V to V_{CC} .

Table 1. Multiplexer Channel Selection

	MUX ADDRESS		CHANNEL #		
	SGL/DIFF	ODD/SIGN	0	1	GND
SINGLE-ENDED MUX MODE	1	0	+		—
	1	1		+	—
DIFFERENTIAL MUX MODE	0	0	+	—	
	0	1	—	+	

1864 TBL1

GENERAL ANALOG CONSIDERATIONS

Grounding

The LTC1865L should be used with an analog ground plane and single point grounding techniques. Do not use wire wrapping techniques to breadboard and evaluate the device. To achieve the optimum performance, use a printed circuit board. The ground pins (AGND and DGND for the MSOP package and GND for the SO-8 package) should be

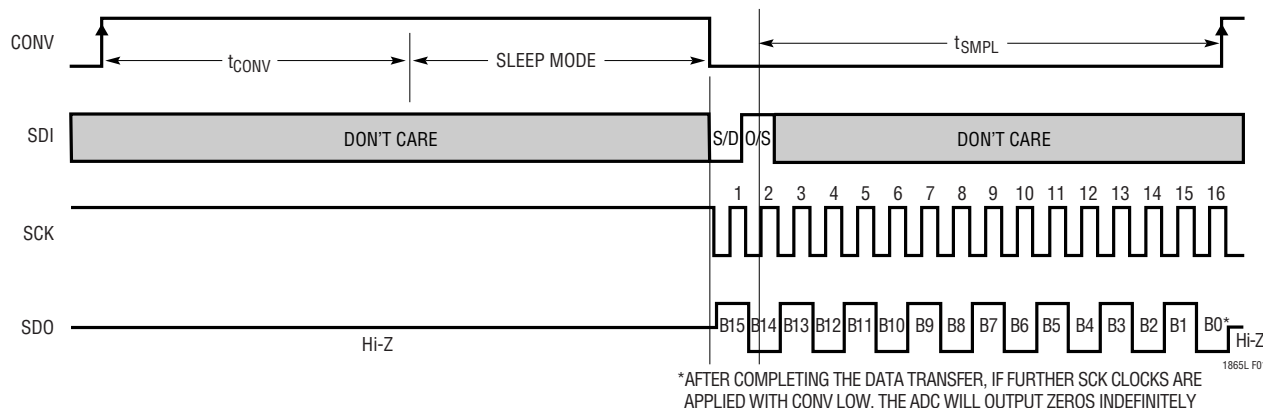


Figure 1. LTC1865L Operating Sequence

1865li

APPLICATIONS INFORMATION

tied directly to the analog ground plane with minimum lead length.

Bypassing

For good performance, the V_{CC} and V_{REF} pins must be free of noise and ripple. Any changes in the V_{CC}/V_{REF} voltage with respect to ground during the conversion cycle can induce errors or noise in the output code. Bypass the V_{CC} and V_{REF} pins directly to the analog ground plane with a minimum of 1 μ F tantalum. Keep the bypass capacitor leads as short as possible.

Analog Inputs

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1865L have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem if source

resistances are less than 200 Ω or high speed op amps are used (e.g., the LT[®]1211, LT1469, LT1807, LT1810, LT1630, LT1226 or LT1215). But if large source resistances are used, or if slow settling op amps drive the inputs, take care to ensure the transients caused by the current spikes settle completely before the conversion begins.

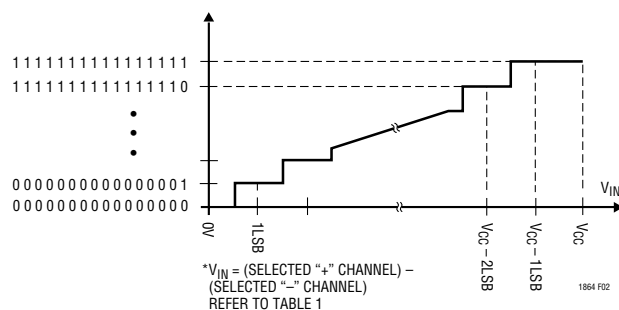
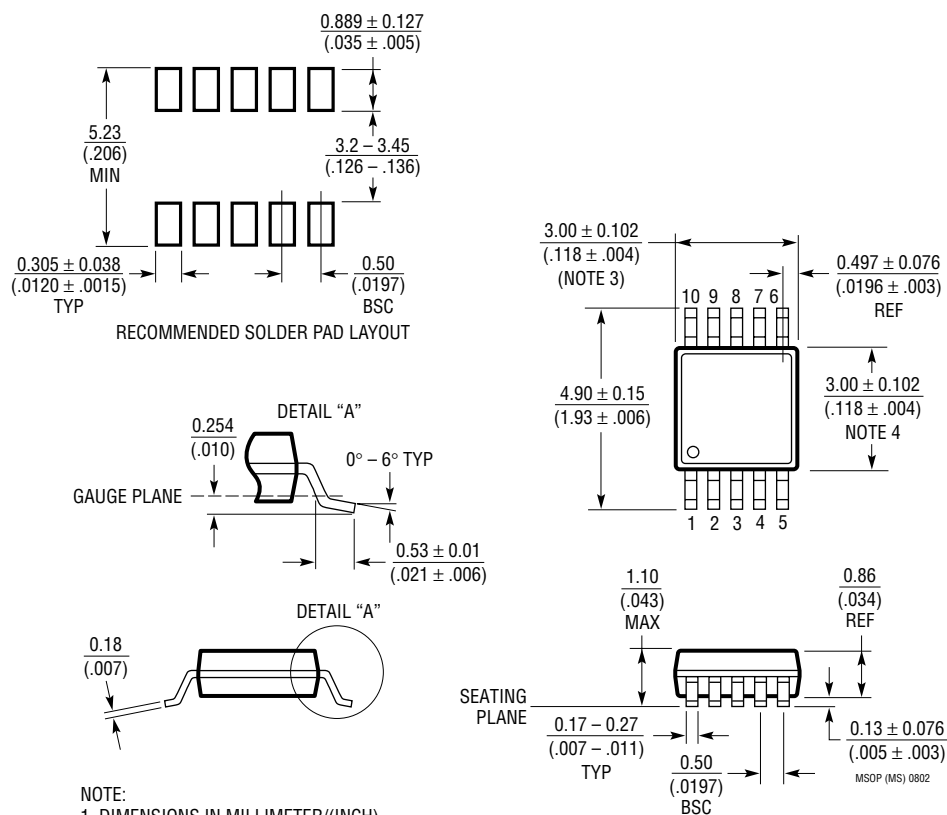


Figure 2. LTC1865L Transfer Curve

PACKAGE DESCRIPTION

MS Package
10-Lead Plastic MSOP
 (Reference LTC DWG # 05-08-1661)

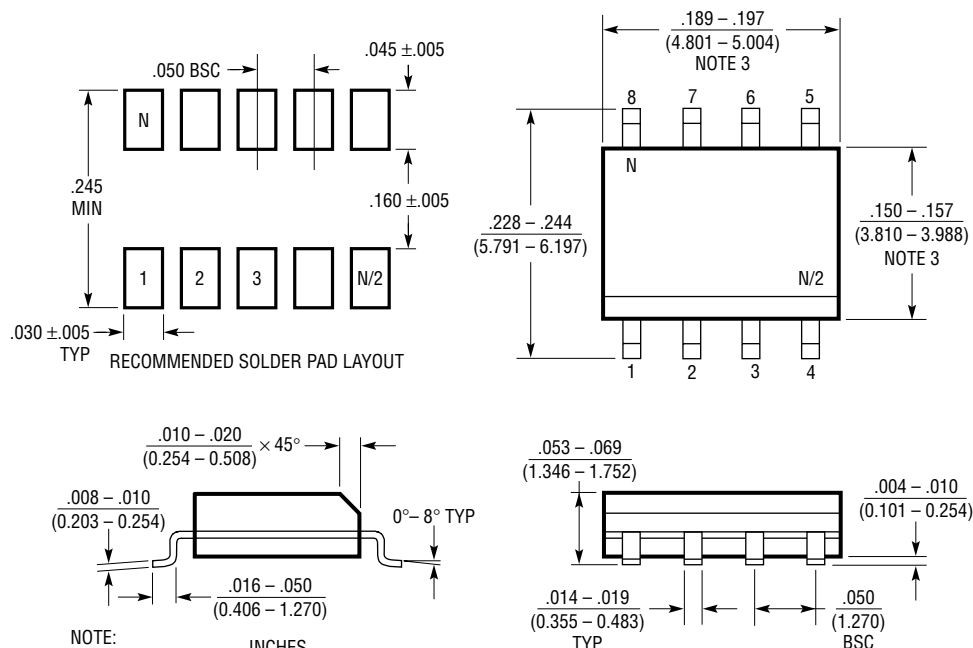


NOTE:

1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
 (Reference LTC DWG # 05-08-1610)



- NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
 2. DRAWING NOT TO SCALE
 3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

S08 0502

RELATED PARTS

PART NUMBER	SAMPLE RATE	POWER DISSIPATION	DESCRIPTION
8-Bit Serial I/O ADCs			
LTC1096/LTC1096L	15ksps	0.9mW	1-Channel, Unipolar Operation, 5V/3V
LTC1098/LTC1098L	15ksps	0.6mW	2-Channel, Unipolar Operation, 5V/3V
LTC1196	1Msps	20mW	1-Channel, Unipolar Operation with Reference Input, 5V/3V
LTC1198	750ksps	20mW	2-Channel, Unipolar Operation, 5V/3V
10-Bit Serial I/O ADCs			
LTC1197/LTC1197L	500ksps/250ksps	22.5mW	SO-8, MS8, 1-Channel, 5V/3V
LTC1199/LTC1199L	450ksps/210ksps	25mW	SO-8, MS8, 2-Channel, 5V/3V
12-Bit Serial I/O ADCs			
LTC1286/LTC1298	12.5ksps/11.1ksps	1.3mW/1.7mW	1-Channel with Reference (LTC1286), 2-Channel (LTC1298), 5V
LTC1400	400ksps	75mW	1-Channel, Bipolar or Unipolar Operation, Internal Reference, 5V
LTC1401	200ksps	15mW	SO-8 with Reference, 3V
LTC1402	2.2Msps	90mW	Serial I/O, Bipolar or Unipolar, Internal Reference
LTC1404	600ksps	25mW	SO-8 with Reference, Bipolar or Unipolar, 5V
LTC1860/LTC1861	250ksps	4.25mW	SO-8, MS8, 1-Channel, 5V/SO-8, MS10, 2-Channel, 5V
LTC1860L/LTC1861L	150ksps	1.95mW	SO-8, MS8, 1-Channel, 3V/SO-8, MS10, 2-Channel, 3V
14-Bit Serial I/O ADCs			
LTC1417	400ksps	20mW	16-Pin SSOP, Unipolar or Bipolar, Reference, 5V
LTC1418	200ksps	15mW	Serial/Parallel I/O, Internal Reference, 5V
16-Bit Serial I/O ADCs			
LTC1609	200ksps	65mW	Configurable Bipolar or Unipolar Input Ranges, 5V
LTC1864/LTC1865	250ksps	4.25mW	SO-8, MS8, 1-Channel, 5V/SO-8, MS10, 2-Channel, 5V
LTC1864L	150ksps	1.22mW	SO-8, MS8, 1-Channel, 3V

PART NUMBER	DESCRIPTION	COMMENTS
References		
LT1460	Micropower Precision Series Reference	Bandgap, 130 μ A Supply Current, 10ppm/ $^{\circ}$ C, Available in SOT-23
LT1790	Micropower Low Dropout Reference	60 μ A Supply Current, 10ppm/ $^{\circ}$ C, SOT-23
Op Amps		
LT1468/LT1469	Single/Dual 90MHz, 16-Bit Accurate Op Amps	22V/ μ s Slew Rate, 75 μ V/125 μ V Offset
LT1806/LT1807	Single/Dual 325MHz Low Noise Op Amps	140V/ μ s Slew Rate, 3.5nV/ $\sqrt{\text{Hz}}$ Noise, –80dBc Distortion
LT1809/LT1810	Single/Dual 180MHz Low Distortion Op Amps	350V/ μ s Slew Rate, –90dBc Distortion at 5MHz