2-Phase, High Efficiency, Step-Down Controller for AMD Opteron™ CPUs

FEATURES

- **Output Stages Operate Antiphase Reducing Input and Output Capacitance Requirements and Power Supply Induced Noise**
- **Dual Input Supply Capability for Load Sharing**
- **5-Bit AMD CPU VID Code:**
  V_{OUT} = 0.8V to 1.55V
- **±1% Output Voltage Accuracy**
- **True Remote Sensing Differential Amplifier**
- **Power Good Output Voltage Monitor**
- **Supports Active Voltage Positioning**
- Current Mode Control Ensures Current Sharing
- OPTI-LOOP® Compensation Minimizes C_{OUT}
- Three Operational Modes: PWM, Burst and Cycle Skip
- Programmable Fixed Frequency: 150kHz to 300kHz
- Wide V_{IN} Range: 4V to 36V Operation
- Adjustable Soft-Start Current Ramping
- Internal Current Foldback and Short-Circuit Shutdown
- Overvoltage Soft Latch Eliminates Nuisance Trips
- Available in 36-Lead Narrow (0.209) SSOP Package

APPLICATIONS

- Servers and Workstations

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OPTI-LOOP and Burst Mode are registered trademarks of Linear Technology Corporation.
AMD Opteron is a trademark of Advanced Micro Devices, Inc.

DESCRIPTION

The LTC®3719 is a 2-phase, VID programmable, synchronous step-down switching regulator controller that drives two N-channel external power MOSFET stages in a fixed frequency architecture. The 2-phase controller drives its two output stages out of phase at frequencies up to 300kHz to minimize the RMS ripple currents in both input and output capacitors. The 2-phase technique effectively multiplies the fundamental frequency by two, improving transient response while operating each channel at an optimum frequency for efficiency. Thermal design is also simplified.

An operating mode select pin (FCB) can be used to select among three modes including Burst Mode® operation for highest efficiency. An internal differential amplifier provides true remote sensing of the regulated supply's positive and negative output terminals as required in high current applications.

The RUN/SS pin provides soft-start and optional timed, short-circuit shutdown. Current foldback limits MOSFET dissipation during short-circuit conditions when the overcurrent latchoff is disabled. OPTI-LOOP compensation allows the transient response to be optimized for a wide range of output capacitors and ESR values.

TYPICAL APPLICATION

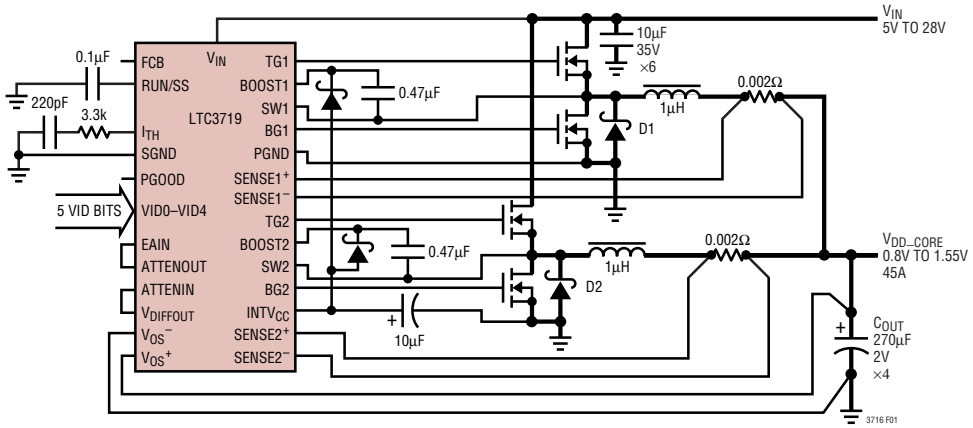


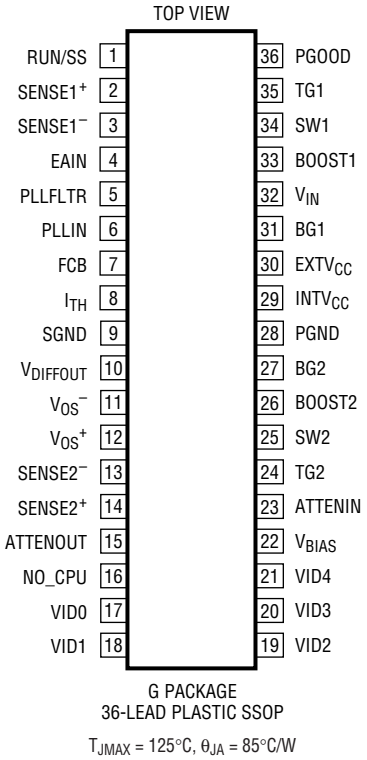
Figure 1. High Current Dual Phase Step-Down Converter

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply Voltage (V_{IN}) ..... 36V to –0.3V
Topside Driver Voltages (BOOST1,2) ..... 42V to –0.3V
Switch Voltage (SW1, 2) ..... 36V to –5 V
SENSE1+, SENSE2+, SENSE1–,
SENSE2– Voltages ..... (1.1)$INTV_{CC}$ to –0.3V
EAIN, V_{OS}^+, V_{OS}^-, $EXTV_{CC}$, $INTV_{CC}$, RUN/SS,
V_{BIAS}, ATTENIN, ATTENOUT, PGOOD, NO_CPU,
VID0–VID4, Voltages ..... 7V to –0.3V
Boosted Driver Voltage (BOOST-SW) ..... 7V to –0.3V
PLLFLTR, PLLIN, $V_{DIFFOUT}$,
FCB Voltages ..... $INTV_{CC}$ to –0.3V
I_{TH} Voltage ..... 2.7V to –0.3V
Peak Output Current <1µs(TG1, 2, BG1, 2) 3A
$INTV_{CC}$ RMS Output Current 50mA
Operating Ambient Temperature Range
(Note 2) ..... –40°C to 85°C
Junction Temperature (Note 3) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
36-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 85°C/W

ORDER PART NUMBER
LTC3719EG

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 15V, V_{BIAS} = 5V, $V_{RUN/SS}$ = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loop							
V_{EAIN}	Regulated Feedback Voltage	I_{TH} Voltage = 1.2V; Measured at V_{EAIN} (Note 4)	●	0.594	0.600	0.606	V
$V_{SENSEMAX}$	Maximum Current Sense Threshold		●	62	75	88	mV
I_{INEAIN}	Feedback Current	(Note 4)			–5	–50	nA
$V_{LOADREG}$	Output Voltage Load Regulation	(Note 4) Measured in Servo Loop, ΔI_{TH} Voltage: 1.2V to 0.7V Measured in Servo Loop, ΔI_{TH} Voltage: 1.2V to 2V	 ● ●		 0.1 –0.1	 0.5 –0.5	 % %
$V_{REFLNREG}$	Reference Voltage Line Regulation	V_{IN} = 3.6V to 30V (Note 4)			0.002	0.02	%/V
V_{FCB}	Forced Continuous Threshold		●	0.57	0.6	0.63	V
I_{FCB}	Forced Continuous Current				–0.17	–1	µA
$V_{BINHIBIT}$	Burst Inhibit (Constant Frequency) Threshold	Measured at FCB pin			4.3	4.8	V
V_{OVL}	Output Overvoltage Threshold	Measured at V_{EAIN}	●	0.64	0.66	0.68	V
UVLO	Undervoltage Lockout	V_{IN} Ramping Down		3	3.33	4	V
g_m	Transconductance Amplifier g_m	I_{TH} = 1.2V, Sink/Source 5µA (Note 4)			3		mmho
g_{mOL}	Transconductance Amplifier Gain	I_{TH} = 1.2V, ($g_m \cdot Z_L$; No Ext Load) (Note 4)			1.5		V/mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 15V, V_{BIAS} = 5V, $V_{RUN/SS}$ = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_Q	Input DC Supply Current Normal Mode Shutdown	(Note 5) $V_{RUN/SS}$ = 0V			 1.2 20	 40	 mA µA
$I_{RUN/SS}$	Soft-Start Charge Current	$V_{RUN/SS}$ = 1.9V		–0.5	–1.2		µA
$V_{RUN/SS}$	RUN/SS Pin ON Threshold	$V_{RUN/SS}$ Rising		1.0	1.5	1.9	V
$V_{RUN/SSLO}$	RUN/SS Pin Latchoff Arming	$V_{RUN/SS}$ Rising from 3V			4.1	4.5	V
I_{SCL}	RUN/SS Discharge Current	Soft Short Condition V_{EAIN} = 0.5V, $V_{RUN/SS}$ = 4.5V		0.5	2	4	µA
I_{SDLHO}	Shutdown Latch Disable Current	V_{EAIN} = 0.5V			1.6	5	µA
I_{SENSE}	Total Sense Pins Source Current	Each Channel: $V_{SENSE1-,\,2-}$ = $V_{SENSE1+,\,2+}$ = 0V		–85	–60		µA
DF_{MAX}	Maximum Duty Factor	In Dropout		98	99.5		%
 $TG1, 2\ t_r$ $TG1, 2\ t_f$	Top Gate Transition Time: Rise Time Fall Time	(Note 6) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 30 40	 90 90	 ns ns
 $BG1, 2\ t_r$ $BG1, 2\ t_f$	Bottom Gate Transition Time: Rise Time Fall Time	(Note 6) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 30 20	 90 90	 ns ns
TG/BG t_{1D}	Top Gate Off to Bottom Gate On Delay Synchronous Switch-On Delay Time	C_{LOAD} = 3300pF Each Driver (Note 6)			90		ns
BG/TG t_{2D}	Bottom Gate Off to Top Gate On Delay Top Switch-On Delay Time	C_{LOAD} = 3300pF Each Driver (Note 6)			90		ns
$t_{ON(MIN)}$	Minimum On-Time	Tested with a Square Wave (Note 7)			180		ns
Internal V_{CC} Regulator							
V_{INTVCC}	Internal V_{CC} Voltage	6V < V_{IN} < 30V, V_{EXTVCC} = 4V		4.8	5.0	5.2	V
V_{LDO} INT	$INTV_{CC}$ Load Regulation	I_{CC} = 0 to 20mA, V_{EXTVCC} = 4V			0.2	1.0	%
V_{LDO} EXT	$EXTV_{CC}$ Voltage Drop	I_{CC} = 20mA, V_{EXTVCC} = 5V			80	160	mV
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage	I_{CC} = 20mA, $EXTV_{CC}$ Ramping Positive	●	4.5	4.7		V
V_{LDOHYS}	$EXTV_{CC}$ Switchover Hysteresis	I_{CC} = 20mA, $EXTV_{CC}$ Ramping Negative			0.2		V
VID Parameters							
V_{BIAS}	Operating Supply Voltage Range			2.7		5.5	V
R_{ATTEN}	Resistance Between ATTENIN and ATTENOUT Pins				10		kΩ
$ATTEN_{ERR}$	Resistive Divider Error		●	–0.35		0.25	%
R_{PULLUP}	VID0 to VID4 Pull-Up Resistance	(Note 8)			40		kΩ
VID_{THLOW}	VID0 to VID4 Logic Threshold Low					0.4	V
VID_{THHIGH}	VID0 to VID4 Logic Threshold High			1.6			V
VID_{LEAK}	VID0 to VID4 Leakage	V_{BIAS} < VID0–VID4 < 7V				±1	µA
V_{NO_CPU}	NO_CPU Maximum Output Voltage	I_{NO_CPU} = 2mA				0.4	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 15V, V_{BIAS} = 5V, $V_{RUN/SS}$ = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Oscillator and Phase-Locked Loop							
f_{NOM}	Nominal Frequency	$V_{PLLFLTR}$ = 1.2V		190	220	250	kHz
f_{LOW}	Lowest Frequency	$V_{PLLFLTR}$ = 0V		120	140	160	kHz
f_{HIGH}	Highest Frequency	$V_{PLLFLTR}$ ≥ 2.4V		280	310	360	kHz
R_{PLLIN}	PLLIN Input Resistance				50		kΩ
$I_{PLLFLTR}$	Phase Detector Output Current Sinking Capability Sourcing Capability	 $f_{PLLIN} < f_{OSC}$ $f_{PLLIN} > f_{OSC}$			 –15 15		 µA µA
R_{RELPHS}	Controller 2-Controller 1 Phase				180		Deg
PGOOD Output							
V_{PGL}	PGOOD Voltage Low	I_{PGOOD} = 2mA			0.1	0.3	V
I_{PGOOD}	PGOOD Leakage Current	V_{PGOOD} = 5V				±1	µA
V_{PG}	PGOOD Trip Level, Either Controller	V_{EAIN} with Respect to Set Output Voltage V_{EAIN} Ramping Negative V_{EAIN} Ramping Positive		 –8 8	 –10 10	 –12 12	 % %
Differential Amplifier/Op Amp Gain Block							
A_{DA}	Differential Amplifier Gain	V_{AMPMD} = 0V		0.995	1	1.005	V/V
$CMRR_{DA}$	Common Mode Rejection Ratio	0V < V_{CM} < 5V; V_{AMPMD} = 0V		46	55		dB
R_{IN}	Input Resistance	Measured at V_{OS}+ Input; V_{AMPMD} = 0V			80		kΩ

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LTC3719EG is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

LTC3719EG: $T_J = T_A + (P_D \bullet 85°C/W)$

Note 4: The LTC3719 is tested in a feedback loop that servos V_{ITH} to a specified voltage and measures the resultant V_{EAIN}.

Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

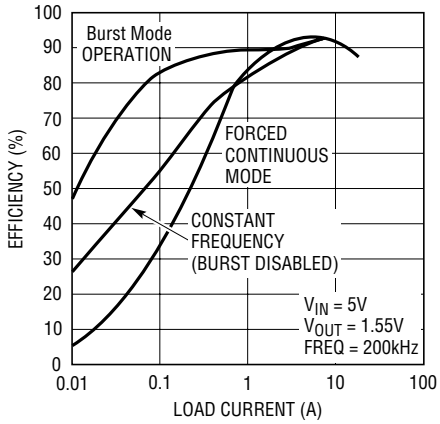
Note 6: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

Note 7: The minimum on-time condition corresponds to the on inductor peak-to-peak ripple current ≥40% I_{MAX} (see Minimum On-Time Considerations in the Applications Information section).

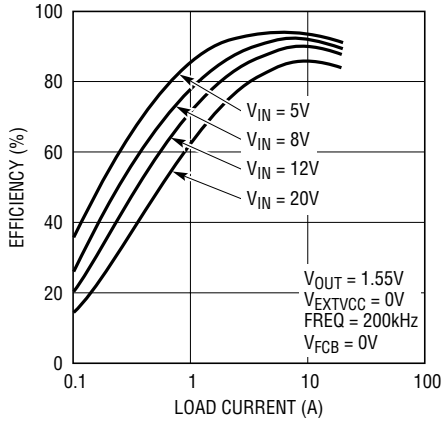
Note 8: Each built-in pull-up resistor attached to the VID inputs also has a series diode to allow input voltages higher than the $VIDV_{CC}$ supply without damage or clamping (see the Applications Information section).

TYPICAL PERFORMANCE CHARACTERISTICS

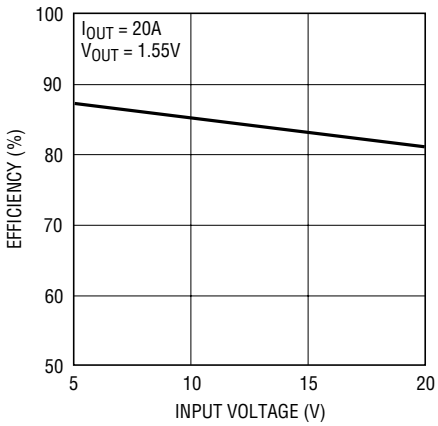
Efficiency vs Load Current (3 Operating Modes) (Figure 12)



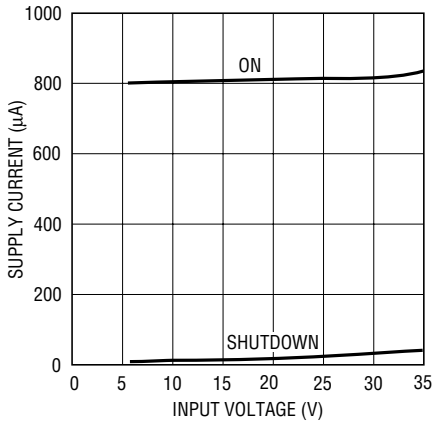
Efficiency vs Load Current (Figure 12)



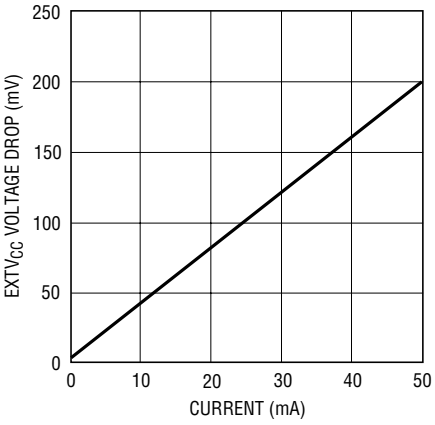
Efficiency vs Input Voltage (Figure 12)



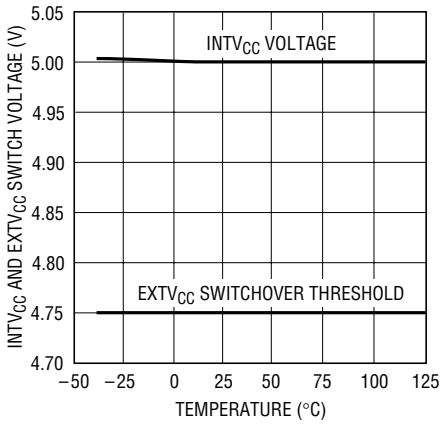
Supply Current vs Input Voltage and Mode



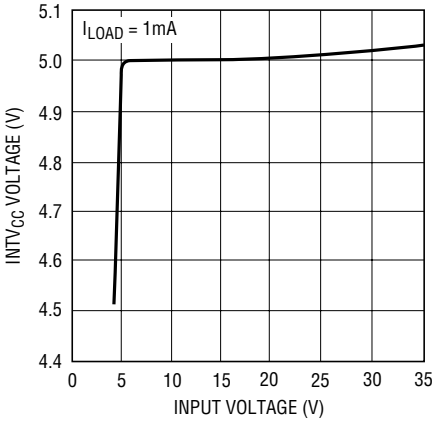
$EXTV_{CC}$ Voltage Drop



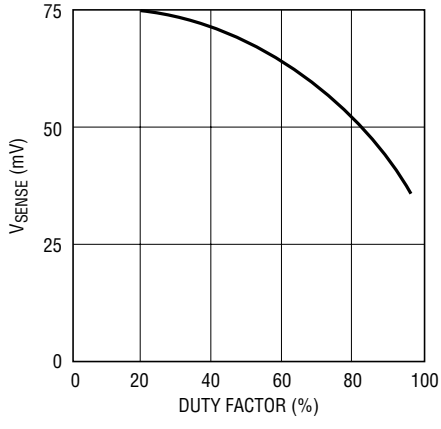
$INTV_{CC}$ and $EXTV_{CC}$ Switch Voltage vs Temperature



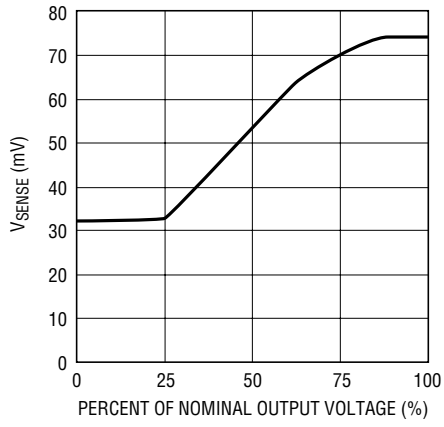
Internal 5V LDO Line Reg



Maximum Current Sense Threshold vs Duty Factor

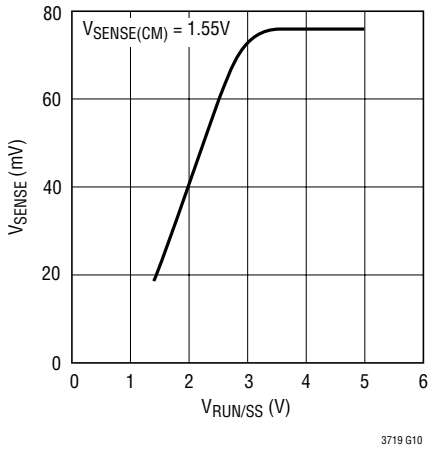


Maximum Current Sense Threshold vs Percent of Nominal Output Voltage (Foldback)



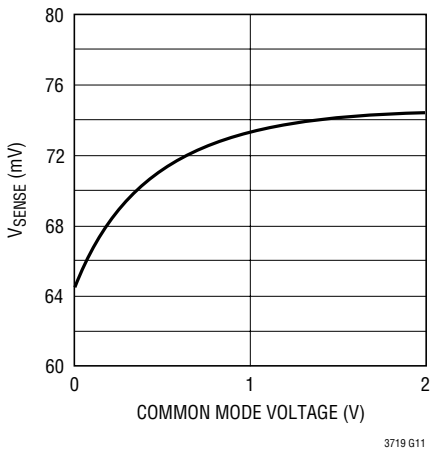
TYPICAL PERFORMANCE CHARACTERISTICS

Maximum Current Sense Threshold vs $V_{RUN/SS}$ (Soft-Start)



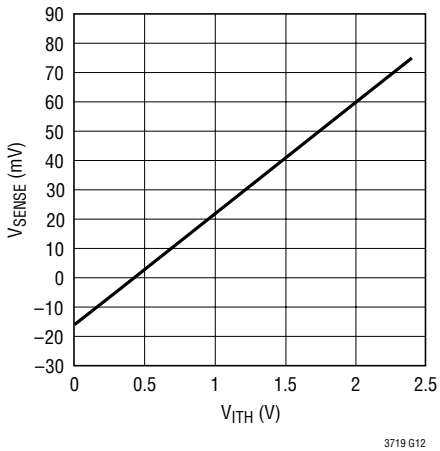
3719 G10

Maximum Current Sense Threshold vs Sense Common Mode Voltage



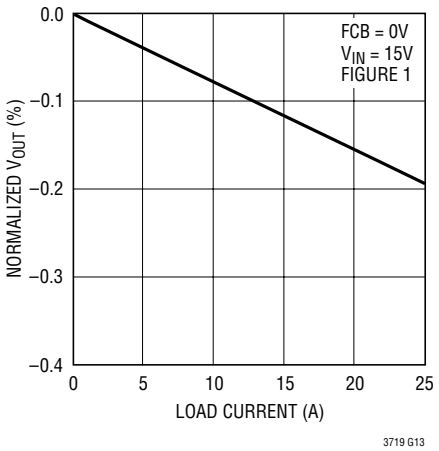
3719 G11

Current Sense Threshold vs I_{TH} Voltage



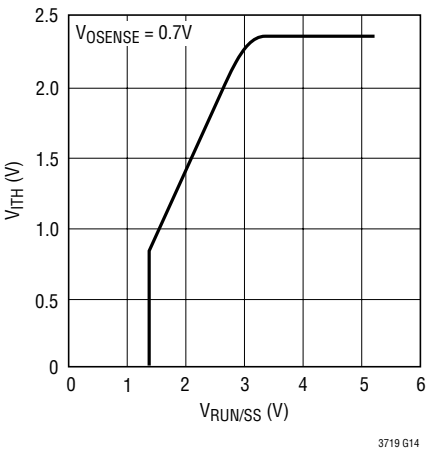
3719 G12

Load Regulation



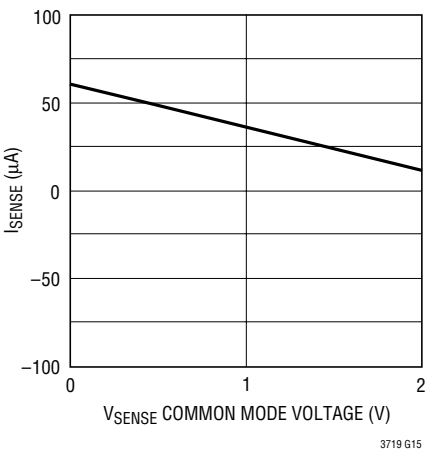
3719 G13

V_{ITH} vs $V_{RUN/SS}$ (Soft-Start)



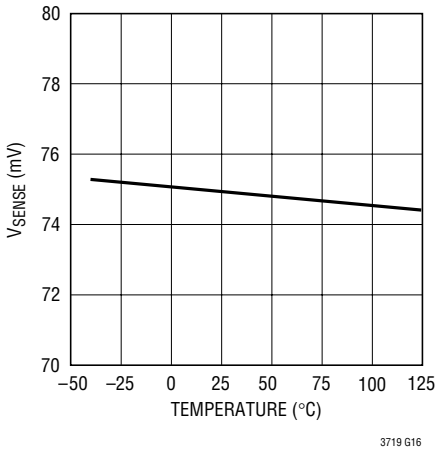
3719 G14

SENSE Pins Total Source Current



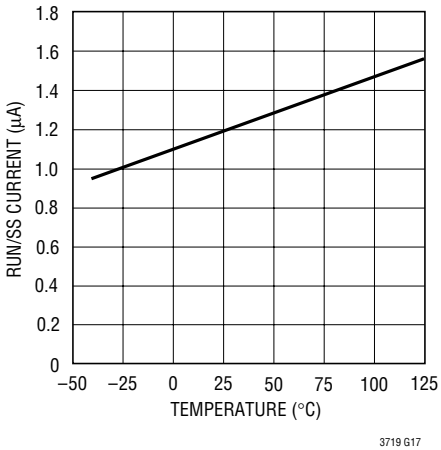
3719 G15

Maximum Current Sense Threshold vs Temperature



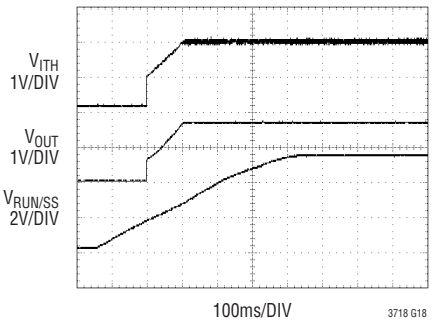
3719 G16

RUN/SS Current vs Temperature



3719 G17

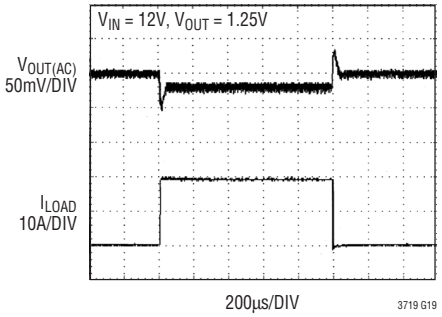
Soft-Start Up (Figure 12)



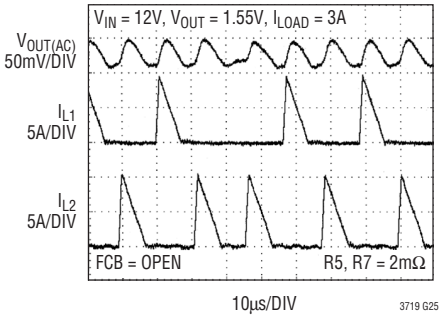
3718 G18

TYPICAL PERFORMANCE CHARACTERISTICS

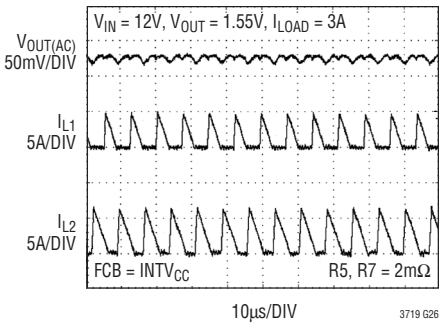
Load Step (Figure 12)



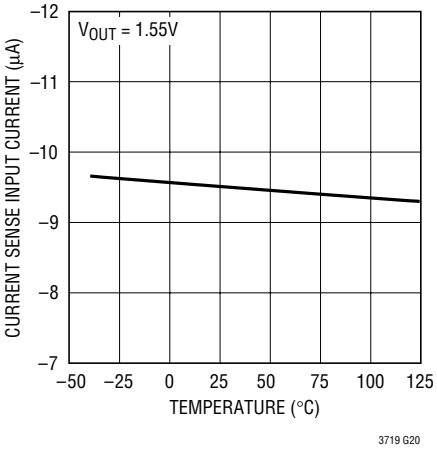
Burst Mode Operation (Figure 12)



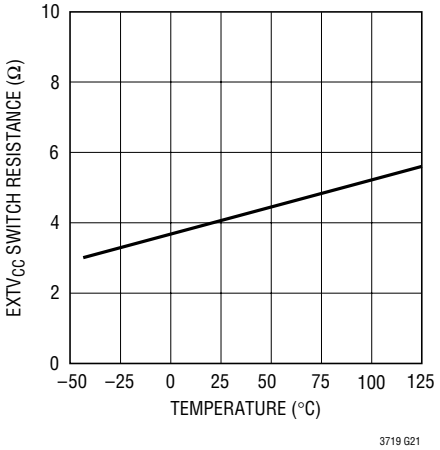
Constant Frequency Mode (Figure 12)



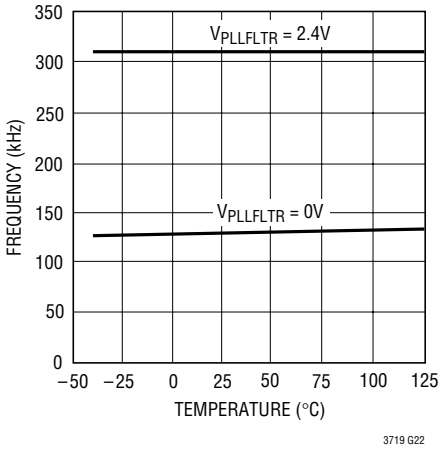
Current Sense Pin Input Current vs Temperature



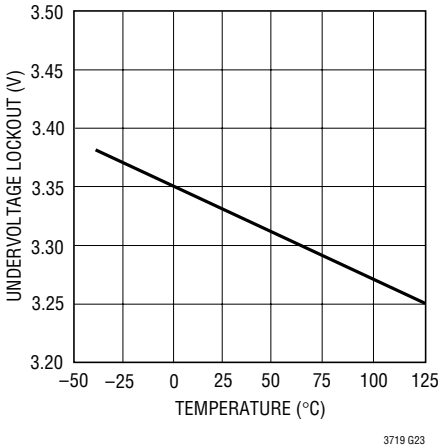
$EXTV_{CC}$ Switch Resistance vs Temperature



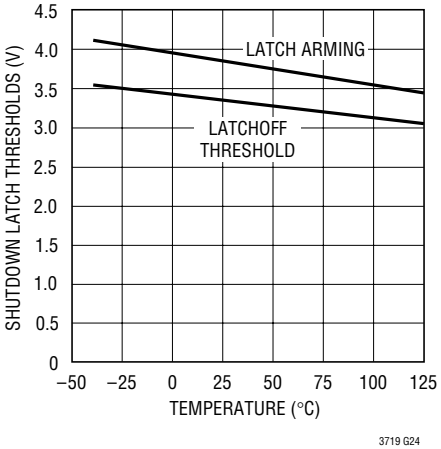
Oscillator Frequency vs Temperature



Undervoltage Lockout vs Temperature



$V_{RUN/SS}$ Shutdown Latch Thresholds vs Temperature



PIN FUNCTIONS

RUN/SS (Pin 1): Combination of Soft-Start, Run Control Input and Short-Circuit Detection Timer. A capacitor to ground at this pin sets the ramp time to full current output. Forcing this pin below 0.8V causes the IC to shut down all internal circuitry. All functions are disabled in shutdown.

SENSE1$^+$, SENSE2$^+$ (Pins 2,14): The (+) Input to Each Differential Current Comparator. The I_{TH} pin voltage and built-in offsets between SENSE$^-$ and SENSE$^+$ pins in conjunction with R_{SENSE} set the current trip threshold.

SENSE1$^-$, SENSE2$^-$ (Pins 3,13): The (–) Input to the Differential Current Comparators.

EAIN (Pin 4): Input to the error amplifier that compares the feedback voltage to the internal 0.6V reference voltage. This pin is normally connected to a resistive divider from the output of the differential amplifier (DIFFOUT).

PLLFLTR (Pin 5): The phase-locked loop's lowpass filter is tied to this pin. Alternatively, this pin can be driven with an AC or DC voltage source to vary the frequency of the internal oscillator. Do not apply voltage to this pin prior to application of V_{IN}.

PLLIN (Pin 6): External Synchronization Input to Phase Detector. This pin is internally terminated to SGND with 50kΩ. The phase-locked loop will force the rising top gate signal of controller 1 to be synchronized with the rising edge of the PLLIN signal.

FCB (Pin 7): Forced Continuous Control Input. This input acts on both output stages. Pulling this pin below 0.6V will force continuous synchronous operation. Do not leave this pin floating without a decoupling capacitor.

I_{TH} (Pin 8): Error Amplifier Output and Switching Regulator Compensation Point. Both current comparator's thresholds increase with this control voltage. The normal voltage range of this pin is from 0V to 2.4V

SGND (Pin 9): Signal Ground. This pin is common to both controllers. Route separately to the PGND pin.

$V_{DIFFOUT}$ (Pin 10): Output of a Differential Amplifier. This pin provides true remote output voltage sensing. $V_{DIFFOUT}$ normally drives an external resistive divider that sets the output voltage.

V_{OS}^-, V_{OS}^+ (Pins 11, 12): Inputs to an Operational Amplifier. Internal precision resistors configure it as a differential amplifier whose output is $V_{DIFFOUT}$.

ATTENOUT (Pin 15): Voltage Feedback Signal Resistively Divided According to the VID Programming Code.

NO_CPU (Pin 16): Open-Drain Logic Output. NO_CPU is pulled to ground if VID0 to VID3 are all high.

VID0–VID4 (Pins 17,18, 19, 20, 21): VID Control Logic Input Pins.

V_{BIAS} (Pin 22): Supply Pin for the VID Control Circuit.

ATTENIN (Pin 23): The Input to the VID Controlled Resistive Divider.

TG2, TG1 (Pins 24, 35): High Current Gate Drives for Top N-Channel MOSFETS. These are the outputs of floating drivers with a voltage swing equal to $INTV_{CC}$ superimposed on the switch node voltage SW.

PIN FUNCTIONS

SW2, SW1 (Pins 25, 34): Switch Node Connections to Inductors. Voltage swing at these pins is from a Schottky diode (external) voltage drop below ground to V_{IN}.

BOOST2, BOOST1 (Pins 26, 33): Bootstrapped Supplies to the Topside Floating Drivers. External capacitors are connected between the BOOST and SW pins, and Schottky diodes are connected between the BOOST and $INTV_{CC}$ pins.

BG2, BG1 (Pins 27, 31): High Current Gate Drives for Bottom N-Channel MOSFETS. Voltage swing at these pins is from ground to $INTV_{CC}$.

PGND (Pin 28): Driver Power Ground. Connect to sources of bottom N-channel MOSFETS and the (–) terminals of C_{IN}.

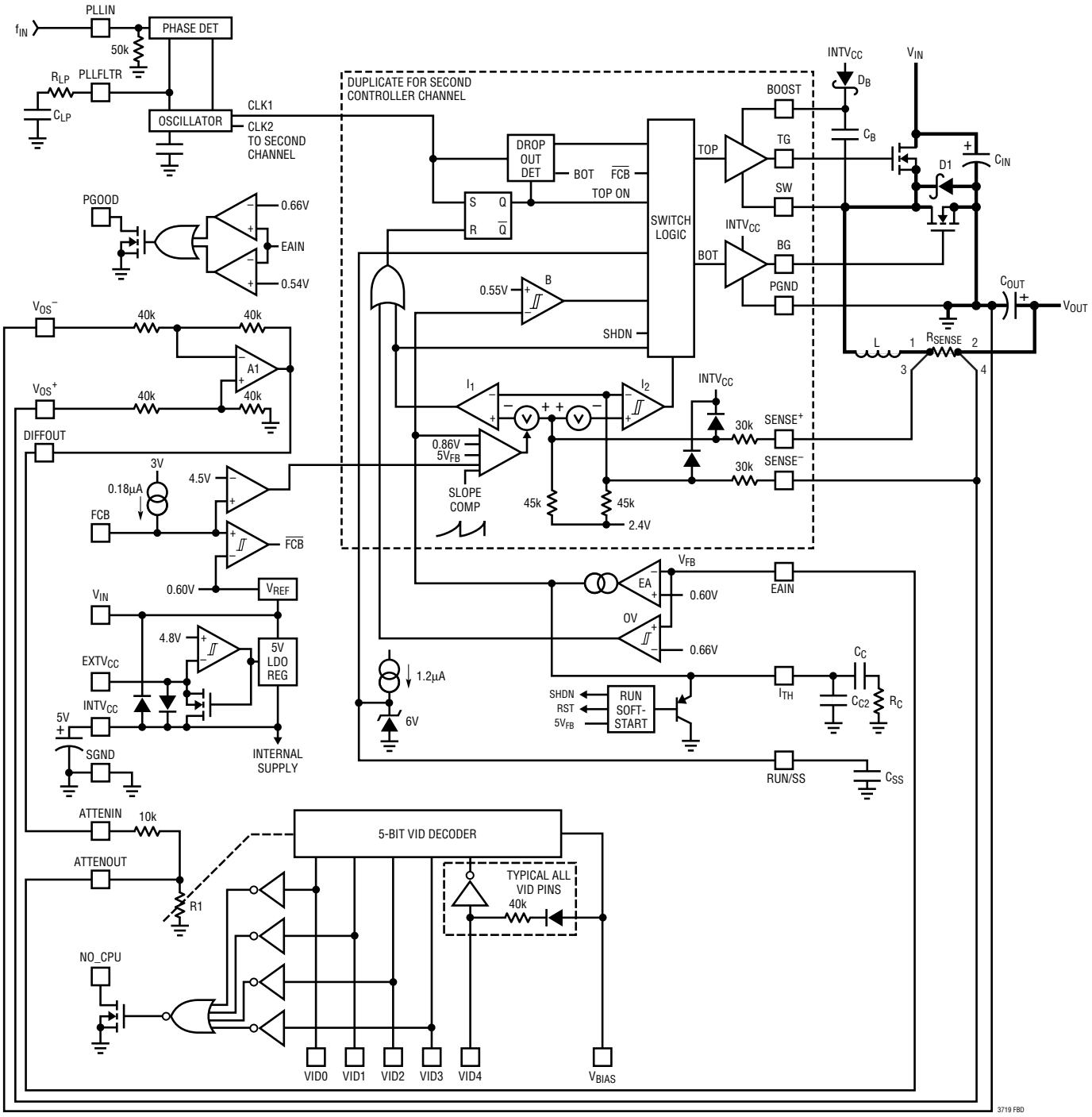
$INTV_{CC}$ (Pin 29): Output of the Internal 5V Linear Low Dropout Regulator and the $EXTV_{CC}$ Switch. The driver and control circuits are powered from this voltage source. Decouple to power ground with a 1µF ceramic capacitor placed directly adjacent to the IC and minimum of 4.7µF additional tantalum or other low ESR capacitor.

$EXTV_{CC}$ (Pin 30): External Power Input to an Internal Switch. This switch closes and supplies $INTV_{CC,}$ bypassing the internal low dropout regulator whenever $EXTV_{CC}$ is higher than 4.7V. See $EXTV_{CC}$ Connection in the Applications Information section. Do not exceed 7V on this pin and ensure $V_{EXTVCC} \leq V_{INTVCC}$.

V_{IN} (Pin 32): Main Supply Pin. Should be closely decoupled to the IC's signal ground pin.

PGOOD (Pin 36): Open-Drain Logic Output. PGOOD is pulled to ground when the voltage on the EAIN pin is not within ±10% of its set point.

FUNCTIONAL DIAGRAM



OPERATION (Refer to Functional Diagram)

Main Control Loop

The LTC3719 uses a constant frequency, current mode step-down architecture with the two output stages operating 180 degrees out of phase. During normal operation, each top MOSFET is turned on when the clock for that channel sets the RS latch, and turned off when the main current comparator, I_1, resets the RS latch. The peak inductor current at which I_1 resets the RS latch is controlled by the voltage on the I_{TH} pin, which is the output of error amplifier EA. The EAIN pin receives the voltage feedback signal, which is compared to the internal reference voltage by the EA. When the load current increases, it causes a slight decrease in V_{EAIN} relative to the 0.6V reference, which in turn causes the I_{TH} voltage to increase until the average inductor current matches the new load current. After the top MOSFET has turned off, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by current comparator I_2, or the beginning of the next cycle.

The top MOSFET drivers are biased from floating bootstrap capacitor C_B, which normally is recharged during each off cycle through an external diode when the top MOSFET turns off. As V_{IN} decreases to a voltage close to V_{OUT}, the loop may enter dropout and attempt to turn on the top MOSFET continuously. The dropout detector detects this and forces the top MOSFET off for about 500ns every tenth cycle to allow C_B to recharge.

The main control loop is shut down by pulling the RUN/SS pin low. Releasing RUN/SS allows an internal 1.2μA current source to charge soft-start capacitor C_{SS}. When C_{SS} reaches 1.5V, the main control loop is enabled with the I_{TH} voltage clamped at approximately 30% of its maximum value. As C_{SS} continues to charge, the I_{TH} pin voltage is gradually released allowing normal, full-current operation.

Low Current Operation

The FCB pin selects between *two* modes of low current operation. When the FCB pin voltage is below 0.6V, the controller forces continuous PWM current mode operation. In this mode, the top and bottom MOSFETs are alternately turned on to maintain the output voltage independent of direction of inductor current. When the FCB pin is below V_{INTVCC} – 2V but greater than 0.6V, the controller enters Burst Mode operation. Burst Mode operation sets a minimum output current level before inhibiting the top switch and turns off the synchronous MOSFET(s) when the inductor current goes negative. This combination of requirements will, at low currents, force the I_{TH} pin below a voltage threshold that will temporarily inhibit turn-on of both output MOSFETs until the output voltage drops. There is 60mV of hysteresis in the burst comparator B tied to the I_{TH} pin. This hysteresis produces output signals to the MOSFETs that turn them on for several cycles, followed by a variable "sleep" interval depending upon the load current. The resultant output voltage ripple is held to a very small value by having the hysteretic comparator after the error amplifier gain block.

Constant Frequency Operation

When the FCB pin is tied to $INTV_{CC}$, Burst Mode operation is disabled and a forced minimum peak output current requirement is removed. This provides constant frequency, discontinuous (preventing reverse inductor current) current operation over the widest possible output current range. This constant frequency operation is not as efficient as Burst Mode operation, but does provide a lower noise, constant frequency operating mode down to approximately 1% of designed maximum output current.

Continuous Current (PWM) Operation

Tying the FCB pin to ground will force continuous current operation. This is the least efficient operating mode, but may be desirable in certain applications. The output can source or sink current in this mode. When sinking current while in forced continuous operation, current will be forced back into the main power supply potentially boosting the input supply to dangerous voltage levels—BEWARE!

OPERATION (Refer to Functional Diagram)

Frequency Synchronization

The phase-locked loop allows the internal oscillator to be synchronized to an external source via the PLLIN pin. The output of the phase detector at the PLLFLTR pin is also the DC frequency control input of the oscillator that operates over a 140kHz to 310kHz range corresponding to a DC voltage input from 0V to 2.4V. When locked, the PLL aligns the turn on of the top MOSFET to the rising edge of the synchronizing signal. When PLLIN is left open, the PLLFLTR pin goes low, forcing the oscillator to minimum frequency.

Input capacitance ESR requirements and efficiency losses are substantially reduced because the peak current drawn from the input capacitor is effectively divided by two and power loss is proportional to the RMS current squared. A two stage, single output voltage implementation can reduce input path power loss by 75% and radically reduce the required RMS current rating of the input capacitor(s).

$INTV_{CC}/EXTV_{CC}$ Power

Power for the top and bottom MOSFET drivers and most of the IC circuitry is derived from $INTV_{CC}$. When the $EXTV_{CC}$ pin is left open, an internal 5V low dropout regulator supplies $INTV_{CC}$ power. If the $EXTV_{CC}$ pin is taken above 4.8V, the 5V regulator is turned off and an internal switch is turned on connecting $EXTV_{CC}$ to $INTV_{CC}$. This allows the $INTV_{CC}$ power to be derived from a high efficiency external source such as the output of the regulator itself or a secondary winding, as described in the Applications Information section. An external Schottky diode can be used to minimize the voltage drop from $EXTV_{CC}$ to $INTV_{CC}$ in applications requiring greater than the specified $INTV_{CC}$ current. Voltages up to 7V can be applied to $EXTV_{CC}$ for additional gate drive capability.

Differential Amplifier

This controller includes a true unity-gain differential amplifier. Sensing both V_{OUT}^+ and V_{OUT}^- benefits regulation in high current applications and/or applications having electrical interconnection losses. The amplifier is a unity-gain stable, 2MHz gain-bandwidth, >120dB open-loop gain design. The amplifier has an output slew rate of 5V/µs and is capable of driving capacitive loads with an output RMS current typically up to 25mA. The amplifier is not capable of sinking current and therefore must be resistively loaded to do so.

Output Overvoltage Protection

An overvoltage comparator, 0V, guards against transient overshoots (>10%) as well as other more serious conditions that may overvoltage the output. In this case, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared.

Power Good (PGOOD)

The PGOOD pin is connected to the drain of an internal MOSFET. The MOSFET turns on when the output voltage is not within ±10% of its nominal output level as determined by the feedback divider. When the output is within ±10% of its nominal value, the MOSFET is turned off within 10µs and the PGOOD pin should be pulled up by an external resistor to a source of up to 7V.

Short-Circuit Detection

The RUN/SS capacitor is used initially to limit the inrush current from the input power source. Once the controllers have been given time, as determined by the capacitor on the RUN/SS pin, to charge up the output capacitors and provide full-load current, the RUN/SS capacitor is then used as a short-circuit timeout circuit. If the output voltage falls to less than 70% of its nominal output voltage the RUN/SS capacitor begins discharging assuming that the output is in a severe overcurrent and/or short-circuit condition. If the condition lasts for a long enough period as determined by the size of the RUN/SS capacitor, the controller will be shut down until the RUN/SS pin voltage is recycled. This built-in latchoff can be overidden by providing a current >5µA at a compliance of 5V to the RUN/SS pin. This current shortens the soft-start period but also prevents net discharge of the RUN/SS capacitor during a severe overcurrent and/or short-circuit condition. Foldback current limiting is activated when the output voltage falls below 70% of its nominal level whether or not the short-circuit latchoff circuit is enabled.

APPLICATIONS INFORMATION

The basic LTC3719 application circuit is shown in Figure 1 on the first page. External component selection begins with the selection of the inductors based on ripple current requirements and continues with the current sensing resistors using the calculated peak inductor current and/or maximum current limit. Next, the power MOSFETs, D1 and D2 are selected. The operating frequency and the inductor are chosen based mainly on the amount of ripple current. Finally, C_{IN} is selected for its ability to handle the input ripple current (that PolyPhase™ operation minimizes) and C_{OUT} is chosen with low enough ESR to meet the output ripple voltage and load step specifications (also minimized with PolyPhase). Current mode architecture provides inherent current sharing between output stages. The circuit shown in Figure 1 can be configured for operation up to an input voltage of 28V (limited by the external MOSFETs). Current mode control allows the ability to connect the two output stages to two *different* input power supply rails. A heavy output load can take some power from *each* input supply according to the selection of the R_{SENSE} resistors.

R_{SENSE} Selection For Output Current

$R_{SENSE1,2}$ are chosen based on the required peak output current. The LTC3719 current comparator has a maximum threshold of 75mV/R_{SENSE} and an input common mode range of SGND to 1.1(INTV_{CC}). The current comparator threshold sets the peak inductor current, yielding a maximum average output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current, ΔI_L.

Assuming a common input power source for each output stage and allowing a margin for variations in the LTC3719 and external component values yields:

$$R_{SENSE} = N\frac{50mV}{I_{MAX}}$$

where N = 2 for 2 phase. For more than 2 phase use the LTC1629-6 plus the LTC3719.

Operating Frequency

The LTC3719 uses a constant frequency, phase-lockable architecture with the frequency determined by an internal capacitor. This capacitor is charged by a fixed current plus an additional current which is proportional to the voltage applied to the PLLFLTR pin. Refer to Phase-Locked Loop and Frequency Synchronization for additional information.

A graph for the voltage applied to the PLLFLTR pin vs frequency is given in Figure 2. As the operating frequency is increased the gate charge losses will be higher, reducing efficiency (see Efficiency Considerations). The maximum switching frequency is approximately 310kHz.

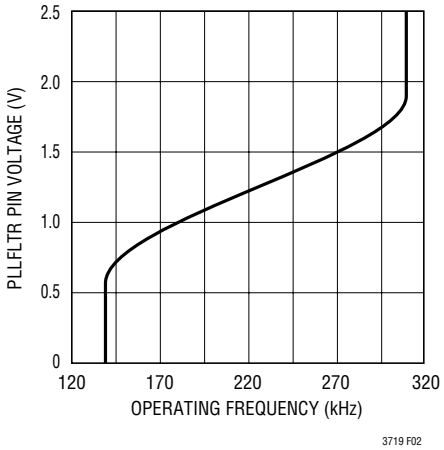


Figure 2. Operating Frequency vs $V_{PLLFLTR}$

Inductor Value Calculation and Output Ripple Current

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. So why would anyone ever choose to operate at lower frequencies with larger components? The answer is efficiency. A higher frequency generally results in lower efficiency because MOSFET gate charge and transition losses increase directly with frequency. In addition to this basic tradeoff, the effect of inductor value on ripple current and low current operation must also be considered. The PolyPhase approach reduces both input and output ripple currents while optimizing individual output stages to run at a lower fundamental frequency, enhancing efficiency.

The inductor value has a direct effect on ripple current. The inductor ripple current ΔI_L per individual section, N, decreases with higher inductance or frequency and increases with higher V_{IN} or V_{OUT}:

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APPLICATIONS INFORMATION

$$\Delta I_L = \frac{V_{OUT}}{f \bullet L}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where f is the individual output stage operating frequency.

In a 2-phase converter, the net ripple current seen by the output capacitor is much smaller than the individual inductor ripple currents due to ripple cancellation. The details on how to calculate the net output ripple current can be found in Application Note 77.

Figure 3 shows the net ripple current seen by the output capacitors for 1- and 2-phase configurations. The output ripple current is plotted for a fixed output voltage as the duty factor is varied between 10% and 90% on the x-axis. The output ripple current is normalized against the inductor ripple current at zero duty factor. The graph can be used in place of tedious calculations, simplifying the design process.

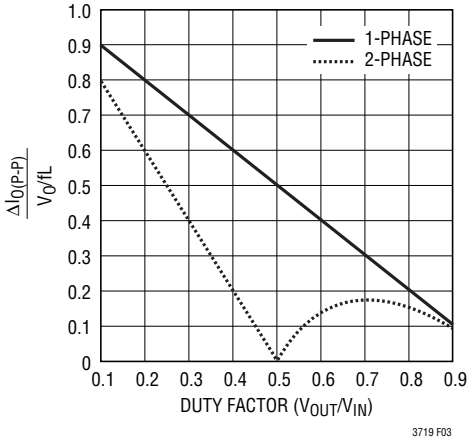

Figure 3. Normalized Output Ripple Current vs Duty Factor [$I_{RMS} \approx 0.3\ (\Delta I_{O(P-P)})$]

Accepting larger values of ΔI_L allows the use of low inductances, but can result in higher output voltage ripple. A reasonable starting point for setting ripple current is $\Delta I_L = 0.4(I_{OUT})/2$, where I_{OUT} is the total load current. Remember, the maximum ΔI_L occurs at the maximum input voltage. The individual inductor ripple currents are determined by the inductor, input and output voltages.

Inductor Core Selection

Once the values for L1 and L2 are known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy, or Kool Mμ® cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductor type selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. *Do not allow the core to saturate!*

Molypermalloy (from Magnetics, Inc.) is a very good, low loss core material for toroids, but it is more expensive than ferrite. A reasonable compromise from the same manufacturer is Kool Mμ. Toroids are very space efficient, especially when you can use several layers of wire. Because they lack a bobbin, mounting is more difficult. However, designs for surface mount are available which do not increase the height significantly.

Power MOSFET, D1 and D2 Selection

Two external power MOSFETs must be selected for each output stage with the LTC3719: one N-channel MOSFET for the top (main) switch, and one N-channel MOSFET for the bottom (synchronous) switch.

The peak-to-peak drive levels are set by the $INTV_{CC}$ voltage. This voltage is typically 5V during start-up (see $EXTV_{CC}$ Pin Connection). Consequently, logic-level threshold MOSFETs must be used in most applications. The only exception is if low input voltage is expected (V_{IN} < 5V); then, sublogic-level threshold MOSFETs ($V_{GS(TH)}$ < 1V) should be used. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; most of the logic-level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the "ON" resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS}, input voltage and maximum output current. When the

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APPLICATIONS INFORMATION

LTC3719 is operating in continuous mode the duty factors for the top and bottom MOSFETs of each output stage are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Synchronous Switch Duty Cycle} = \left(\frac{V_{IN} - V_{OUT}}{V_{IN}}\right)$$

The MOSFET power dissipations at maximum output current are given by:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}\left(\frac{I_{MAX}}{2}\right)^2(1+\delta)R_{DS(ON)} + k(V_{IN})^2\left(\frac{I_{MAX}}{2}\right)(C_{RSS})(f)$$

$$P_{SYNC} = \frac{V_{IN} - V_{OUT}}{V_{IN}}\left(\frac{I_{MAX}}{2}\right)^2(1+\delta)R_{DS(ON)}$$

where δ is the temperature dependency of $R_{DS(ON)}$ and k is a constant inversely related to the gate drive current.

Both MOSFETs have I^2R losses but the topside N-channel equation includes an additional term for transition losses, which peak at the highest input voltage. For $V_{IN} < 20V$ the high current efficiency generally improves with larger MOSFETs, while for $V_{IN} > 20V$ the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{RSS} actual provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during a short-circuit when the synchronous switch is on close to 100% of the period.

The term $(1 + \delta)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve, but $\delta = 0.005/°C$ can be used as an approximation for low voltage MOSFETs. C_{RSS} is usually specified in the MOSFET characteristics. The constant k = 1.7 can be used to estimate the contributions of the two terms in the main switch dissipation equation.

The Schottky diodes, D1 and D2 shown in Figure 1 conduct during the dead-time between the conduction of the two large power MOSFETs. This helps prevent the body diode of the bottom MOSFET from turning on, storing charge during the dead-time, and requiring a reverse recovery period which would reduce efficiency. A 1A to 3A Schottky (depending on output current) diode is generally a good compromise for both regions of operation due to the relatively small average current. Larger diodes result in additional transition losses due to their larger junction capacitance.

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of each top N-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. A low ESR input capacitor sized for the maximum RMS current must be used. The details of a closed form equation can be found in Application Note 77. Figure 4 shows the input capacitor ripple current for a 2-phase configuration with the output voltage fixed and input voltage varied. The input ripple current is normalized against the DC output current. The graph can be used in place of tedious calculations. The minimum input ripple current can be achieved when the input voltage is twice the output voltage.

In the graph of Figure 4, the 2-phase local maximum input RMS capacitor currents are reached when:

$$\frac{V_{OUT}}{V_{IN}} = \frac{2k-1}{4}$$

where k = 1, 2

These worst-case conditions are commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the capacitor manufacturer if there is any question.

APPLICATIONS INFORMATION

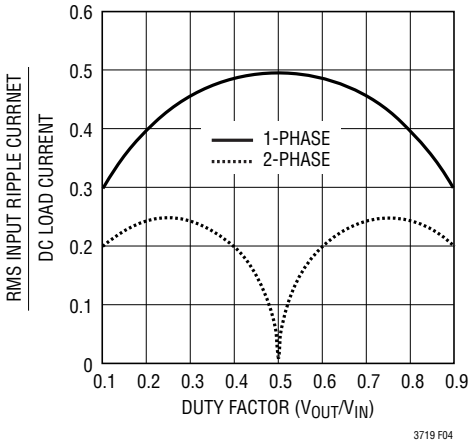

Figure 4. Normalized RMS Input Ripple Current vs Duty Factor for 1 and 2 Output Stages

It is important to note that the efficiency loss is proportional to the input RMS current *squared* and therefore a 2-phase implementation results in 75% less power loss when compared to a single phase design. Battery/input protection fuse resistance (if used), PC board trace and connector resistance losses are also reduced by the reduction of the input ripple current in a 2-phase system. The required amount of input capacitance is further reduced by the factor, 2, due to the effective increase in the frequency of the current pulses.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically once the ESR requirement has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirements. The steady state output ripple (ΔV_{OUT}) is determined by:

$$\Delta V_{OUT} \approx \Delta I_{RIPPLE}\left(ESR + \frac{1}{16fC_{OUT}}\right)$$

Where f = operating frequency of each stage, C_{OUT} = output capacitance and ΔI_{RIPPLE} = combined inductor ripple currents.

The output ripple varies with input voltage since ΔI_L is a function of input voltage. The output ripple will be less than 50mV at max V_{IN} with $\Delta I_L = 0.4I_{OUT(MAX)}/2$ assuming:

C_{OUT} required ESR < $4(R_{SENSE})$ and

$C_{OUT} > 1/(16f)(R_{SENSE})$

The emergence of very low ESR capacitors in small, surface mount packages makes very physically small implementations possible. The ability to externally compensate the switching regulator loop using the I_{TH} pin(OPTI-LOOP compensation) allows a much wider selection of output capacitor types. OPTI-LOOP compensation effectively removes constraints on output capacitor ESR. The impedance characteristics of each capacitor type are significantly different than an ideal capacitor and therefore require accurate modeling or bench evaluation during design.

Manufacturers such as Nichicon, United Chemicon and Sanyo should be considered for high performance through-hole capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo and the Panasonic SP surface mount types have the lowest (ESR)(size) product of any aluminum electrolytic at a somewhat higher price. An additional ceramic capacitor in parallel with OS-CON type capacitors is recommended to reduce the inductance effects.

In surface mount applications, multiple capacitors may have to be paralleled to meet the ESR or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. New special polymer surface mount capacitors offer very low ESR also but have much lower capacitive density per unit volume. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. Several excellent choices are the AVX TPS, AVX TPSV or the KEMET T510 series of surface mount tantalums, available in case heights ranging from 2mm to 4mm. Other capacitor types include Sanyo OS-CON, POSCAPs, Panasonic SP caps, Nichicon PL series and Sprague 595D series. Consult the manufacturer for other specific recommendations. A combination of capacitors will often result in maximizing performance and minimizing overall cost and size.

APPLICATIONS INFORMATION

$INTV_{CC}$ Regulator

An internal P-channel low dropout regulator produces 5V at the $INTV_{CC}$ pin from the V_{IN} supply pin. The $INTV_{CC}$ regulator powers the drivers and internal circuitry of the LTC3719. The $INTV_{CC}$ pin regulator can supply up to 50mA peak and must be bypassed to power ground with a minimum of 4.7µF tantalum or electrolytic capacitor. An additional 1µF ceramic capacitor placed very close to the IC is recommended due to the extremely high instantaneous currents required by the MOSFET gate drivers.

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC3719 to be exceeded. The supply current is dominated by the gate charge supply current, in addition to the current drawn from the differential amplifier output. The gate charge is dependent on operating frequency as discussed in the Efficiency Considerations section. The supply current can either be supplied by the internal 5V regulator or via the $EXTV_{CC}$ pin. When the voltage applied to the $EXTV_{CC}$ pin is less than 4.7V, all of the $INTV_{CC}$ load current is supplied by the internal 5V linear regulator. Power dissipation for the IC is higher in this case by $(I_{IN})(V_{IN} – INTV_{CC})$ and efficiency is lowered. The junction temperature can be estimated by using the equations given in Note 1 of the Electrical Characteristics. For example, the LTC3719 V_{IN} current is limited to less than 24mA from a 24V supply:

$$T_J = 70°C + (24mA)(24V)(85°C/W) = 119°C$$

Use of the $EXTV_{CC}$ pin reduces the junction temperature to:

$$T_J = 70°C + (24mA)(5V)(85°C/W) = 80.2°C$$

The input supply current should be measured while the controller is operating in continuous mode at maximum V_{IN} and the power dissipation calculated in order to prevent the maximum junction temperature from being exceeded.

$EXTV_{CC}$ Connection

The LTC3719 contains an internal P-channel MOSFET switch connected between the $EXTV_{CC}$ and $INTV_{CC}$ pins. When the voltage applied to $EXTV_{CC}$ rises above 4.7V, the internal regulator is turned off and an internal switch closes, connecting the $EXTV_{CC}$ pin to the $INTV_{CC}$ pin thereby supplying internal and MOSFET gate driving power to the IC. The switch remains closed as long as the voltage applied to $EXTV_{CC}$ remains above 4.5V. This allows the MOSFET driver and control power to be derived from a separate 5V supply during normal operation ($4.7V < V_{EXTVCC} < 7V$) and from the internal regulator when the external 5V supply is not available. Do not apply greater than 7V to the $EXTV_{CC}$ pin and ensure that $EXTV_{CC} < V_{IN} + 0.3V$ when using the application circuits shown. If an external voltage source is applied to the $EXTV_{CC}$ pin when the V_{IN} supply is not present, a diode can be placed in series with the LTC3719's V_{IN} pin and a Schottky diode between the $EXTV_{CC}$ and the V_{IN} pin, to prevent current from backfeeding V_{IN}.

Topside MOSFET Driver Supply (C_B, D_B) (Refer to Functional Diagram)

External bootstrap capacitors C_{B1} and C_{B2} connected to the BOOST1 and BOOST2 pins supply the gate drive voltages for the topside MOSFETs. Capacitor C_B in the Functional Diagram is charged though diode D_B from $INTV_{CC}$ when the SW pin is low. When the topside MOSFET turns on, the driver places the C_B voltage across the gate-source of the desired MOSFET. This enhances the MOSFET and turns on the topside switch. The switch node voltage, SW, rises to V_{IN} and the BOOST pin rises to $V_{IN} + V_{INTVCC}$. The value of the boost capacitor C_B needs to be 30 to 100 times that of the total input capacitance of the topside MOSFET(s). The reverse breakdown of D_B must be greater than $V_{IN(MAX)}$.

The final arbiter when defining the best gate drive amplitude level will be the input supply current. If a change is made that decreases input current, the efficiency has improved. If the input current does not change then the efficiency has not changed either.

APPLICATIONS INFORMATION

Output Voltage

The LTC3719 has a true remote voltage sense capablity. The sensing connections should be returned from the load back to the differential amplifier's inputs through a common, tightly coupled pair of PC traces. The differential amplifier corrects for DC drops in both the power and ground paths. The differential amplifier output signal is divided down and compared with the internal precision 0.6V voltage reference by the error amplifier.

Output Voltage Programming

The output voltage is digitally programmed as defined in Table 1 using the VID0 to VID4 logic input pins. The VID logic inputs program a precision, 0.25% internal feedback resistive divider. The LTC3719 has an output voltage range of 0.8V to 1.55V in 25mV steps.

Between the ATTENOUT pin and ground is a variable resistor, R1, whose value is controlled by the five VID input pins (VID0 to VID4). Another resistor, R2, between the ATTENIN and the ATTENOUT pins completes the resistive divider. The output voltage is thus set by the ratio of (R1 + R2) to R1.

Each VID digital input is pulled up by a 40k resistor in series with a diode from V_{BIAS}. Therefore, it must be grounded to get a digital low input, and can be either floated or connected to V_{BIAS} to get a digital high input. The series diode is used to prevent the digital inputs from being damaged or clamped if they are driven higher than V_{BIAS}. The digital inputs accept CMOS voltage levels.

V_{BIAS} is the supply voltage for the VID section. It is normally connected to $INTV_{CC}$ but can be driven from other sources. If it is driven from another source, that source *must* be in the range of 2.7V to 5.5V and *must* be alive prior to enabling the LTC3719.

Table 1. VID Output Voltage Programming

CODE	VID4	VID3	VID2	VID1	VID0	OUTPUT
00000	GND	GND	GND	GND	GND	1.550
00001	GND	GND	GND	GND	Float	1.525
00010	GND	GND	GND	Float	GND	1.500
00011	GND	GND	GND	Float	Float	1.475
00100	GND	GND	Float	GND	GND	1.450
00101	GND	GND	Float	GND	Float	1.425
00110	GND	GND	Float	Float	GND	1.400
00111	GND	GND	Float	Float	Float	1.375
01000	GND	Float	GND	GND	GND	1.350
01001	GND	Float	GND	GND	Float	1.325
01010	GND	Float	GND	Float	GND	1.300
01011	GND	Float	GND	Float	Float	1.275
01100	GND	Float	Float	GND	GND	1.250
01101	GND	Float	Float	GND	Float	1.225
01110	GND	Float	Float	Float	GND	1.200
01111	GND	Float	Float	Float	Float	1.175
10000	Float	GND	GND	GND	GND	1.150
10001	Float	GND	GND	GND	Float	1.125
10010	Float	GND	GND	Float	GND	1.100
10011	Float	GND	GND	Float	Float	1.075
10100	Float	GND	Float	GND	GND	1.050
10101	Float	GND	Float	GND	Float	1.025
10110	Float	GND	Float	Float	GND	1.000
10111	Float	GND	Float	Float	Float	0.975
11000	Float	Float	GND	GND	GND	0.950
11001	Float	Float	GND	GND	Float	0.925
11010	Float	Float	GND	Float	GND	0.900
11011	Float	Float	GND	Float	Float	0.875
11100	Float	Float	Float	GND	GND	0.850
11101	Float	Float	Float	GND	Float	0.825
11110	Float	Float	Float	Float	GND	0.800
11111	Float	Float	Float	Float	Float	Shutdown

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Soft-Start/Run Function

The RUN/SS pin provides three functions: 1) Run/Shutdown, 2) soft-start and 3) a defeatable short-circuit latchoff timer. Soft-start reduces the input power sources' surge currents by gradually increasing the controller's current limit $I_{TH(MAX)}$. The latchoff timer prevents very short, extreme load transients from tripping the overcurrent latch. A small pull-up current (>5µA) supplied to the RUN/SS pin will prevent the overcurrent latch from operating. The following explanation describes how the functions operate.

An internal 1.2µA current source charges up the soft-start capacitor, C_{SS}. When the voltage on RUN/SS reaches 1.5V, the controller is permitted to start operating. As the voltage on RUN/SS increases from 1.5V to 3.0V, the internal current limit is increased from 25mV/R_{SENSE} to 75mV/R_{SENSE}. The output current limit ramps up slowly, taking an additional 1.4s/µF to reach full current. The output current thus ramps up slowly, reducing the starting surge current required from the input power supply. If RUN/SS has been pulled all the way to ground there is a delay before starting of approximately:

$$t_{DELAY} = \frac{1.5V}{1.2\mu A} C_{SS} = \left(1.25s/\mu F\right) C_{SS}$$

The time for the output current to ramp up is then:

$$t_{IRAMP} = \frac{3V - 1.5V}{1.2\mu A} C_{SS} = \left(1.25s/\mu F\right) C_{SS}$$

By pulling the RUN/SS pin below 0.8V the LTC3719 is put into low current shutdown (I_Q < 40µA). The RUN/SS pins can be driven directly from logic as shown in Figure 5. Diode D1 in Figure 5 reduces the start delay but allows C_{SS} to ramp up slowly providing the soft-start function. The RUN/SS pin has an internal 6V zener clamp (see Functional Diagram).

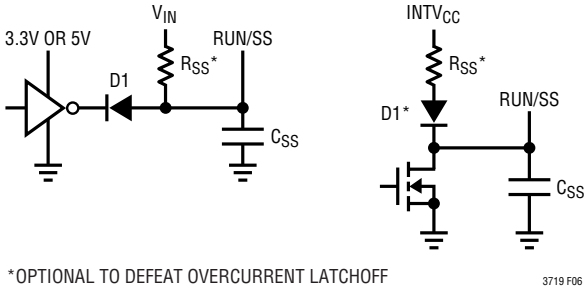

Figure 5. RUN/SS Pin Interfacing

Fault Conditions: Overcurrent Latchoff

The RUN/SS pin also provides the ability to latch off the controllers when an overcurrent condition is detected. The RUN/SS capacitor, C_{SS}, is used initially to limit the inrush current of both controllers. After the controllers have been started and been given adequate time to charge up the output capacitors and provide full load current, the RUN/SS capacitor is used for a short-circuit timer. If the output voltage falls to less than 70% of its nominal value after C_{SS} reaches 4.1V, C_{SS} begins discharging on the assumption that the output is in an overcurrent condition. If the condition lasts for a long enough period as determined by the size of the C_{SS}, the controller will be shut down until the RUN/SS pin voltage is recycled. If the overload occurs during start-up, the time can be approximated by:

$$t_{LO1} \approx (C_{SS} \bullet 0.6V)/(1.2\mu A) = 5 \bullet 10^5 (C_{SS})$$

If the overload occurs after start-up, the voltage on C_{SS} will continue charging and will provide additional time before latching off:

$$t_{LO2} \approx (C_{SS} \bullet 3V)/(1.2\mu A) = 2.5 \bullet 10^6 (C_{SS})$$

This built-in overcurrent latchoff can be overridden by providing a pull-up resistor, R_{SS}, to the RUN/SS pin as shown in Figure 5. This resistance shortens the soft-start period and prevents the discharge of the RUN/SS capacitor during a severe overcurrent and/or short-circuit

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condition. When deriving the 5μA current from V_{IN} as in the figure, current latchoff is always defeated. The diode connecting this pull-up resistor to $INTV_{CC}$, as in Figure 5, eliminates any extra supply current during shutdown while eliminating the $INTV_{CC}$ loading from preventing controller start-up.

Why should you defeat current latchoff? During the prototyping stage of a design, there may be a problem with noise pickup or poor layout causing the protection circuit to latch off the controller. Defeating this feature allows troubleshooting of the circuit and PC layout. The internal short-circuit and foldback current limiting still remains active, thereby protecting the power supply system from failure. A decision can be made after the design is complete whether to rely solely on foldback current limiting or to enable the latchoff feature by removing the pull-up resistor.

The value of the soft-start capacitor C_{SS} may need to be scaled with output voltage, output capacitance and load current characteristics. The minimum soft-start capacitance is given by:

$$C_{SS} > (C_{OUT})(V_{OUT})(10^{-4})(R_{SENSE})$$

The minimum recommended soft-start capacitor of C_{SS} = 0.1μF will be sufficient for most applications.

Phase-Locked Loop and Frequency Synchronization

The LTC3719 has a phase-locked loop comprised of an internal voltage controlled oscillator and phase detector. This allows the top MOSFET turn-on to be locked to the rising edge of an external source. The frequency range of the voltage controlled oscillator is ±50% around the center frequency f_O. A voltage applied to the PLLFLTR pin of 1.2V corresponds to a frequency of approximately 220kHz. The nominal operating frequency range of the LTC3719 is 140kHz to 310kHz.

The phase detector used is an edge sensitive digital type which provides zero degrees phase shift between the external and internal oscillators. This type of phase detector will not lock up on input frequencies close to the harmonics of the VCO center frequency. The PLL hold-in range, Δf_H, is equal to the capture range, Δf_C:

$$\Delta f_H = \Delta f_C = \pm 0.5\ f_O \text{ (150kHz-300kHz)}$$

The output of the phase detector is a complementary pair of current sources charging or discharging the external filter network on the PLLFLTR pin. A simplified block diagram is shown in Figure 6.

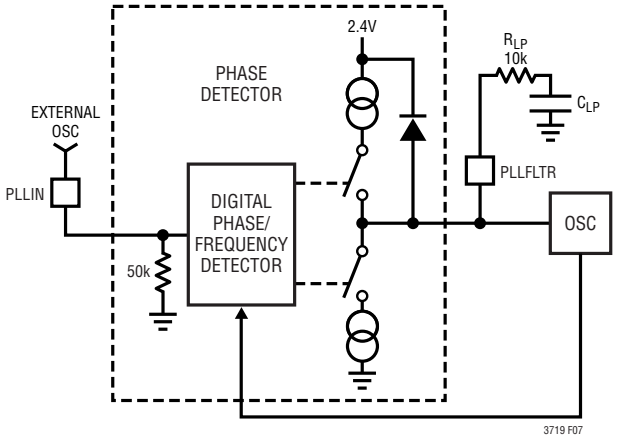

Figure 6. Phase-Locked Loop Block Diagram

If the external frequency (f_{PLLIN}) is greater than the oscillator frequency f_{OSC}, current is sourced continuously, pulling up the PLLFLTR pin. When the external frequency is less than f_{OSC}, current is sunk continuously, pulling down the PLLFLTR pin. If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. Thus the voltage on the PLLFLTR pin is adjusted until the phase and frequency of the external and internal oscillators are identical. At this stable operating point the phase comparator output is open and the filter capacitor C_{LP} holds the voltage. The LTC3719 PLLIN pin must be driven from a low impedance source such as a logic gate located close to the pin.

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The loop filter components (C_{LP}, R_{LP}) smooth out the current pulses from the phase detector and provide a stable input to the voltage controlled oscillator. The filter components C_{LP} and R_{LP} determine how fast the loop acquires lock. Typically R_{LP} =10k and C_{LP} is 0.01µF to 0.1µF.

Minimum On-Time Considerations

Minimum on-time, $t_{ON(MIN)}$, is the smallest time duration that the LTC3719 is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN}(f)}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the LTC3719 will begin to skip cycles resulting in variable frequency operation. The output voltage will continue to be regulated, but the ripple current and ripple voltage will increase.

The minimum on-time for the LTC3719 is generally less than 200ns. However, as the peak sense voltage decreases, the minimum on-time gradually increases. This is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger ripple current and voltage ripple.

If an application can operate close to the minimum on-time limit, an inductor must be chosen that has a low enough inductance to provide sufficient ripple amplitude to meet the minimum on-time requirement. *As a general rule, keep the inductor ripple current of each phase equal to or greater than 15% of $I_{OUT(MAX)}$ at $V_{IN(MAX)}$.*

FCB Pin Operation

The following table summarizes the possible states available on the FCB pin:

Table 2

FCB Pin	Condition
0V to 0.55V	Forced Continuous (Current Reversal Allowed—Burst Inhibited)
0.65V < V_{FCB} < 4.3V (typ)	Minimum Peak Current Induces Burst Mode Operation No Current Reversal Allowed
>4.8V	Burst Mode Operation Disabled Constant Frequency Mode Enabled No Current Reversal Allowed No Minimum Peak Current

Active Voltage Positioning

Active voltage positioning can be used to minimize peak-to-peak output voltage excursion under worst-case transient loading conditions. The open-loop DC gain of the control loop is reduced depending upon the maximum load step specifications. Active voltage positioning can easily be added to the LTC3719 by loading the I_{TH} pin with a resistive divider having a Thevenin equivalent voltage source equal to the midpoint operating voltage of the error amplifier, or 1.2V (see Figure 7).

The resistive load reduces the DC loop gain while maintaining the linear control range of the error amplifier. The worst-case peak-to-peak output voltage deviation due to transient loading can theoretically be reduced to half or alternatively the amount of output capacitance can be reduced for a particular application. A complete explanation is included in Design Solutions 10 or the LTC1736 data sheet. (See www.linear-tech.com)

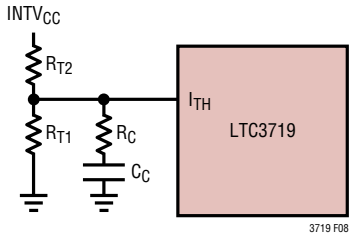

Figure 7. Active Voltage Positioning Applied to the LTC3719

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Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

%Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC3719 circuits: 1) I^2R losses, 2) Topside MOSFET transition losses, 3) $INTV_{CC}$ regulator current and 4) LTC3719 V_{IN} current (including loading on the differential amplifier output).

1) I^2R losses are predicted from the DC resistances of the fuse (if used), MOSFET, inductor, current sense resistor, and input and output capacitor ESR. In continuous mode the average output current flows through L and R_{SENSE}, but is "chopped" between the topside MOSFET and the synchronous MOSFET. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L, R_{SENSE} and ESR to obtain I^2R losses. For example, if each $R_{DS(ON)} = 10m\Omega$, $R_L = 10m\Omega$, and $R_{SENSE} = 5m\Omega$, then the total resistance is $25m\Omega$. This results in losses ranging from 2% to 8% as the output current increases from 3A to 15A per output stage for a 5V output, or a 3% to 12% loss per output stage for a 3.3V output. Efficiency varies as the inverse square of V_{OUT} for the same external components and output power level. The combined effects of increasingly lower output voltages and higher currents required by high performance digital systems is not doubling but quadrupling the importance of loss terms in the switching regulator system!

2) Transition losses apply only to the topside MOSFET(s), and are significant only when operating at high input voltages (typically 12V or greater). Transition losses can be estimated from:

$$\text{Transition Loss} = (1.7)V_{IN}^2\left(\frac{I_{O(MAX)}}{2}\right)C_{RSS}f$$

3) $INTV_{CC}$ current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from $INTV_{CC}$ to ground. The resulting dQ/dt is a current out of $INTV_{CC}$ that is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} = (Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the topside and bottom side MOSFETs.

Supplying $INTV_{CC}$ power through the $EXTV_{CC}$ switch input from an output-derived source will scale the V_{IN} current required for the driver and control circuits by the ratio (Duty Factor)/(Efficiency). For example, in a 20V to 5V application, 10mA of $INTV_{CC}$ current results in approximately 3mA of V_{IN} current. This reduces the mid-current loss from 10% or more (if the driver was powered directly from V_{IN}) to only a few percent.

4) The V_{IN} current has two components: the first is the DC supply current given in the Electrical Characteristics table, which excludes MOSFET driver and control currents; the second is the current drawn from the differential amplifier output. V_{IN} current typically results in a small (<0.1%) loss.

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Other "hidden" losses such as copper trace and internal battery resistances can account for an additional 5% to 10% efficiency degradation in portable systems. It is very important to include these "system" level losses in the design of a system. The internal battery and input fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and a very low ESR at the switching frequency. A 50W supply will typically require a minimum of 200µF to 300µF of output capacitance having a maximum of 10mΩ to 20mΩ of ESR. The LTC3719 2-phase architecture typically halves the input and output capacitance requirements over competing solutions. Other losses including Schottky conduction losses during dead-time and inductor core losses generally account for less than 2% total additional loss.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to ΔI_{LOAD}(ESR), where ESR is the effective series resistance of C_{OUT} (ΔI_{LOAD}) also begins to charge or discharge C_{OUT} generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem. *The availability of the I_{TH} pin not only allows optimization of control loop behavior but also provides a DC coupled and AC filtered closed loop response test point. The DC step, rise time, and settling at this test point truly reflects the closed loop response.* Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The I_{TH} external components shown in the Figure 1 circuit will provide an adequate starting point for most applications.

The I_{TH} series R_C-C_C filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.2 to 5 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be decided upon first because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of <2µs will produce output voltage and I_{TH} pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the Ith pin signal which is in the feedback loop and is the filtered and compensated control loop response. The gain of the loop will be increased by increasing R_C and the bandwidth of the loop will be increased by decreasing C_C. If R_C is increased by the same factor that C_C is decreased, the zero frequency will be kept the same, thereby keeping the phase the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance.

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Design Example

As a design example, assume V_{IN} = 5V (nominal), V_{IN} = 5.5V (max), V_{OUT} = 1.2V, I_{MAX} = 20A, T_A = 70°C and f = 300kHz.

The inductance value is chosen first based on a 30% ripple current assumption. The highest value of ripple current occurs at the maximum input voltage. Tie the FREQSET pin to the $INTV_{CC}$ pin for 300kHz operation. The minimum inductance for 30% ripple current is:

$$L \geq \frac{V_{OUT}}{f(\Delta L)}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

$$\geq \frac{1.2V}{(300kHz)(30\%)(10A)}\left(1-\frac{1.2V}{5.5V}\right)$$

$$\geq 1.04\mu H$$

A 1µH inductor will produce 31% ripple current. The peak inductor current will be the maximum DC value plus one half the ripple current, or 11.5A. The minimum on-time occurs at maximum V_{IN}:

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN} f} = \frac{1.2V}{(5.5V)(300kHz)} = 0.73\mu s$$

The R_{SENSE} resistors value can be calculated by using the maximum current sense voltage specification with some accomodation for tolerances:

$$R_{SENSE} = \frac{50mV}{11.5A} \approx 0.004\Omega$$

The power dissipation on the topside MOSFET can be easily estimated. Using a Siliconix Si4420DY for example; $R_{DS(ON)}$ = 0.013Ω, C_{RSS} = 300pF. At maximum input voltage with T_J (estimated) = 110°C at an elevated ambient temperature:

$$P_{MAIN} = \frac{1.2V}{5.5V}(10)^2\left[1+(0.005)(110°C-25°C)\right]$$
$$0.013\Omega + 1.7(5.5V)^2(10A)(300pF)$$
$$(300kHz) = 0.45W$$

The worst-case power disipated by the synchronous MOSFET under normal operating conditions at elevated ambient temperature and estimated 50°C junction temperature rise is:

$$P_{SYNC} = \frac{5.5V-1.2V}{5.5V}2(10A)^2(1.48)(0.013\Omega)$$
$$= 1.5W$$

A short-circuit to ground will result in a folded back current of about:

$$I_{SC} = \frac{25mV}{0.004\Omega} + \frac{1}{2}\left[\frac{200ns(5.5V)}{1\mu H}\right] = 6.8A$$

The worst-case power disipated by the synchronous MOSFET under short-circuit conditions at elevated ambient temperature and estimated 50°C junction temperature rise is:

$$P_{SYNC} = \frac{5.5V-1.2V}{5.5V}(6.8A)^2(1.48)(0.013\Omega)$$
$$= 696mW$$

which is less than normal, full-load conditions. Incidentally, since the load no longer dissipates power in the shorted condition, total system power dissipation is decreased by over 99%.

The duty factor for this application is:

$$DF = \frac{V_O}{V_{IN}} = \frac{1.2V}{5V} = 0.24$$

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Using Figure 4, the RMS ripple current will be:

$$I_{INRMS} = (20A)(0.25) = 5A_{RMS}$$

An input capacitor(s) with a $5A_{RMS}$ ripple current rating is required.

The output capacitor ripple current is calculated by using the inductor ripple already calculated for each inductor and multiplying by the factor obtained from Figure 3 along with the calculated duty factor. The output ripple in continuous mode will be highest at the maximum input voltage since the duty factor is <50%. The maximum output current ripple is:

$$\Delta I_{COUT} = \frac{V_{OUT}}{fL}(0.5) \text{ at } 24\% \text{ D F}$$

$$\Delta I_{COUTMAX} = \frac{1.2V}{(300kHz)(1.0\mu H)}0.5$$

$$= 2A_{P-P}$$

$$V_{OUTRIPPLE} = 20m\Omega(2A_{P-P}) = 40mV_{P-P}$$

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3719. Check the following in your layout:

1) Are the signal and power grounds separate? The signal ground traces should return to Pin 9 first. Connect Pin 9 to Pin 28 through a wide and straight trace. Then the signal ground joins the power ground plane beside Pin 28. It is recommended that the Pin 28 return to the (–) plates of C_{IN}.

2) Does the LTC3719 V_{OS}^+ pin connect to the point of load? Does the LTC3719 V_{OS}^- pin connect to the load return?

3) Are the SENSE$^-$ and SENSE$^+$ leads routed together with minimum PC trace spacing? The filter capacitors between SENSE$^+$ and SENSE$^-$ pin pairs should be as close as possible to the LTC3719. Ensure accurate current sensing with Kelvin connections at the current sense resistor. See Figure 8.

4) Does the (+) plate of C_{IN} connect to the drains of the topside MOSFETs as closely as possible? This capacitor provides the AC current to the MOSFETs. Keep the input current path formed by the input capacitor, top and bottom MOSFETs, and the Schottky diode on the same side of the PC board in a tight loop to minimize conducted and radiated EMI.

5) Is the $INTV_{CC}$ 1µF ceramic decoupling capacitor connected closely between $INTV_{CC}$ and the PGND pin? This capacitor carries the MOSFET driver peak currents. A small value is recommended to allow placement immediately adjacent to the IC.

6) Keep the switching nodes, SW1 (SW2), away from sensitive small-signal nodes. Ideally the switch nodes should be placed at the furthest point from the LTC3719.

7) Use a low impedance source such as a logic gate to drive the PLLIN pin and keep the lead as short as possible.

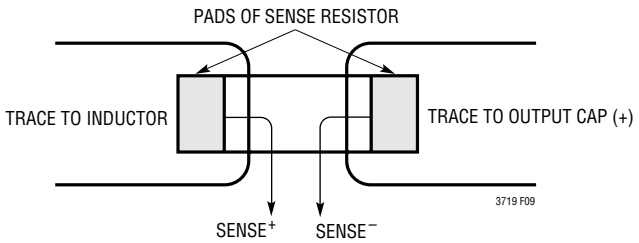

Figure 8. Proper Current Sense Connections

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The diagram in Figure 9 illustrates all branch currents in a 2-phase switching regulator. It becomes very clear after studying the current waveforms why it is critical to keep the high-switching-current paths to a small physical size. High electric and magnetic fields will radiate from these "loops" just as radio stations transmit signals. The output capacitor ground should return to the negative terminal of the input capacitor and not share a common ground path with any switched current paths. The left half of the circuit gives rise to the "noise" generated by a switching regulator. The ground terminations of the sychronous MOSFETs and Schottky diodes should return to the negative plate(s) of the input capacitor(s) with a short isolated PC trace since very high switched currents are present. A separate isolated path from the negative plate(s) of the input capacitor(s) should be used to tie in the IC power ground pin (PGND) and the signal ground pin (SGND). This technique keeps inherent signals generated by high current pulses from taking alternate current paths that have finite impedances during the total period of the switching regulator. External OPTI-LOOP compensation allows overcompensation for PC layouts which are not optimized but this is not the recommended design procedure.

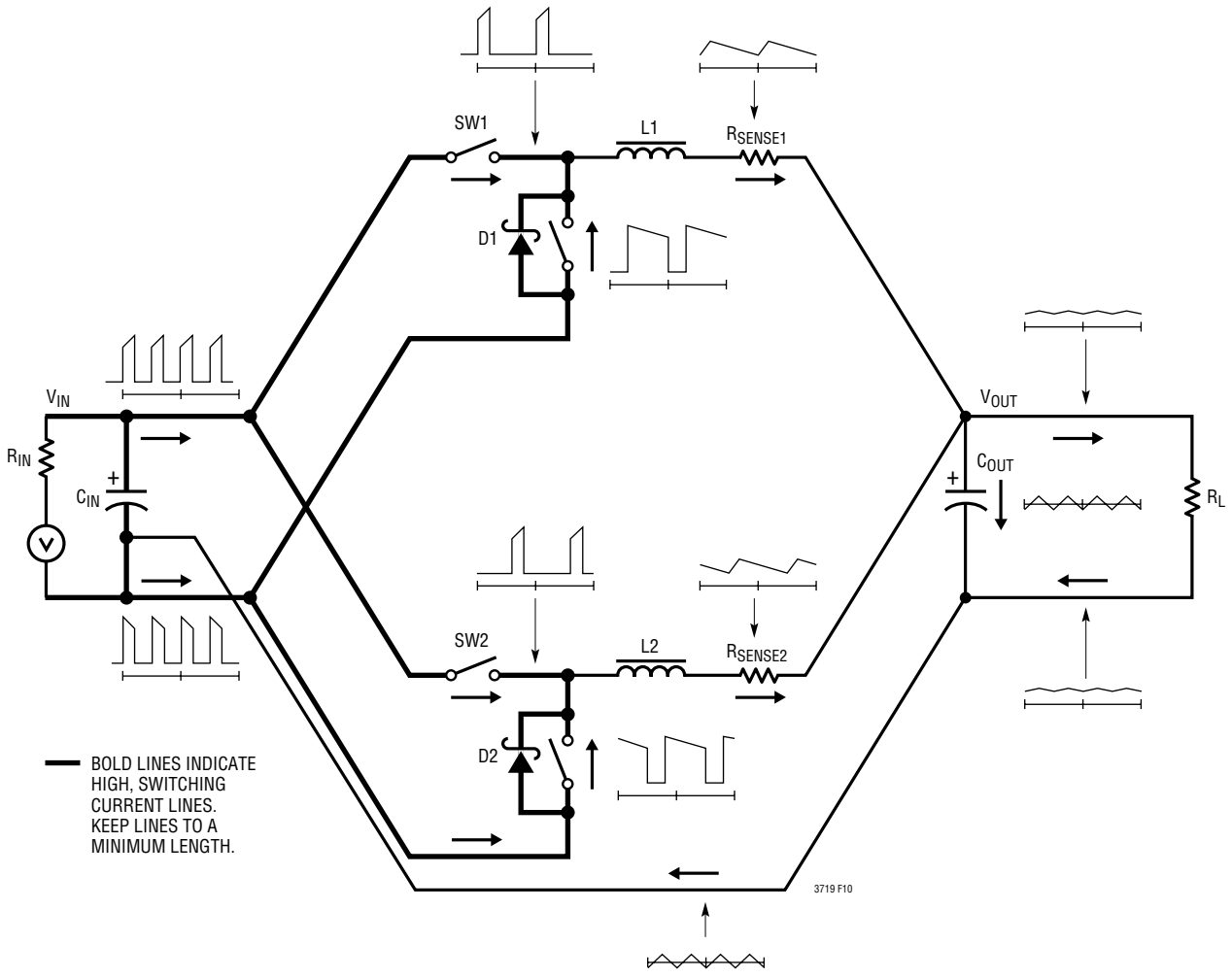

Figure 9. Instantaneous Current Path Flow in a Multiple Phase Switching Regulator

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Simplified Visual Explanation of How a 2-Phase Controller Reduces Both Input and Output RMS Ripple Current

A multiphase power supply significantly reduces the amount of ripple current in both the input and output capacitors. The RMS input ripple current is divided by, and the effective ripple frequency is multiplied up by the number of phases used (assuming that the input voltage is greater than the number of phases used times the output voltage). The output ripple amplitude is also reduced by, and the effective ripple frequency is increased by the number of phases used. Figure 10 graphically illustrates the principle.

The worst-case RMS ripple current for a single stage design peaks at an input voltage of twice the output voltage. The worst-case RMS ripple current for a two stage design results in peak outputs of 1/4 and 3/4 of input voltage. When the RMS current is calculated, higher effective duty factor results and the peak current levels are divided as long as the currents in each stage are balanced. Refer to Application Note 19 for a detailed description of how to calculate RMS current for the single stage switching regulator. Figures 3 and 4 illustrate how the input and output currents are reduced by using an additional phase. The input current peaks drop in half and the frequency is doubled for this 2-phase converter. The input capacity requirement is thus reduced theoretically by a factor of four! Ceramic input capacitors with their unbeatably low ESR characteristics can be used.

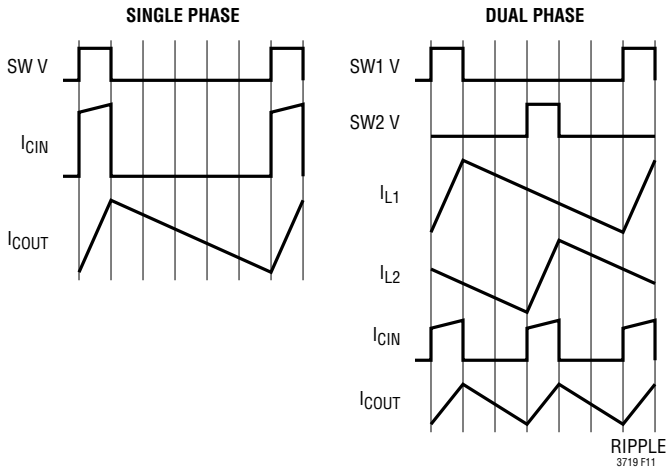

Figure 10. Single and 2-Phase Current Waveforms

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Figure 4 illustrates the RMS input current drawn from the input capacitance vs the duty cycle as determined by the ratio of input and output voltage. The peak input RMS current level of the single phase system is reduced by 50% in a 2-phase solution due to the current splitting between the two stages.

An interesting result of the 2-phase solution is that the V_{IN} which produces worst-case ripple current for the input capacitor, $V_{OUT} = V_{IN}/2$, in the single phase design produces zero input current ripple in the 2-phase design.

The output ripple current is reduced significantly when compared to the single phase solution using the same inductance value because the V_{OUT}/L discharge current term from the stage that has its bottom MOSFET on subtracts current from the $(V_{IN} – V_{OUT})/L$ charging current resulting from the stage which has its top MOSFET on. The output ripple current is:

$$\Delta I_{RIPPLE} = \frac{2V_{OUT}}{fL}\left[\frac{\left|1-2D\right|\left(1-D\right)}{\left|1-2D\right|+1}\right]$$

where D is duty factor.

The input and output ripple frequency is increased by the number of stages used, reducing the output capacity requirements. When V_{IN} is approximately equal to $2(V_{OUT})$ as illustrated in Figures 3 and 4, very low input and output ripple currents result.

Figure 11 shows a typical application using LTC3719 to power the AMD CPU core. The input can vary from 7V to 24V, the output voltage can be programmed from 0.8V to 1.55V with a maximum current of 45A. This power supply receives three input signals to generate different output voltage offsets based on the operation conditions.

TYPICAL APPLICATION

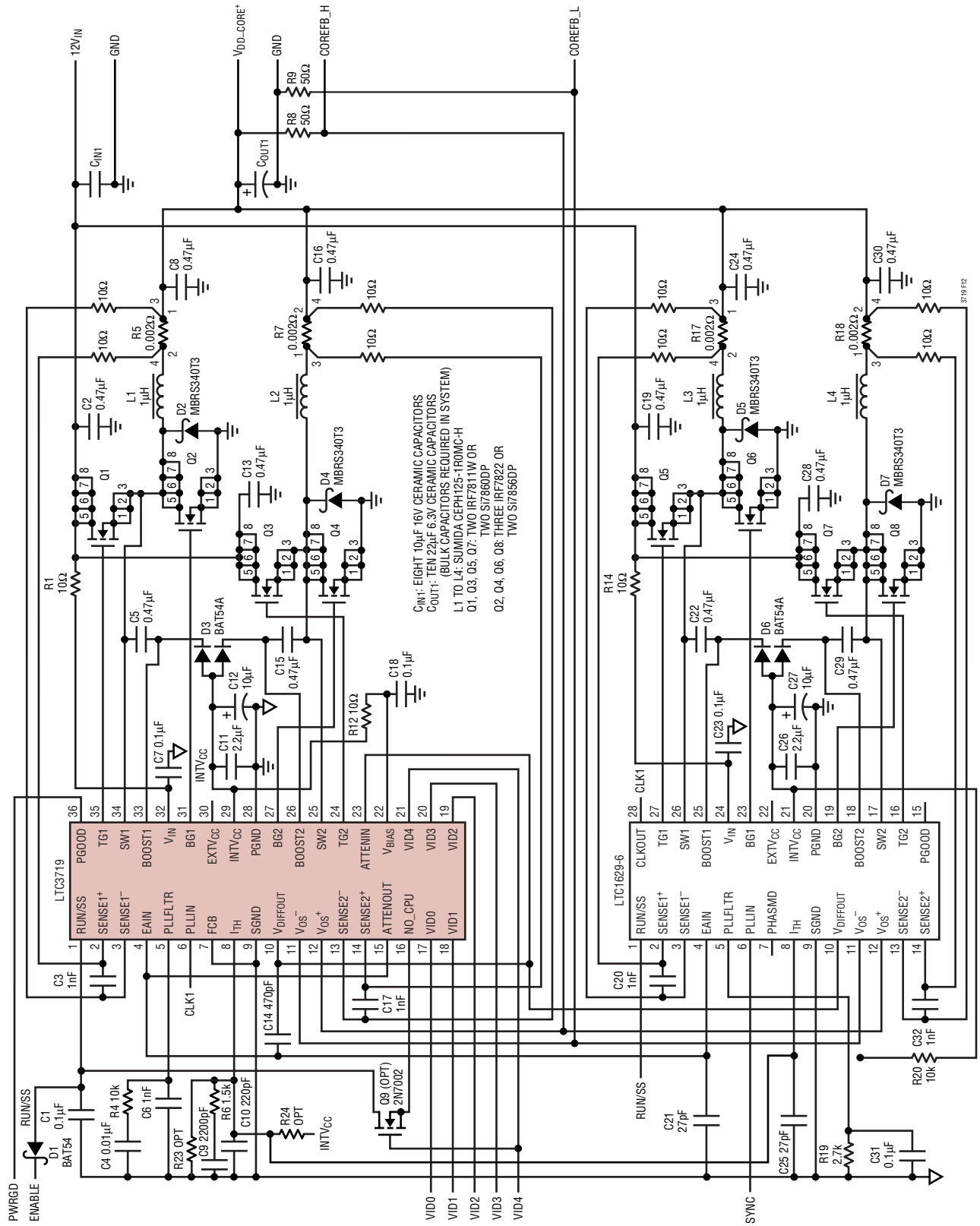


Figure 11. 4-Phase 12V Input, 0.8V to 1.55V/80A Max Power Supply for Server Applications

TYPICAL APPLICATION

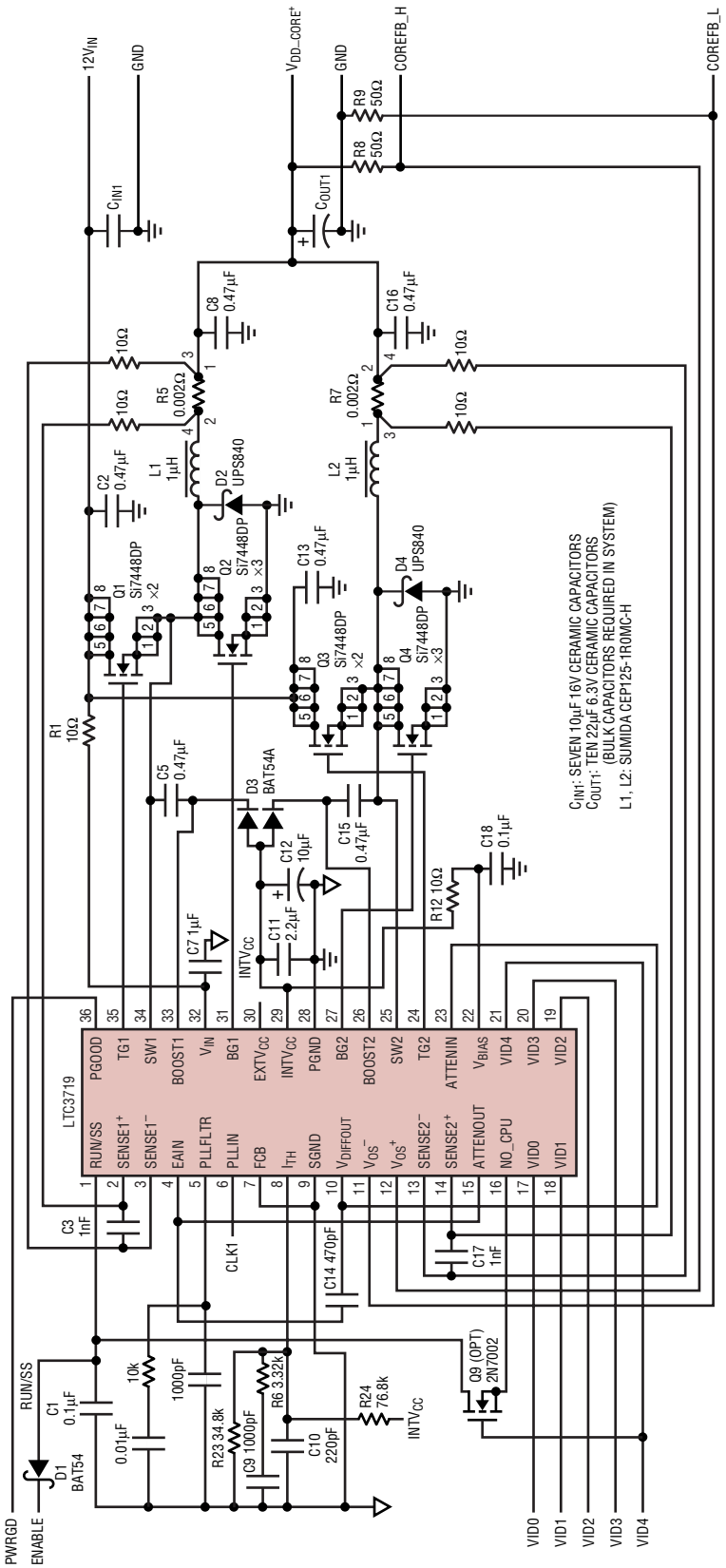
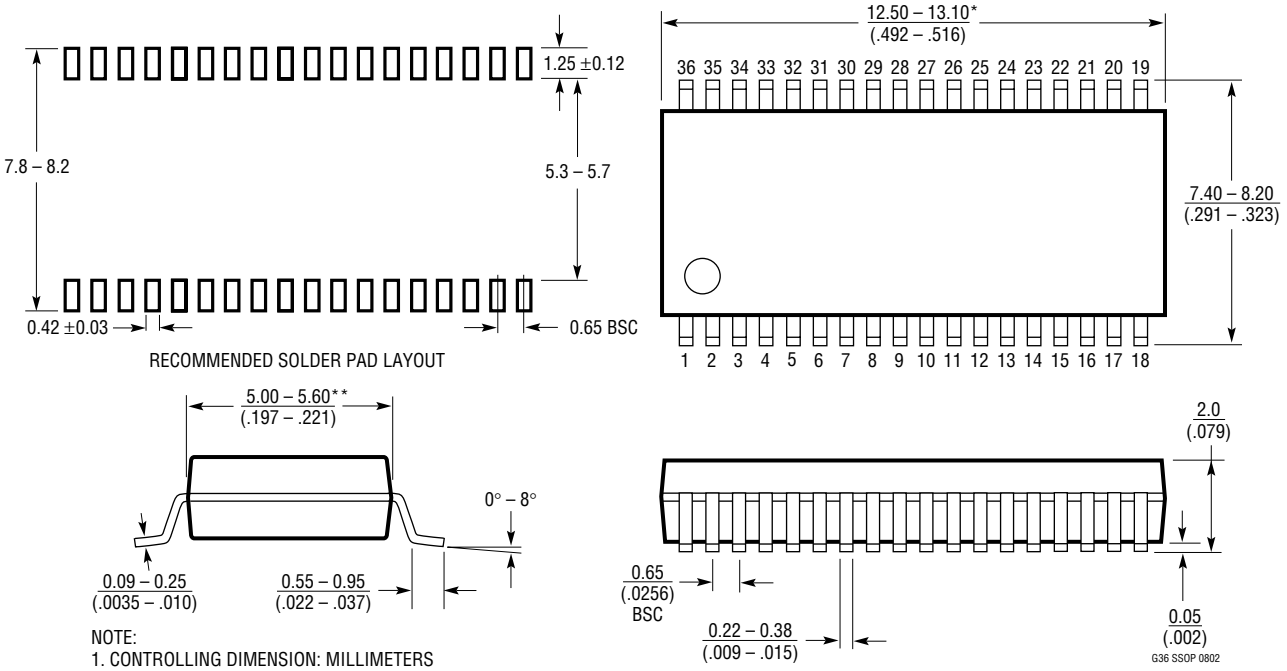


Figure 12. 2-Phase 12V Input, 0.8V to 1.55V/42A Max Power Supply for AMD Hammer CPUs with Active Voltage Positioning (AVP)

PACKAGE DESCRIPTION

G Package
36-Lead Plastic SSOP (5.3mm)
(Reference LTC DWG # 05-08-1640)



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1436A-PLL	High Efficiency Low Noise Synchronous Step-Down Switching Regulator	Adaptive Power™ Mode, 24-Pin SSOP
LTC1438/LTC1439	Dual High Efficiency Low Noise Synchronous Step-Down Switching Regulators	POR, Auxiliary Regulator
LTC1438-ADJ	Dual Synchronous Controller with Auxiliary Regulator	POR, External Feedback Divider
LTC1538-AUX	Dual High Efficiency Low Noise Synchronous Step-Down Switching Regulator	Auxiliary Regulator, 5V Standby
LTC1539	Dual High Efficiency Low Noise Synchronous Step-Down Switching Regulator	5V Standby, POR, Low Battery, Aux Regulator
LTC1628/LTC1628-PG	Dual High Efficiency, 2-Phase Synchronous Step-Down Switching Regulator	Constant Frequency, Standby, 5V and 3.3V LDOs
LTC1629/LTC1629-PG	PolyPhase High Efficiency Controller	Expandable Up to 12 Phases, G-28, Up to 120A
LTC1702A/LTC1703	Dual High Efficiency, 2-Phase Synchronous Step-Down Switching Regulators	500kHz, 25MHz GBW, Error Amplifer
LTC1708-PG	Dual High Efficiency, 2-Phase Synchronous Step-Down Switching Regulator with 5-Bit VID and Power Good Indication	$1.3V \le V_{OUT} \le 3.5V$, Current Mode Ensures Accurate Current Sharing, $3.5V \le V_{IN} \le 36V$
LTC1709-7	2-Phase High Efficiency Controller with 5-Bit Mobile VID and Power Good Indication ($0.9V \le V_{OUT} \le 2V$)	Burst Mode Operation and Cycle Skip Low Current Modes, $3.5V \le V_{IN} \le 36V$
LTC1709-8/LTC1709-9	2-Phase High Efficiency Controller with 5-Bit VID and Power Good Indication	VID Tables VRM 8.4 and VRM9.0, $I_{OUT} \le 40A$
LTC1735	High Efficiency Synchronous Step-Down Controller	Burst Mode Operation, 16-Pin Narrow SSOP, Fault Protection, $3.5V \le V_{IN} \le 36V$
LTC1736	High Efficiency Synchronous Step-Down Controller with 5-Bit VID	Output Fault Protection, Power Good, GN-24, $3.5V \le V_{IN} \le 36V$, $0.925V \le V_{OUT} \le 2V$
LT1769	2A Monolithic Battery Charger	CC/CV Switching DC/DC Converter, 5% Charge Accuracy, Adapter Current Limit for Maximum Charge Current
LTC1778	No R_{SENSE}™ Synchronous Current Mode Step-Down Controller	No Sense Resistor Required, $4V \le V_{IN} \le 36V$, $0.8V \le V_{OUT} \le V_{IN}$, SSOP-16
LTC1929/LTC1929-PG	2-Phase High Efficiency Controller	Adjustable Output Up to 40A, G-28
LTC1960	Dual Battery Charger/Selector with SPI Interface	Extends Run Time by 10%, Reduces Charging Time by 50%, 36-Lead SSOP
LTC3716	2-Phase High Efficiency Controller with 5-Bit VID and Power Good Indication	$0.6V \le V_{OUT} \le 1.75V$, $I_{OUT} \le 40A$
LTC3717/LTC3831	DDR Memory Termination Regulators (V_{TT} Supply)	Precision Regulation, Up to 20A, Small PCB Area
LTC3728	Dual 2-Phase 550kHz Step-Down Synchronous Controller	Up to 550kHz per Phase, Dual Output, $I_{OUT} \le 20A$
LTC3729	550kHz PolyPhase Step-Down Synchronous Controller	Up to 550kHz per Phase, Up to 12-Phase Operation, I_{OUT} = 20A per Phase
LTC3732	3-Phase Step-Down Synchronous Controller (VRM 9.0/9.1)	600kHz per Phase, 5-Bit VID, ±5% Accurate Current Sharing, $I_{OUT} \le 60A$

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