

Bias Resistor Transistors

NPN Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

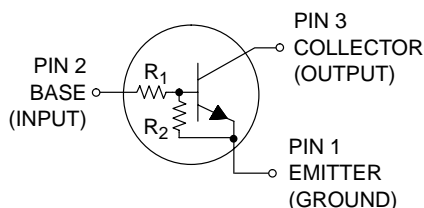
This new series of digital transistors is designed to replace a single device and its external resistor bias network. The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space. The device is housed in the SOT-23 package which is designed for low power surface mount applications.

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count

LMUN2237LT1



CASE 318-08, STYLE 6
SOT-23 (TO-236AB)



MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	50	Vdc
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector Current	I_C	100	mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	230 (Note 1) 338 (Note 2) 1.8 (Note 1) 2.7 (Note 2)	mW $^\circ\text{C/W}$
Thermal Resistance – Junction-to-Ambient	$R_{\theta JA}$	540 (Note 1) 370 (Note 2)	$^\circ\text{C/W}$
Thermal Resistance – Junction-to-Lead	$R_{\theta JL}$	264 (Note 1) 287 (Note 2)	$^\circ\text{C/W}$
Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

1. FR-4 @ Minimum Pad
2. FR-4 @ 1.0 x 1.0 inch Pad

LMUN2237LT1

DEVICE MARKING AND RESISTOR VALUES

Device	Package	Marking	R1 (K)	R2 (K)
LMUN2237LT1	SOT-23	A8P	47	22

3. New devices. Updated curves to follow in subsequent data sheets.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted) (Continued)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Collector-Base Cutoff Current ($V_{CB} = 40\text{ V}$, $I_E = 0$)	I_{CBO}	–	–	50	nAdc
Collector-Emitter Cutoff Current ($V_{CE} = 40\text{ V}$, $I_B = 0$)	I_{CEO}	–	–	50	nAdc
Emitter-Base Cutoff Current ($V_{BE} = 6.0\text{ V}$, $I_C = 0$)	I_{EBO}	–	–	0.13	mAdc
Collector-Base Breakdown Voltage ($I_C = 10\text{ }\mu\text{A}$, $I_E = 0$)	$V_{(BR)CBO}$	50	–	–	Vdc
Collector-Emitter Breakdown Voltage (Note 4) ($I_C = 2.0\text{ mA}$, $I_B = 0$)	$V_{(BR)CEO}$	50	–	–	Vdc

ON CHARACTERISTICS (Note 4)

DC Current Gain ($V_{CE} = 10\text{ V}$, $I_C = 5.0\text{ mA}$)	h_{FE}	80	140	–	
Collector-Emitter Saturation Voltage ($I_C = 10\text{ mA}$, $I_B = 5\text{ mA}$)	$V_{CE(sat)}$	–	–	0.25	Vdc
Output Voltage (on) ($V_{CC} = 5.0\text{ V}$, $V_B = 4.0\text{ V}$, $R_L = 1.0\text{ k}\Omega$)	V_{OL}	–	–	0.2	Vdc
Input Resistor	R_1	32.9	47	61.1	$\text{k}\Omega$
Resistor Ratio	R_1/R_2	1.7	2.1	2.6	

4. Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%

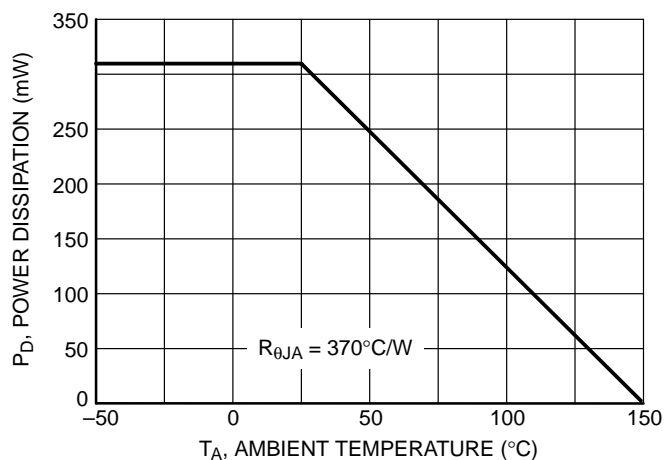


Figure 1. Derating Curve

TYPICAL ELECTRICAL CHARACTERISTICS – LMUN2237LT1

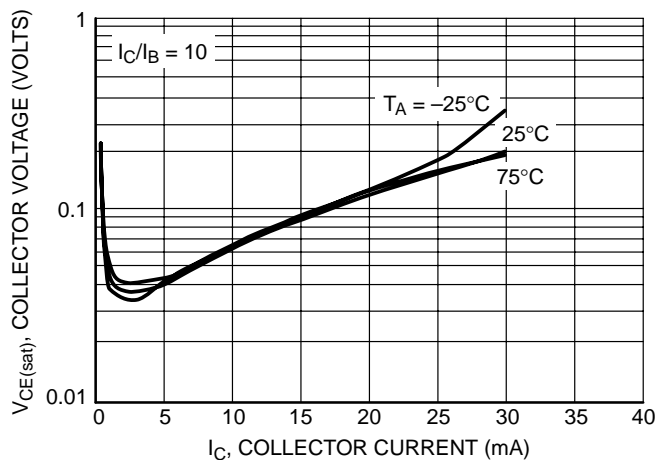


Figure 2. $V_{CE(sat)}$ versus I_C

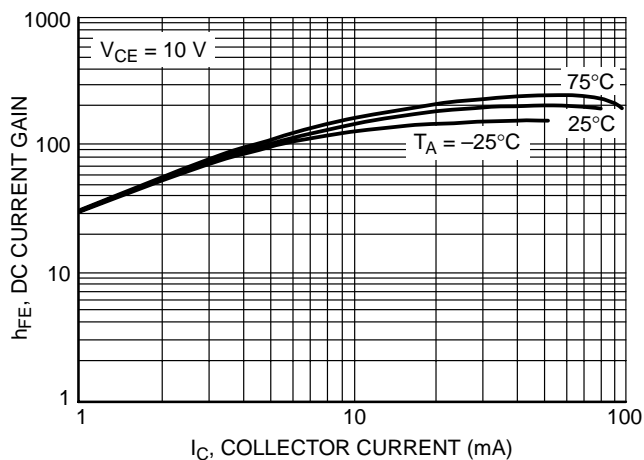


Figure 3. DC Current Gain

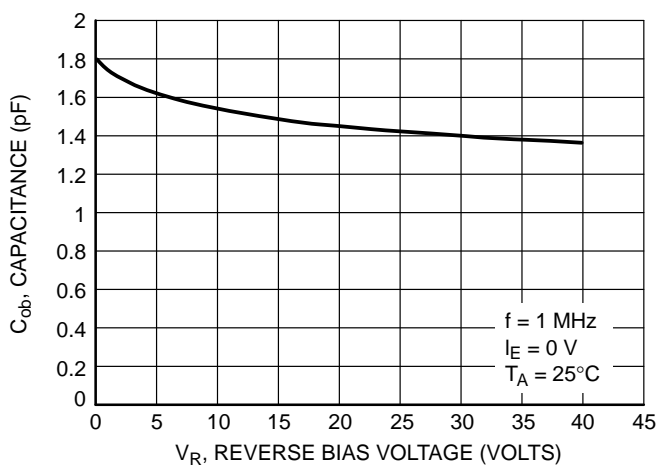


Figure 4. Output Capacitance

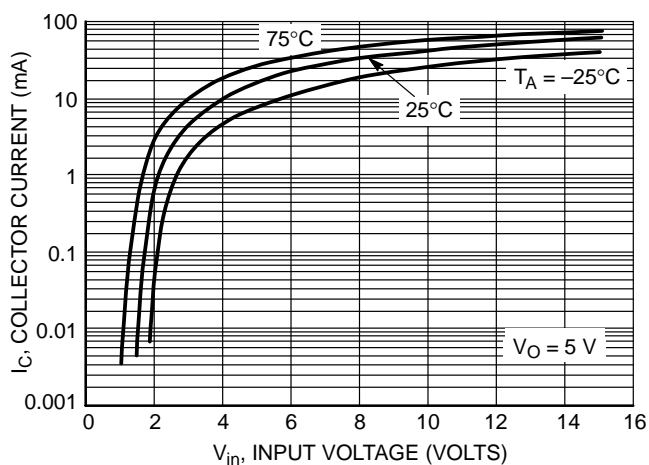


Figure 5. Output Current versus Input Voltage

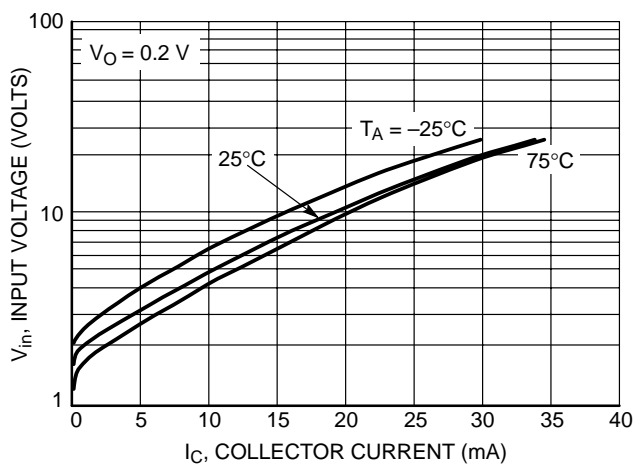
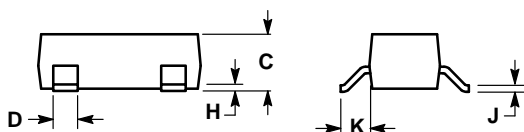
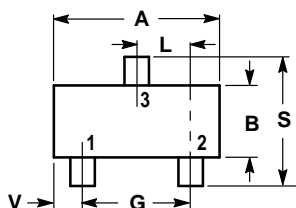


Figure 6. Input Voltage versus Output Current

LMUN2237LT1

SOT-23



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI
Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60

- PIN 1. BASE
2. EMITTER
3. COLLECTOR

