LSI/CSI
Manufacturers of Custom and Standard LSI Circuits

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LS7100

Revised July 1989

BCD TO 7-SEGMENT LATCH/DECODER/DRIVER

for liquid crystal (dynamic scattering) displays

FEATURES:

- Up to −50V Segment Output
- All Inputs are TTL or CMOS Compatible
- Internal Pull-Down Resistors on all Inputs
- Operating Voltage Range From −5V to −60V

DESCRIPTION:

The LS7100 is a monolithic, ion implanted MOS, BCD to 7-segment latched decoder/driver capable of driving displays over a wide voltage range.

This circuit is specifically intended to drive large light scattering liquid crystal displays.

DESCRIPTION OF OPERATION:

COMMON (COM) INPUT

COM is the common source for 7 internal FET Switch segment outputs.

A, B, C, D AND LOAD (LD) INPUTS

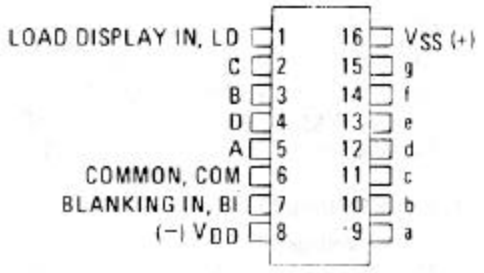
The BCD (or binary) data applied to the A,B,C,D inputs are latched into internal flip-flops when the LD input is high. If the input data changes while LD is high, the flip-flops will follow the input data. When LD is low, the inputs are isolated from the flip-flops. The latched data are decoded to 7-segments to control the opening and closing of the segment switch outputs (See display format for 0-15 binary decoding).

Each of these inputs has an internal pull-down (to logic "0") resistor.

SEGMENT OUTPUTS

The segment outputs are open-drain outputs of FET switches, with COM input as the common source. The electrical path from COM to any segment output is effectively an analog switch which can be either closed or opened by decoded data stored in internal latches associated with A,B,C,D inputs. The display segment drive wave-forms are not generated internally. The desired output wave-forms must be applied to the COM input. When a segment analog switch is closed, the drive wave-form at COM is connected to the respective output and when the switch is open, the output is cut off from COM and has very high impedance.

PIN ASSIGNMENT DIAGRAM



TOP VIEW
STANDARD 16 PIN DIP
FIGURE 1

BLANKING (BI) INPUT

Blanking of the display is provided by the BI. When BI is high, all FET switches are opened thereby turning off display segments. When BI is low, the selected FET switches are closed.

BI has an internal pull-down (to logic "0") resistor.

INPUT INTERFACE

LS7100 inputs can be interfaced with TTL, CMOS, NMOS or PMOS outputs by connecting VSS to the positive terminal (output logic "1", reference supply) of the TTL, CMOS, NMOS or PMOS supply.

ABSOLUTE MAXIMUM RATINGS:

(All voltages referenced to V_{SS}, Pin 16)

	SYMBOL	VALUE	UNIT
DC Supply Voltage	V_{DD}	+0.3 to −60	V
Common In	V_{CI}	+0.3 to −60	V
All other inputs	V_{IN}	+0.3 to −30	V
Operating Temperature	T_A	−40 to +70	°C
Storage Temperature	Tstg	−65 to +125	°C

ELECTRICAL CHARACTERISTICS:

-40°C T_A 70°C unless otherwise specified
V_{SS} = 0 unless otherwise specified

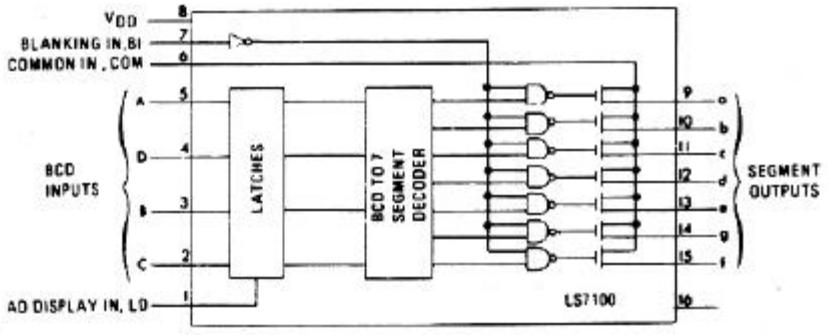
PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS, REMARKS
POWER SUPPLY					
V_{DD}	−5	–	−60	V	
I_{DD}	–	600	–	µA	@V_{DD} = −40V
COMMON INPUT					
V_{COM} High	–	−.5	0	V	
V_{COM} Low	V_{DD}+3	V_{DD}+10	–	V	
V_{COM} Low − V_{SS}	–	–	−50	V	
Leakage Current	–	–	5	nA	@V_{DD} = -40V, V_{DD} +3V< V_{COM} -0.5V
ALL OTHER INPUTS					
Input High Voltage V_{IH}, "1"	−1.5	–	0	V	
Input Low Voltage V_{IL}, "0"	V_{DD}	–	−4	V	V_{DD} ≥ −15V
	−15	–	−4	V	V_{DD} < −15V
Input High Current I_{IH}	–	–	40	µA	T_A = 25°C
Input Low Current I_{IL}	–	–	40	µA	T_A = 25°C
SEGMENT OUTPUTS					
OFF Segment Leakage Current	–	5	–	nA	@V_{DD} = −40V, V_{DD} +3V< V_{SEG} ≤ −0.5V
ON Segment Output Current	–	–	5	mA	Maximum recommended

SWITCHING CHARACTERISTICS*

V_{DD} = −40V, T_A = 25°C
(Outputs unloaded)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
BCD data set up time	t_{DS}	0	–	–	ns
BCD data hold time	t_{HS}	500	–	–	ns
Load pulse width	t_{LW}	1.0	–	–	µs
BCD data pulse width	t_{DW}	1.5	–	–	µs
Blank to seg off delay	t_{PBH}	–	1.0	–	µs
Blank to seg on delay	t_{PBL}	–	1.3	–	µs
Load to seg on delay	t_{PLH}	–	1.5	–	µs
Load to seg off dealy	t_{PLL}	–	1.0	–	µs
Propagation delay from COM input to any segment output	–	–	–	300	ns

*See Figure 3.



LS7100 FUNCTIONAL DIAGRAM

FIGURE 2

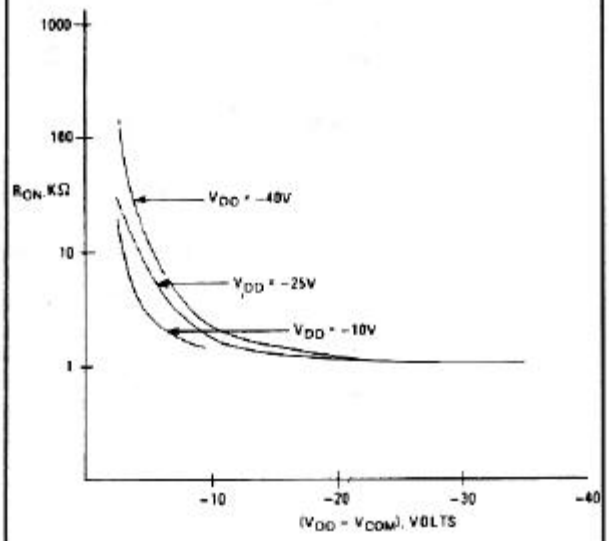
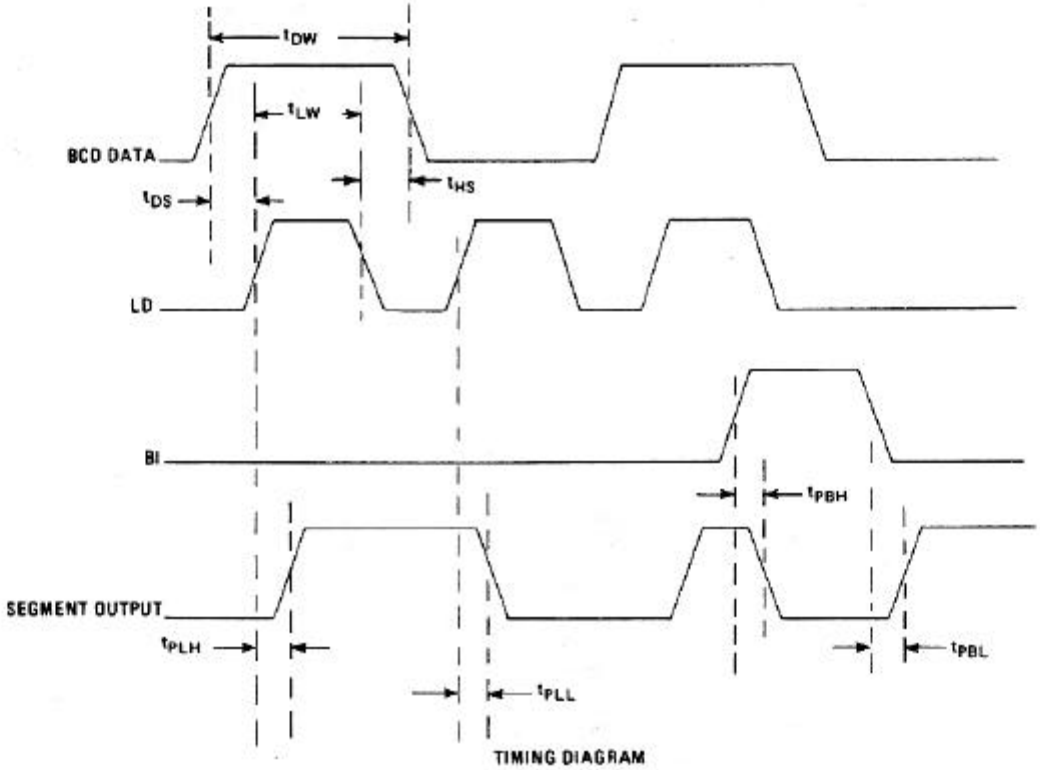


FIGURE 4

CHANNEL ON RESISTANCE, R_{ON}



TIMING DIAGRAM

FIGURE 3

DISPLAY FORMAT

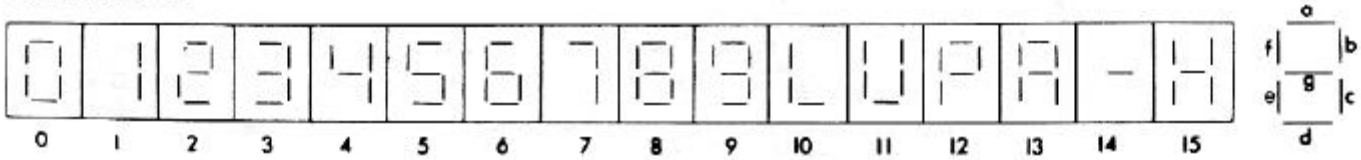
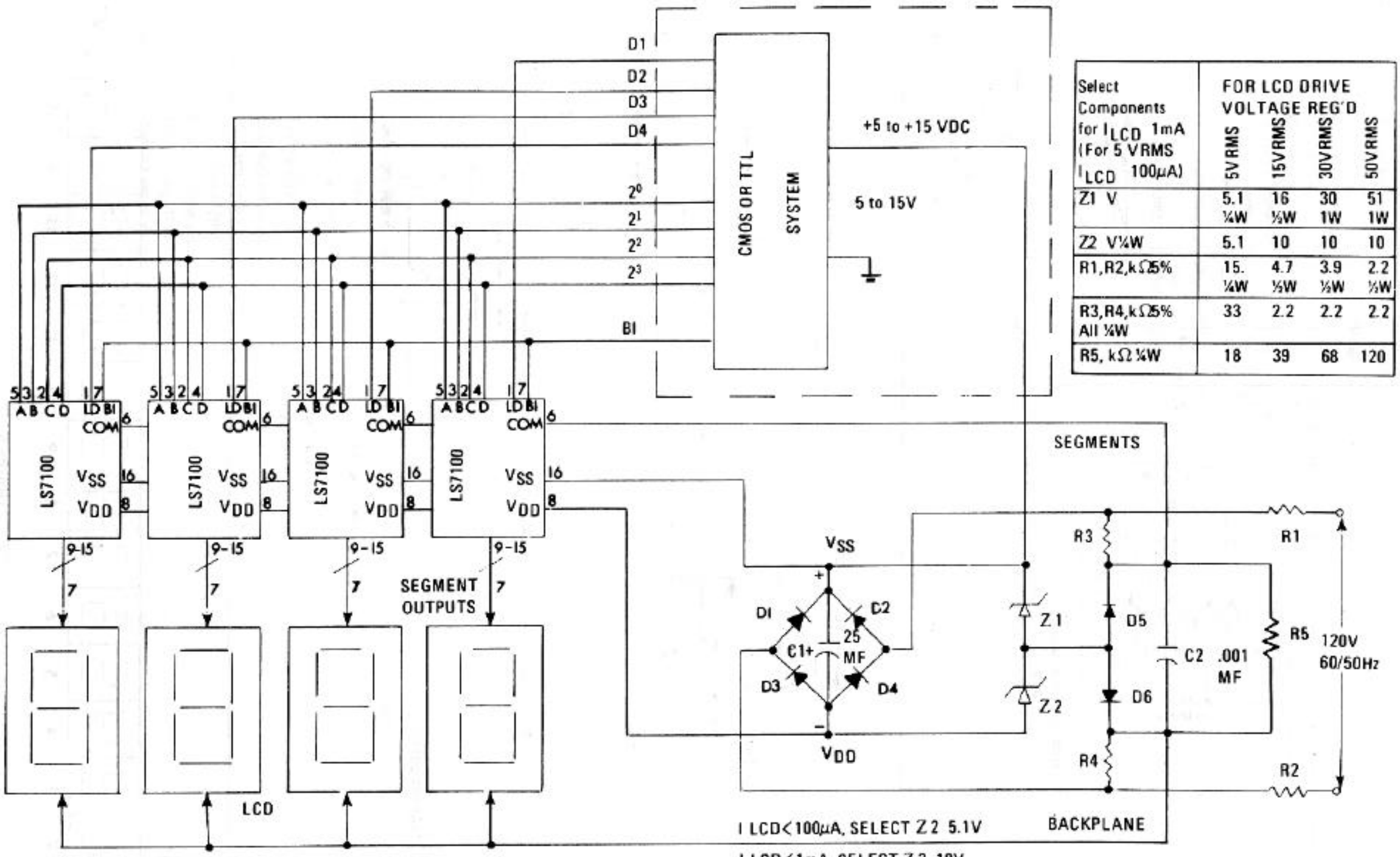


FIGURE 5



Select Components for I_{LCD} 1mA (For 5 VRMS I_{LCD} 100μA)	FOR LCD DRIVE VOLTAGE REG'D 5VRMS	15VRMS	30VRMS	50VRMS
Z1 V	5.1 ¼W	16 ½W	30 1W	51 1W
Z2 V¼W	5.1	10	10	10
R1,R2,kΩ5%	15. ¼W	4.7 ½W	3.9 ½W	2.2 ½W
R3,R4,kΩ5% All ¼W	33	2.2	2.2	2.2
R5, kΩ ¼W	18	39	68	120

APPLICATION NOTE – 4 DIGIT LCD DRIVE USING LS7100
(from 120 VAC line)

FIGURE 6