

MAX331/DG201A/DG217

Features

- ◆ Improved 2nd Source! (See pages 3 and 5 for "MAXIM Advantage"™)
- ◆ Guaranteed $\pm 4.5V$ to $\pm 18V$ Operation
- ◆ No V_L Supply Required
- ◆ Non-Latching with Supplies Turned-off and Input Signals Present
- ◆ CMOS and TTL Logic Compatible
- ◆ Monolithic, Low Power CMOS Design

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX331MJE	-55°C to +125°C	16 Lead Cerdip
DG201AAK	-55°C to +125°C	16 Lead Cerdip
DG201ABK	-25°C to +85°C	16 Lead Cerdip
DG201ACK	0°C to +70°C	16 Lead Cerdip
DG201ACJ	0°C to +70°C	16 Lead Plastic DIP
DG201ACSE	0°C to +70°C	16 Lead Small Outline
DG201C/D	0°C to +70°C	Dice
DG211CJ	0°C to +70°C	16 Lead Plastic DIP
DG211CSE	0°C to +70°C	16 Lead Small Outline
DG211C/D	0°C to +70°C	Dice

Pin Configuration

Top View

Pinout diagram for MAX331 DG201A and DG211. The diagram shows a 16-pin package with pins numbered 1 to 16. The pin functions are:

- 1 IN1
- 2 D1
- 3 S1
- 4 V-
- 5 GND
- 6 S4
- 7 D4
- 8 IN4
- 9 IN3
- 10 D3
- 11 S3
- 12 NC*
- 13 V+ (SUBSTRATE)
- 14 S2
- 15 D2
- 16 IN2

LOGIC	SWITCH
0	ON
1	OFF

Note: * Pins 1, 8, 9 and 16 are logic control inputs.

Quad SPST CMOS Analog Switches

ABSOLUTE MAXIMUM RATINGS (DG211)

V^+ to V^-	40V
V_{IN} to Ground	V^-, V^+
V_L to Ground	-0.3V, 25V
V_S or V_D to V^+	0, -40V
V_S or V_D to V^-	0, 40V
V^+ to Ground	25V
V^- to Ground	-25V
Current, Any Terminal Except S or D	30mA
Continuous Current, S or D	20mA
Peak Current, S or D (Pulsed at 1msec, 10% duty cycle max)	70mA

Storage Temperature	-65°C to +125°C
Operating Temperature	0°C to +70°C
Power Dissipation (Note 1)	
16 Pin Plastic DIP (Note 2)	470mW
16 Pin Small Outline (SE) (Note 3)	400mW

Note 1: Device mounted with all leads soldered to PC board.

Note 2: Derate 6.5mW/°C above +25°C.

Note 3: Derate 7mW/°C above +25°C.

Stresses listed under "Absolute Maximum Ratings" may be applied (one at a time) to devices without resulting in permanent damage. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (DG211)

($V^+ = +15V$, $V^- = -15V$, GND = 0V, $T_A = +25^\circ\text{C}$, unless otherwise noted)

	PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
				MIN (Note 4)	TYP (Note 5)	MAX	
SWITCH	Analog Signal Range	V_{ANALOG}		-15		15	V
	Drain-Source ON Resistance	$r_{DS(on)}$	$V_D = \pm 10V$, $V_{IN} = 0.8V$, $I_S = 1mA$		115	175	Ω
	Source OFF Leakage Current	$I_{S(off)}$	$V_{IN} = 2.4V$ $V_S = 14V$, $V_D = -14V$ $V_S = -14V$, $V_D = 14V$		0.01 -5.0	5.0 -0.02	nA
	Drain OFF Leakage Current	$I_{D(off)}$	$V_{IN} = 2.4V$ $V_S = 14V$, $V_D = -14V$ $V_S = -14V$, $V_D = 14V$		0.01 -5.0	5.0 -0.02	
	Drain ON Leakage Current (Note 6)	$I_{D(on)}$	$V_S = V_D = 14V$, $V_{IN} = 0.8V$ $V_S = V_D = -14V$, $V_{IN} = 0.8V$		0.1 -5.0	5.0 -0.15	
INPUT	Input Current With Input Voltage High	I_{INH}	$V_{IN} = 2.4V$ $V_{IN} = 15V$	-1.0	-0.0004	1.0	μA
	Input Current With Input Voltage Low	I_{INL}	$V_{IN} = 0V$	-1.0	-0.0004		
DYNAMIC	Turn-ON Time	t_{on}	See Switching Time Test Circuit $V_S = 2V$, $R_L = 1k\Omega$, $C_L = 35pF$		460	1000	ns
	Turn-OFF Time	t_{off1}			360	500	
		t_{off2}			450		
	Source OFF Capacitance	$C_{S(off)}$	$V_S = 0V$, $V_{IN} = 5V$, $f = 1MHz$		5		pF
	Drain OFF Capacitance	$C_{D(off)}$	$V_D = 0V$, $V_{IN} = 5V$, $f = 1MHz$		5		
	Channel ON Capacitance	$C_{D-S(on)}$	$V_D = V_S = 0V$, $V_{IN} = 0V$, $f = 1MHz$		16		
SUPPLY	OFF Isolation (Note 7)	OIRR	$V_{IN} = 5V$, $R_L = 1k\Omega$, $C_L = 15pF$, $V_S = 1VRMS$, $f = 100kHz$		70		dB
	Crosstalk (Channel to Channel)	CCRR			90		
	Positive Supply Current	I^+			0.35	0.48	
	Negative Supply Current	I^-	$V_{IN} = 0V$ and $2.4V$		0.30	0.48	mA
	Logic Supply Current	I_L			0.5	1.2	

Note 4: The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.

Note 5: Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Note 6: $I_{D(on)}$ is leakage from driver into "ON" switch.

Note 7: OFF Isolation = $20 \log \frac{V_S}{V_D}$, V_S = input to OFF switch, V_D = output.

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Quad SPST CMOS Analog Switches

- ◆ Significantly Reduced Power Consumption
- ◆ Third (Logic) Supply Not Required
- ◆ Fault Protected

ABSOLUTE MAXIMUM RATINGS (DG211) This device conforms to the Absolute Maximum Ratings on the adjacent page.

ELECTRICAL CHARACTERISTICS (DG211): Specifications below satisfy or exceed all "tested" parameters on adjacent page.

($V^+ = +15V$, $V^- = -15V$, GND = 0V, $T_A = +25^\circ C$, unless otherwise noted)

	PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
				MIN (Note 4)	TYP (Note 5)	MAX	
SWITCH	Analog Signal Range	V_{ANALOG}		-15		15	V
	Drain-Source ON Resistance	$r_{DS(on)}$	$V_D = \pm 10V$, $V_{IN} = 0.8V$, $I_S = 1mA$		115	175	Ω
	Source OFF Leakage Current	$I_{S(off)}$	$V_{IN} = 2.4V$ $V_S = 14V$, $V_D = -14V$ $V_S = -14V$, $V_D = 14V$		0.01 -0.02	5.0	nA
	Drain OFF Leakage Current	$I_{D(off)}$	$V_{IN} = 2.4V$ $V_S = 14V$, $V_D = -14V$ $V_S = -14V$, $V_D = 14V$		0.01 -0.02	5.0	
	Drain ON Leakage Current (Note 6)	$I_{D(on)}$	$V_S = V_D = 14V$, $V_{IN} = 0.8V$ $V_S = V_D = -14V$, $V_{IN} = 0.8V$		0.1 -0.15	5.0	
INPUT	Input Current With Input Voltage High	I_{INH}	$V_{IN} = 2.4V$ $V_{IN} = 15V$	-1.0	-0.0004 0.003	1.0	μA
	Input Current With Input Voltage Low	I_{INL}	$V_{IN} = 0V$	-1.0	-0.0004		
DYNAMIC	Turn-ON Time	t_{on}	See Switching Time Test Circuit $V_S = 2V$, $R_L = 1k\Omega$, $C_L = 35pF$		460	1000	ns
	Turn-OFF Time	t_{off1}			360	500	
		t_{off2}			450		
	Source OFF Capacitance	$C_{S(off)}$	$V_S = 0V$, $V_{IN} = 5V$, $f = 1MHz$		5		pF
	Drain OFF Capacitance	$C_{D(off)}$	$V_D = 0V$, $V_{IN} = 5V$, $f = 1MHz$		5		
	Channel ON Capacitance	$C_{D+S(on)}$	$V_D = V_S = 0V$, $V_{IN} = 0V$, $f = 1MHz$		16		dB
SUPPLY	OFF Isolation (Note 8)	OIRR	$V_{IN} = 5V$, $R_L = 1k\Omega$, $C_L = 15pF$, $V_S = 1VRMS$, $f = 100kHz$		70		
	Crosstalk (Channel to Channel)	CCRR			90		
	Positive Supply Current	I^+			0.02	0.1	mA
	Negative Supply Current	I^-			0.01	0.1	
	Logic Supply Current	I_L			0.0	0.0	
	Power Supply Range for Continuous Operation	V_{OP}	$V_{IN} = 0V$ and $2.4V$	± 4.5		± 18	V

Note 8: Electrical characteristics, such as ON Resistance, will change when power supplies, other than $\pm 15V$, are used.

MAX331/DG201A/DG211

Quad SPST CMOS Analog Switches

ABSOLUTE MAXIMUM RATINGS (MAX331, DG201A)

Voltages Referenced to V ⁻		Storage Temperature	-65°C to +150°C
V ⁺	44V	Power Dissipation (Note 2)	
GND	25V	16 Pin CERDIP (Note 3)	900mW
Digital Inputs (Note 1), V _S , V _D	-2V to (V ⁺ +2V) or 20mA, whichever occurs first	16 Pin Plastic DIP (Note 4)	470mW
Current, Any Terminal Except S or D	30mA	16 Pin Small Outline (SE) (Note 5)	400mW
Continuous Current, S or D	20mA		
Peak Current, S or D (Pulsed at 1msec, 10% duty cycle max.)	70mA		
Operating Temperature			
DG201A (A Suffix)	-55°C to +125°C		
(B Suffix)	-25°C to +85°C		
(C Suffix)	0°C to +70°C		
MAX331MJE	-55°C to +125°C		

Note 1: Signals on S_X, D_X, or I_{NX} exceeding V⁺ or V⁻ on Maxim's MAX331 and DG201A will be clamped by internal diodes, and are also internally current limited to 25mA.

Note 2: Device mounted with all leads soldered to PC board.

Note 3: Derate 12mW/°C above +75°C.

Note 4: Derate 6.5mW/°C above +25°C.

Note 5: Derate 7mW/°C above +25°C.

Stresses listed under "Absolute Maximum Ratings" may be applied (one at a time) to devices without resulting in permanent damage. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (DG201A)

(V⁺ = -15V, V⁻ = -15V, GND = 0V, T_A = +25°C, unless otherwise noted)

	PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS						UNITS
					DG201AA			DG201AB,C			
					MIN	TYP	MAX	MIN	TYP	MAX	
					(Note 6)	(Note 7)		(Note 6)	(Note 7)		
SWITCH	Analog Signal Range	V _{ANALOG}			-15		15	-15		15	V
	Drain-Source ON Resistance	r _{DS(on)}	V _D = +10V, V _{IN} = 0.8V, I _S = 1mA			115	175		115	200	Ω
	Source OFF Leakage Current	I _{S(off)}	V _{IN} = 2.4V	V _S = 14V, V _D = -14V V _S = -14V, V _D = 14V	0.01	1.0		0.01	5.0	nA	
	Drain OFF Leakage Current	I _{D(off)}	V _{IN} = 2.4V	V _S = 14V, V _D = -14V V _S = -14V, V _D = 14V	0.01	1.0		0.01	5.0		
	Drain ON Leakage Current (Note 8)	I _{D(on)}	V _S = -14V, V _{IN} = 0.8V V _D = 14V, V _{IN} = 0.8V	0.1	1.0		0.1	5.0			
				-1.0	-0.15		-5.0	-0.15			
INPUT	Input Current With Input Voltage High	I _{INH}	V _{IN} = 2.4V V _{IN} = 15V		-1.0	-0.0004		-1.0	-0.0004	μA	
	Input Current With Input Voltage Low	I _{INL}	V _{IN} = 0V		-1.0	-0.0004		-1.0	-0.0004		
	DYNAMIC	Turn-ON Time	t _{on}	See Switching Time Test Circuit		480	600		480	600	ns
Turn-OFF Time		t _{off1}	370			450		370	450		
Charge Injection		Q	C _L = 1000pF, V _{GEN} = 0V, R _{GEN} = 0Ω		20			20	pC		
Source OFF Capacitance		C _{S(off)}	V _S = 0V, V _{IN} = 5V	f = 140kHz	5			5	pF		
Drain OFF Capacitance		C _{D(off)}			5			5			
Channel ON Capacitance		C _{D(on)} + C _{S(on)}	V _D = V _S = 0V, V _{IN} = 0V		16			16			
OFF Isolation			V _{IN} = 5V, Z _L = 75Ω		70			70	dB		
Crosstalk (Channel to Channel)		V _S = 2.0V, f = 100kHz		90			90				
SUPPLY	Positive Supply Current	I ⁺	All Channels ON or OFF		0.9	2		0.9	2	mA	
	Negative Supply Current	I ⁻			-1	-0.3		-1	-0.3		

Note 6: The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.

Note 7: Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Note 8: I_{D(on)} is leakage from driver into "ON" switch.

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Quad SPST CMOS Analog Switches

- ◆ Significantly Reduced Power Consumption
- ◆ Lower Input Current Over Temperature
- ◆ No Input Current Spike

ABSOLUTE MAXIMUM RATINGS (MAX331, DG201A) This device conforms to the Absolute Maximum Ratings on the adjacent page.

ELECTRICAL CHARACTERISTICS (MAX331, DG201A): Specifications below satisfy or exceed all "tested" parameters on adjacent page.

($V^+ = +15V$, $V^- = -15V$, GND = 0V, $T_A = +25^\circ C$, unless otherwise noted)

	PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS						UNITS
					MAX331/DG201AA			DG201AB,C			
					MIN (Note 6)	TYP (Note 7)	MAX (Note 7)	MIN (Note 6)	TYP (Note 7)	MAX (Note 7)	
SWITCH	Analog Signal Range	V _{ANALOG}			-15		15	-15		15	V
	Drain-Source ON Resistance (Note 9)	r _{DS(on)}	V _D = ±10V, V _{IN} = 0.8V, I _S = 1mA			115	175		115	200	Ω
	Source OFF Leakage Current	I _{S(off)}	V _{IN} = 2.4V	V _S = 14V, V _D = -14V V _S = -14V, V _D = 14V	0.01	1.0		0.01	5.0		nA
	Drain OFF Leakage Current	I _{D(off)}	V _{IN} = 2.4V	V _S = 14V, V _D = -14V V _S = -14V, V _D = 14V	0.01	1.0		0.01	5.0		
	Drain ON Leakage Current (Note 8)	I _{D(on)}	V _S = -14V, V _{IN} = 0.8V V _D = 14V, V _{IN} = 0.8V		0.1	1.0		0.1	5.0		
INPUT	Input Current With Input Voltage High	I _{INH}	V _{IN} = 2.4V V _{IN} = 15V		-1.0	-0.0004		-1.0	-0.0004		μA
	Input Current With Input Voltage Low	I _{INL}	V _{IN} = 0V		-1.0	-0.0004		-1.0	-0.0004		
DYNAMIC	Turn-ON Time	t _{on}	See Switching Time Test Circuit		480	600		480	600		ns
	Turn-OFF Time	t _{off1}			370	450		370	450		
	Charge Injection	Q	C _L = 1000pF, V _{GEN} = 0V, R _{GEN} = 0Ω		20			20		pC	
	Source OFF Capacitance	C _{S(off)}	V _S = 0V, V _{IN} = 5V		5			5		pF	
	Drain OFF Capacitance	C _{D(off)}	f = 140kHz		5			5			
	Channel ON Capacitance	C _{D(on)} + C _{S(on)}			16			16			
	OFF Isolation		V _{IN} = 5V, Z _L = 75Ω		70			70		dB	
Crosstalk (Channel to Channel)		V _S = 2.0V, f = 100kHz		90			90				
SUPPLY	Positive Supply Current	I ⁺	All Channels ON or OFF		0.02	0.1		0.02	0.1		mA
	Negative Supply Current	I ⁻	All Channels ON or OFF		-0.1	-0.01		-0.1	-0.01		
	Power Supply Range for Continuous Operation	V _{OP}			±4.5	±18		±4.5	±18		V

Note 6: The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.

Note 7: Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Note 8: $I_{D(on)}$ is leakage from driver into "ON" switch.

Note 9: Electrical characteristics, such as ON Resistance, will change when power supplies other than $\pm 15V$, are used.

MAX331/DG201A/DG211

Quad SPST CMOS Analog Switches

ELECTRICAL CHARACTERISTICS (DG201A)

(V⁺ = +15V, V⁻ = -15V, GND = 0V, T_A = Full Operating Temperature Range)

	PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS						UNITS
					DG201AA			DG201AB,C			
					MIN	TYP	MAX	MIN	TYP	MAX	
					(Note 6)	(Note 7)		(Note 6)	(Note 7)		
SWITCH	Analog Signal Range	V _{ANALOG}			-15		15	-15		15	V
	Drain-Source ON Resistance	r _{DS(on)}	V _D = ±10V, V _{IN} = 0.8V, I _S = 1mA				250			250	Ω
	Source OFF Leakage Current	I _{S(off)}	V _{IN} = 2.4V	V _S = 14V, V _D = -14V			100			100	nA
				V _S = -14V, V _D = 14V	-100			-100			
	Drain OFF Leakage Current	I _{D(off)}	V _{IN} = 2.4V	V _S = 14V, V _D = -14V			100			100	
				V _S = -14V, V _D = 14V	-100			-100			
Drain ON Leakage Current (Note 10)	I _{D(on)}	V _S = -14V, V _{IN} = 0.8V				200			200		
		V _D = 14V, V _{IN} = 0.8V		-200			-200				
INPUT	Input Current With Input Voltage High	I _{INH}	V _{IN} = 2.4V		-1.0			-10			μA
			V _{IN} = 15V				-10			-10	
	Input Current With Input Voltage Low	I _{INL}	V _{IN} = 0V		-10			-10			

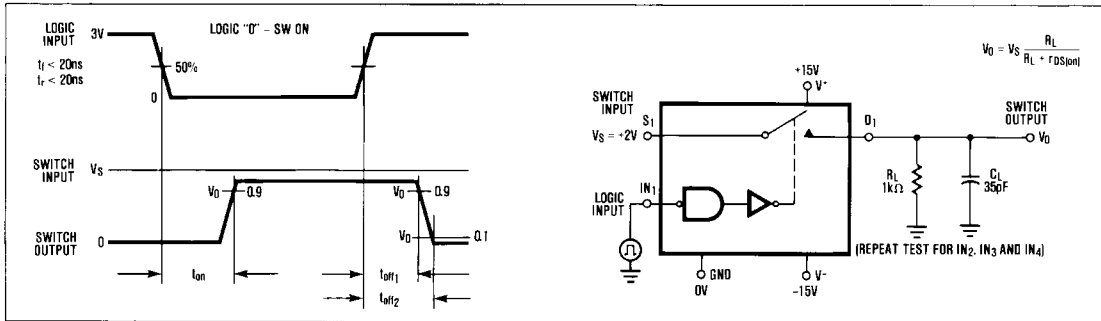
Note 10: I_{D(on)} is leakage from driver into "ON" switch.

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Switching Time Test Circuit

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be +ve or -ve as per switching times test circuit.

V_O is the steady state output with switch on. Feed-through via gate capacitance may result in spikes at leading and trailing edge of output waveform.



Typical R_{DS(ON)} vs. Power Supplies for Maxim's MAX331, DG201A and DG211

POWER SUPPLIES	R _{DS(ON)} AT ANALOG SIGNAL LEVEL					
	-5V	+5V	-10V	+10V	-15V	+15V
±5V	350Ω	380Ω				
±10V			165Ω	250Ω		
±15V			125Ω	160Ω	135Ω	155Ω



Quad SPST CMOS Analog Switches

ELECTRICAL CHARACTERISTICS (MAX331, DG201A):

($V^+ = +15V$, $V^- = -15V$, GND = 0V, T_A = full operating temperature range)

	PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS						UNITS
					MAX331/DG201AA			DG201AB,C			
					MIN (Note 6)	TYP (Note 7)	MAX	MIN (Note 6)	TYP (Note 7)	MAX	
SWITCH	Analog Signal Range	V _{ANALOG}			-15		15	-15		15	V
	Drain-Source ON Resistance (Note 11)	r _{DS(on)}	V _D = ±10V, V _{IN} = 0.8V, I _S = 1mA				250			250	Ω
	Source OFF Leakage Current	I _{S(off)}	V _{IN} = 2.4V	V _S = 14V, V _D = -14V V _S = -14V, V _D = 14V			100			100	nA
	Drain OFF Leakage Current	I _{D(off)}	V _{IN} = 2.4V	V _S = 14V, V _D = -14V V _S = -14V, V _D = 14V			100			100	
							100			100	
							100			100	
Drain ON Leakage Current (Note 10)	I _{D(on)}	V _S = -14V, V _{IN} = 0.8V V _D = 14V, V _{IN} = 0.8V				200			200		
INPUT	Input Current With Input Voltage High	I _{INH}	V _{IN} = 2.4V V _{IN} = 15V				-1.0			-1.0	μA
							1.0			1.0	
	Input Current With Input Voltage Low	I _{INL}	V _{IN} = 0V				-1.0			-1.0	

Note 10: $I_{D(on)}$ is leakage from driver into "ON" switch.

Note 11: Electrical characteristics, such as ON Resistance, will change when power supplies other than $\pm 15V$, are used.

Protecting Against Fault Conditions

Fault conditions occur when power supplies are turned off when input signals are still present or when over voltages occur at the inputs during normal operation. In either case, source-to-body diodes can be forward biased and conduct current from the signal source. If this current is required to be kept to low (μA) levels then the addition of external protection diodes is recommended.

To provide protection for over-voltages up to 20V above the supplies, a 1N4001 or 1N914 type diode should be placed in series with the positive and negative supplies as shown in Fig. 1. The addition of these diodes will reduce the analog signal range to 1 volt below the positive supply and 1 volt above the negative supply.

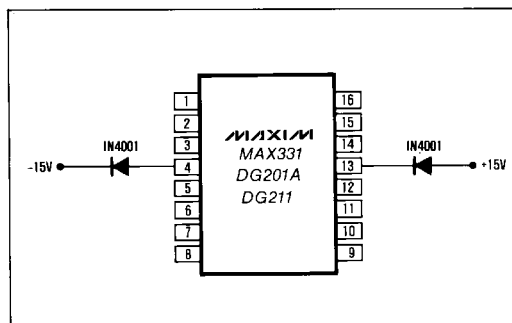
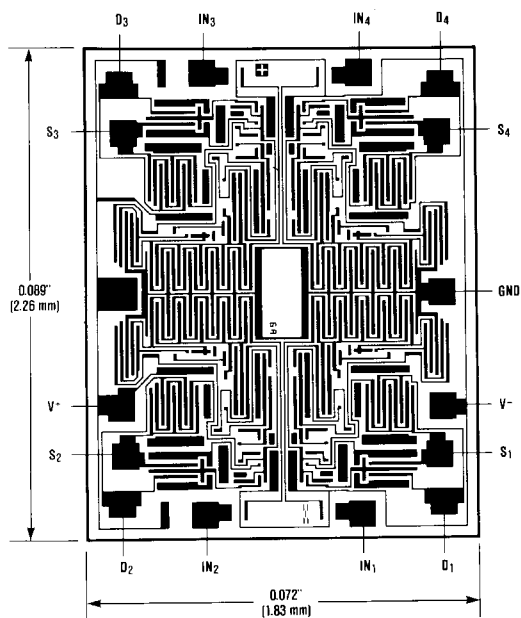


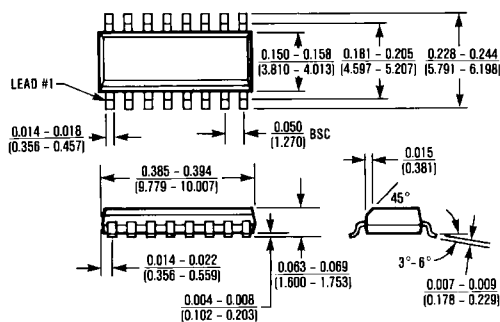
Figure 1. Protection Against Fault Conditions

Quad SPST CMOS Analog Switches

Chip Topography



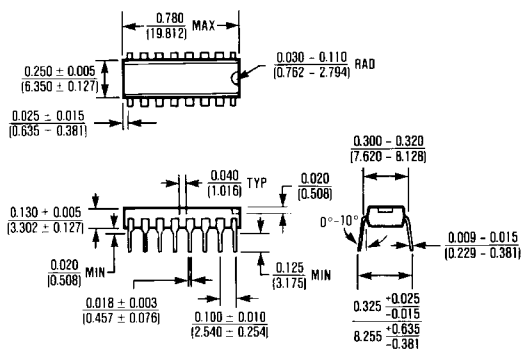
Package Information



16 Lead Small Outline (SE)

$\theta_{JA} = 110^{\circ}\text{C/W}$

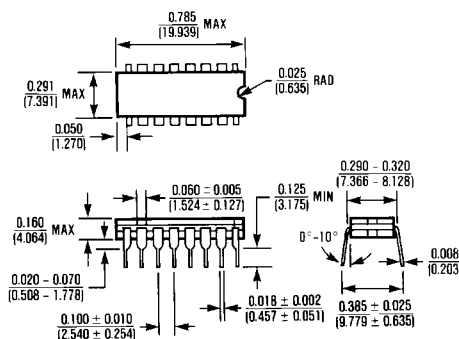
$\theta_{JC} = 60^{\circ}\text{C/W}$



16 Lead Plastic DIP

$\theta_{JA} = 135^{\circ}\text{C/W}$

$\theta_{JC} = 65^{\circ}\text{C/W}$



16 Lead Cerdip

$\theta_{JA} = 100^{\circ}\text{C/W}$

$\theta_{JC} = 60^{\circ}\text{C/W}$

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8 Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 (408) 737-7600

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