

MAXIM
Monolithic CMOS Analog Multiplexers

General Description

Maxim's DG508A and DG509A are monolithic CMOS analog multiplexers (muxes): the DG508A is a single 8-channel (1-of-8) mux, and the DG509A is a differential 4-channel (2-of-8) mux.

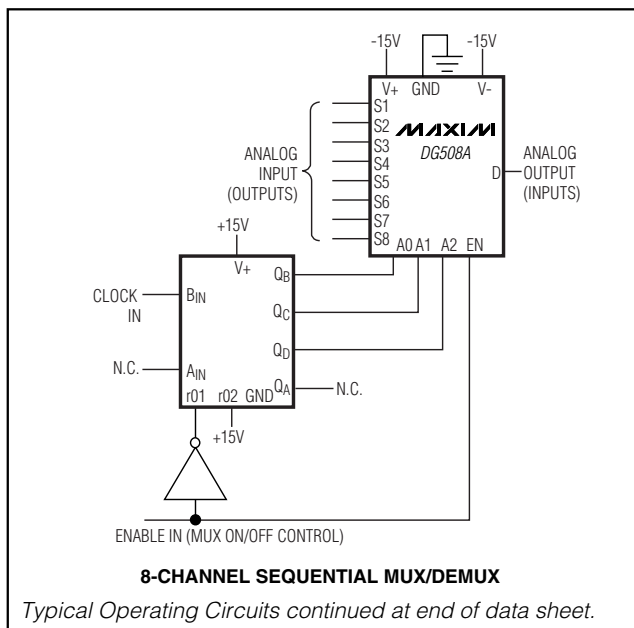
Both devices guarantee break-before-make switching. Maxim guarantees these muxes will not latch up if the power supplies are turned off with the input signals still present. Maxim also guarantees continuous operation when these devices are powered by supplies ranging from $\pm 4.5\text{V}$ to $\pm 18\text{V}$.

The DG508A/DG509A are plug-in upgrades for the industry-standard DG08A/DG509A, respectively. Maxim's parts have lower on-resistance, faster enable switching times, and significantly lower leakage currents. The DG508A/DG509A also consume significantly lower power, making them ideal for portable equipment.

Applications

- Control Systems
- Data Logging Systems
- Aircraft Heads-Up Displays
- Data-Acquisition Systems
- Signal Routing

Typical Operating Circuits



Features

- ◆ Improved Second Source
- ◆ Operate from $\pm 4.5\text{V}$ to $\pm 18\text{V}$ Supplies
- ◆ Symmetrical, Bidirectional Operation
- ◆ Logic and Enable Inputs, TTL and CMOS Compatible
- ◆ Latchup-Proof Construction
- ◆ Monolithic, Low-Power CMOS Design

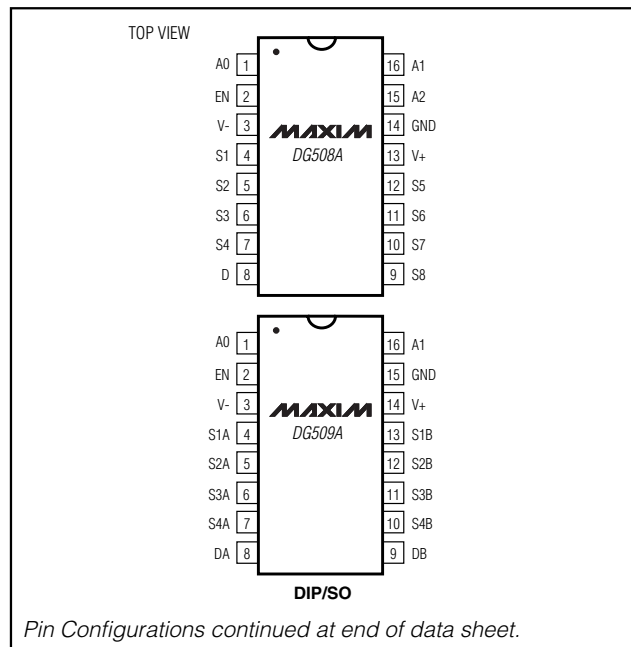
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DG508ACJ	0°C to +70°C	16 Plastic DIP
DG508ACWE	0°C to +70°C	16 Wide SO
DG508AC/D	0°C to +70°C	Dice*
DG508ABK	-20°C to +85°C	16 Cerdip
DG508ADJ	-40°C to +85°C	16 Plastic DIP
DG508ADY	-40°C to +85°C	16 Narrow SO
DG508AEGE	-40°C to +85°C	16 QFN
DG508AEWE	-40°C to +85°C	16 Wide SO
DG508AAK	-55°C to +125°C	16 Cerdip

Ordering Information continued at end of data sheet.

*Contact factory for dice specifications.

Pin Configurations



DG508A/DG509A

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ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-

V++44V
GND+25V
Digital Inputs, V _S and V _D (Note 1)-2V to (V+ + 2V) or 20mA, whichever occurs first
Current (any terminal, except S or D)30mA
Continuous Current, S or D20mA
Peak Current, S or D (pulsed at 1ms, 10% duty cycle max)40mA
Continuous Power Dissipation (T _A = +70°C)	
Plastic DIP (derate 10.53mW/°C above +70°C)842mW
QFN (derate 19.2mW/°C above +70°C)1538mW
Narrow SO (derate 8.70mW/°C above +70°C)696mW
Wide SO (derate 9.52mW/°C above +70°C)762mW
CERDIP (derate 10.00mW/°C above +70°C)800mW

Operating Temperature Ranges:

DG50_ACJ/CWE/CGE0°C to +70°C
DG50_ABK-20°C to +85°C
DGS0_ADJ/DY/EWE/EGE-40°C to +85°C
DG50_AAK-55°C to +125°C
Storage Temperature Range-65°C to +150°C
Lead Temperature (soldering, 10s)+300°C

Note 1: Signals on S₋, D₋, or IN₋ exceeding V+ or V- are clamped by internal diodes. Limit forward-diode current to maximum current ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 15V, V- = -15V, GND = OV, T_A = +25°C, unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS		DG508AA DG509AA			DG508AD/E/B/C DG509AD/E/B/C			UNITS		
					MIN	TYP	MAX	MIN	TYP	MAX			
SWITCH													
Analog Signal Range		V _{ANALOG}			-15		+15		-15		+15		V
Drain-Source On-Resistance		R _{DS(ON)}	Sequence each switch on, V _{AL} = 0.8V, V _{AH} = 2.4V (Note 4)	V _D = 10V, I _S = -200μA	170		300		170		350		Ω
				V _D = 10V, I _S = -200μA	130		300		130		350		
Greatest Change in Drain-Source On-Resistance Between Channels		ΔR _{DS(ON)}	$\Delta R_{DS(ON)} = \left(\frac{R_{DS(ON) \text{ max}} - R_{DS(ON) \text{ min}}}{R_{DS(ON)}} \right)$, -10V ≥ V _S ≥ 10V		6			6			%		
Source Off-Leakage Current		I _{S(OFF)}	V _{EN} = 0V	V _S = 10V, V _D = -10V	0.002		0.5		0.002		1		nA
				V _S = -10V, V _D = 10V	-0.5		-0.005		-1		-0.005		
Drain Off-Leakage Current	DG508A	I _{D(OFF)}	V _{EN} = 0V	V _D = 10V, V _S = -10V	0.01		2		0.01		5		nA
	V _D = 10V, V _S = -10V			-2		-0.015		-5		-0.015			
	DG509A			V _D = 10V, V _S = -10V	0.005		2		0.005		5		
	V _D = -10V, V _S = 10V			-2		-0.008		-5		-0.008			
Drain On-Leakage Current	DG508A	I _{D(ON)}	Sequence each switch on, V _{AL} = 0.8V V _{AH} = 2.4V (Note 2)	V _{S(all)} = V _D = 10V	0.015		2		0.015		5		nA
	V _{S(all)} = V _D = -10V			-2		-0.03		-5		-0.03			
	DG509A			V _{S(all)} = V _D = 10V	0.007		2		0.007		5		
	V _{S(all)} = V _D = -10V			-2		-0.015		-5		-0.015			

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DG508A/DG509A

ELECTRICAL CHARACTERISTICS (continued)

(V₊ = 15V, V₋ = -15V, GND = 0V, T_A = +25°C, unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS		DG508AA DG509AA			DG508AD/E/B/C DG509AD/E/B/C			UNITS
					MIN	TYP	MAX	MIN	TYP	MAX	
LOGIC INPUT											
Logic Input Current, Input Voltage High		I _{AH}	V _A = 24V		-10	-0.002		10	-0.002		μA
			V _A = 15V			0.006	10		0.006	10	
Logic Input Current, Input Voltage Low		I _{AL}	All V _A = 0V	V _{EN} = 2.4V	-10	-0.002		10	-0.002		μA
				V _{EN} = 0V	-10	-0.002		-10	-0.002		
DYNAMIC											
Multiplexer Switching Time		t _{transition}	Figure 1			0.6	1.0		0.6	1.0	μs
Break-Before-Make Interval		t _{OPEN}	Figure 3			0.2			0.2		μs
Enable Turn-On Time		t _{ON(EN)}	Figure 2			0.4	1.0		0.4	1.5	μs
Enable Turn-Off Time		t _{OFF(EN)}	Figure 2			0.2	0.7		0.2	1.0	μs
Off-Isolation		OIRR	V _{EN} = 0V, R _L = 1kΩ, C _L = 15pF, V _S = 7V _{RMS} f = 500kHz (Note 3)			68			68		dB
Source Off-Capacitance		C _{S(OFF)}	V _S = 0V, V _{EN} = 0V, f = 140kHz			5			5		pF
Drain Off-Capacitance	IDG508A	C _{D(OFF)}	V _S = 0V, V _{EN} = 0V, f = 140kHz			25			25		pF
	DGS09A					12			12		
SUPPLY											
Positive Supply Current		I ₊	V _{EN} = 2.4V, all V _A = 0V or 2.4V			0.02	0.2		0.02	0.2	mA
Negative Supply Current		I ₋	V _{EN} = 2.4V, all V _A = 0V or 2.4V		-0.1	-0.01		-0.1	-0.01		mA
Positive Supply Current in Standby		I ₊	V _{EN} = 0V, all V _A = 0V or 2.4V			0.02	0.2		0.02	0.2	mA
Negative Supply Current in Standby		I ₋	V _{EN} = 0V, all V _A = 0V or 2.4V		-0.1	-0.01		-0.1	-0.01		mA
Power-Supply Range for Continuous Operation		V ₋ , V ₊	(Notes 4, 5)		±4.5		±18.0	±4.5		±18.0	V

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ELECTRICAL CHARACTERISTICS

(V₊ = 15V, GND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS		DG508AA DG509AA MIN TYP MAX			DG508AD/E/B/C DG509AD/E/B/C MIN TYP MAX			UNITS
SWITCH											
Analog Signal Range		V _{ANALOG}			-15		+15	-15		+15	V
Drain-Source On-Resistance		R _{DS(ON)}	Sequence each switch on, V _{AL} = 0.8V, V _{AH} = 2.4V	V _D = 10V, I _S = -200μA	400		450		Ω		
				V _D = 10V, I _S = -200μA	400		450				
Source Off-Leakage Current		I _{S(OFF)}	V _{EN} = 0V	V _S = 10V, V _D = -10V	+50		+50		nA		
				V _S = -10V, V _D = -10V	-50		-50				
Drain Off-Leakage Current	DG508A	I _{D(OFF)}	V _{EN} = 0V	V _D = 10V, V _S = -10V	+200		+100		nA		
	V _D = -10V, V _S = -10V			-200		-200					
	DG509A			V _D = 10V, V _S = -10V	+200		+100				
	DG509A			V _D = -10V, V _S = -10V	-100		-100				
Drain On-Leakage Current	DG508A	I _{D(ON)}	Sequence each switch on, V _{AL} = 0.8V, V _{AH} = 2.4V (Note 2)	V _{S(all)} = V _D = 10V	+200		+100		nA		
	V _{S(all)} = V _D = -10V			-200		-100					
	DG509A			V _{S(all)} = V _D = 10V	+100		+100				
	DG509A			V _{S(all)} = V _D = -10V	-100		-100				
LOGIC INPUT											
Logic Input Current, Input Voltage High		I _{AH}	V _A = 2.4V		-30		-30		μA		
			V _A = 15V		+30		+30				
Logic Input Current, Input Voltage Low		I _{AL}	All V _A = 0V	V _{EN} = 2.4V	-30		-30		μA		
				V _{EN} = 0V	-30		-30				

Note 2: I_{D(ON)} is leakage from driver into on switch.

Note 3: Off-isolation = 20log $\frac{|V_S|}{|V_D|}$

V_S = input to off switch,
V_D = output due to V_S.

Note 4: Electrical characteristics (such as on-resistance) change when power supplies other than ±15V are used.

Note 5: For designs requiring single 5V or dual ±5V operation, refer to Maxim's improved MAX338 and MAX339. Minimum operating voltage for DG508ADY and DG509ADY is ±9V.

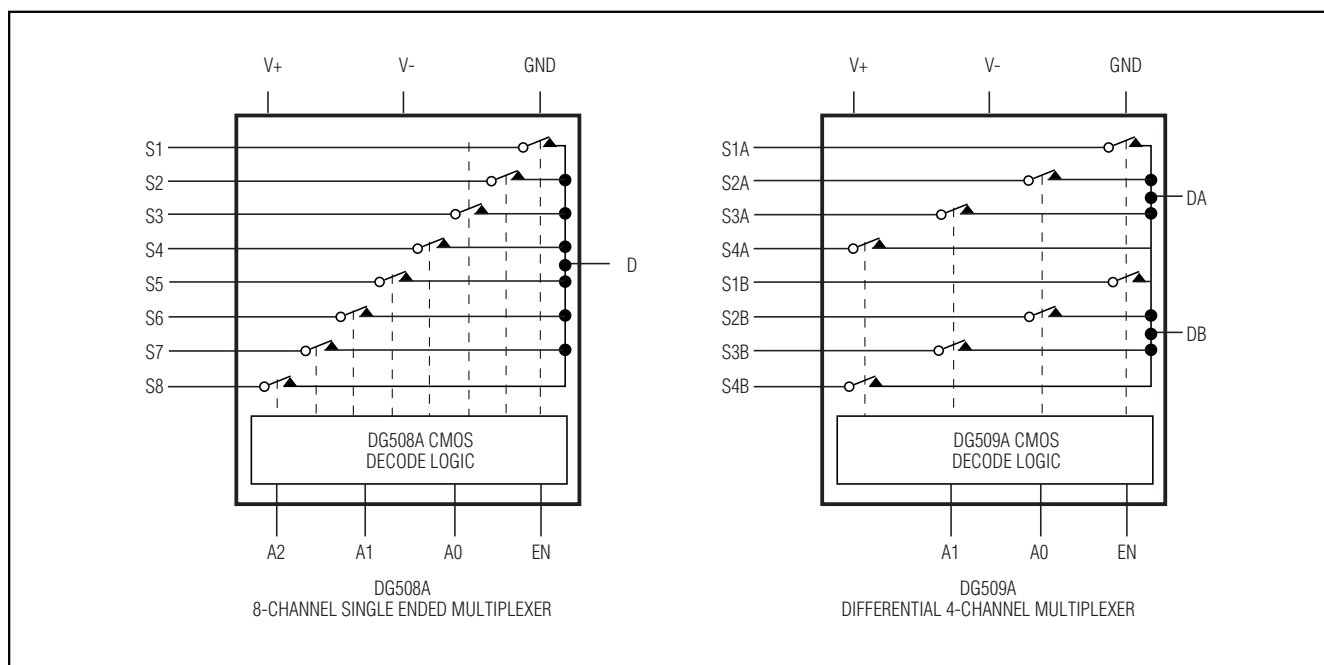
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Pin Description

PIN				NAME	FUNCTION
DG508A		DG509A			
DIP/SO	QFN	DIP/SO	QFN		
1, 15, 16	15, 14, 13	—	—	A0, A2, A1	Address Input
—	—	1, 16	15, 14	A0, A1	Address Input
2	16	2	16	EN	Enable
3	1	3	1	V-	Negative-Supply Voltage Input
4–7	2–5	—	—	S1–S4	Analog Inputs, Bidirectional
—	—	4–7	2–5	S1A–S4A	Analog Inputs, Bidirectional
8	6	—	—	D	Analog Outputs, Bidirectional
—	—	8, 9	6, 7	DA, DB	Analog Outputs, Bidirectional
9–12	7–10	—	—	S8–S5	Analog Inputs, Bidirectional
—	—	10–13	8–11	S4B–S1B	Analog Inputs, Bidirectional
13	11	14	12	V+	Positive-Supply Voltage Input
14	12	15	13	GND	Ground

DG508A/DG509A

Functional Diagrams



Monolithic CMOS Analog Multiplexers

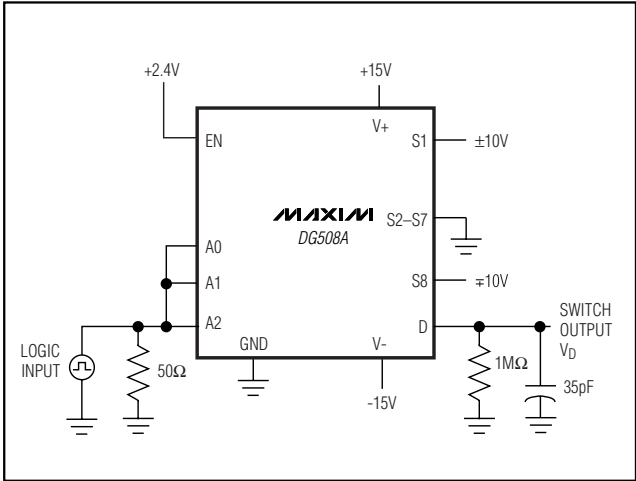


Figure 1a. Switching-Time Test Circuit

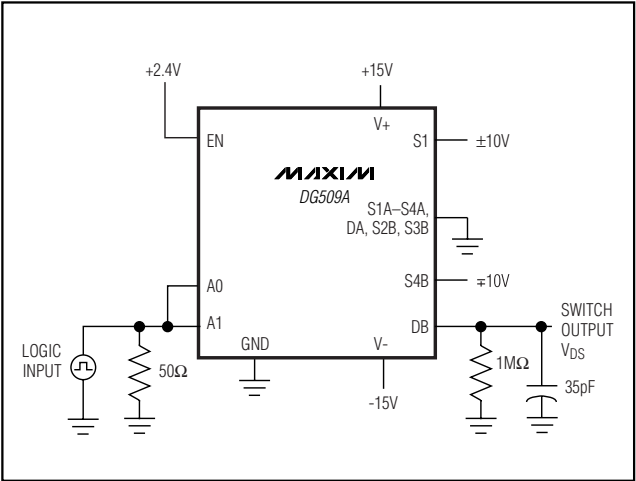


Figure 1b. Switching-Time Test Circuit

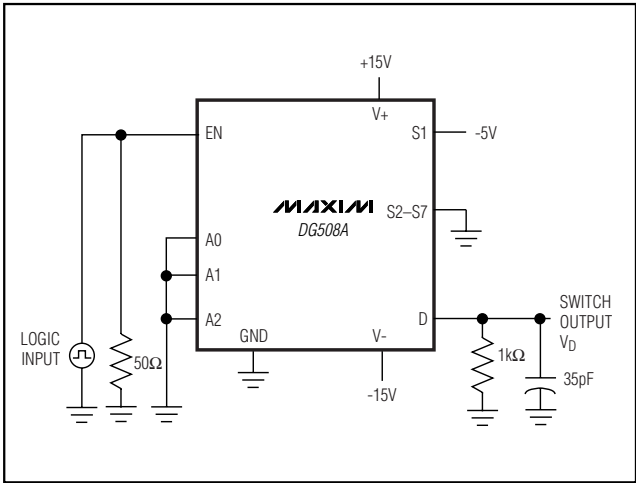


Figure 2a. DG509A Enable-Time Test Circuit

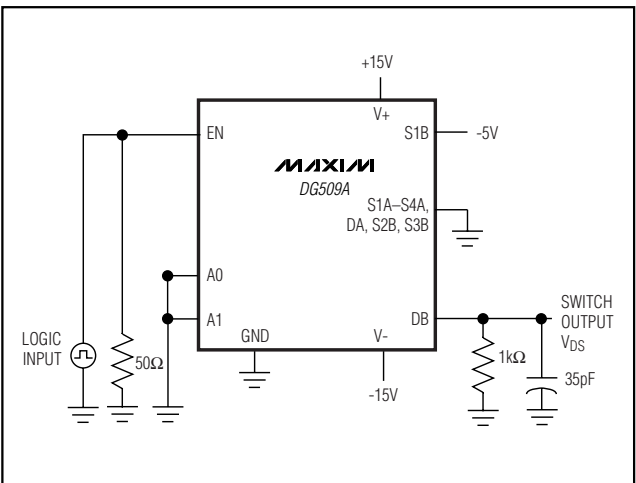


Figure 2b. DG509A Enable-Time Test Circuit

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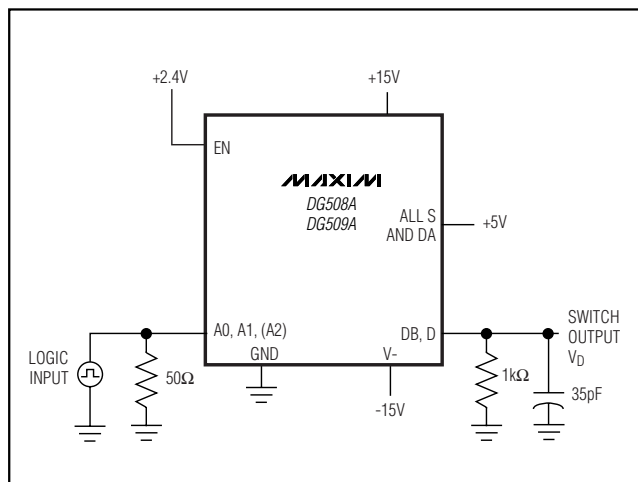


Figure 3. Break-Before-Make Test Circuit

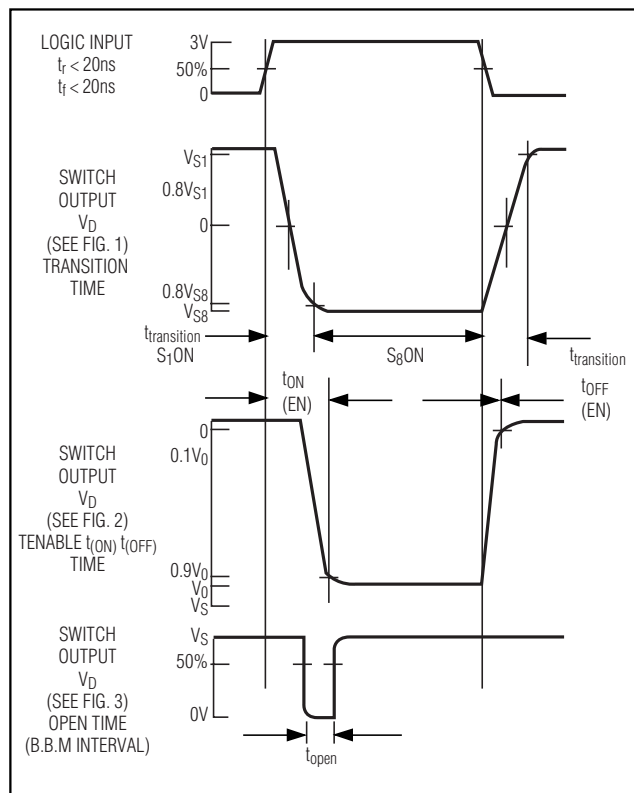


Figure 4. Timing Diagram for Figures 1, 2, and 3

Table 1a. DG508A Truth Table

A2	A1	A0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

X = Don't care.

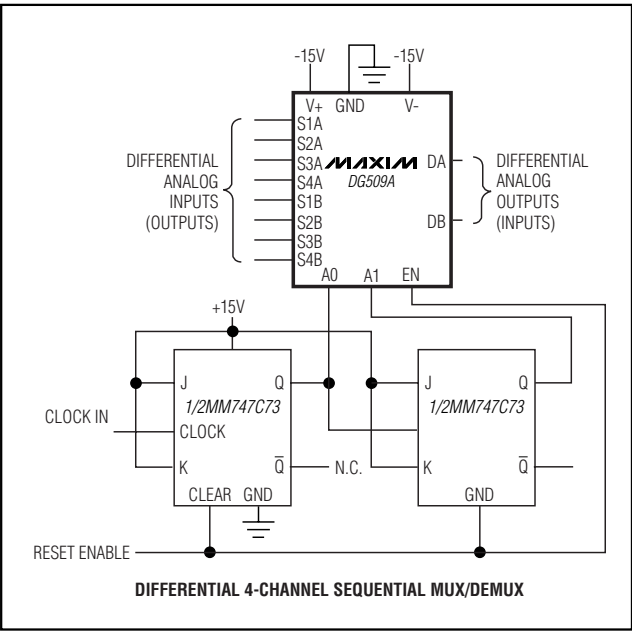
Table 1 b. DG509A Truth Table

A1	A0	EN	ON SWITCH
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

X = Don't care.

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Typical Operating Circuits (continued)

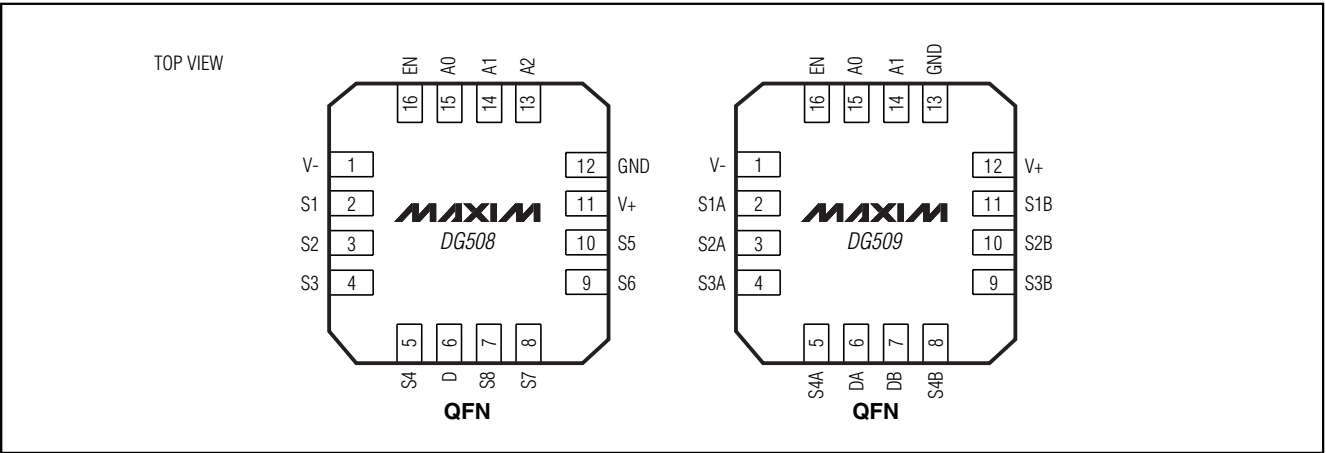


Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE
DG509ACJ	0°C to +70°C	16 Plastic DIP
DG509ACWE	0°C to +70°C	16 Wide SO
DG509AC/D	0°C to +70°C	Dice*
DG509ABK	-20°C to +85°C	16 Cerdip
DG509ADJ	-40°C to +85°C	16 Plastic DIP
DG509ADY	-40°C to +85°C	16 Narrow SO
DG509AEGE	-40°C to +85°C	16 QFN
DG509AEWE	-40°C to +85°C	16 Wide SO
DG509AAK	-55°C to +125°C	16 Cerdip

*Contact factory for dice specifications.

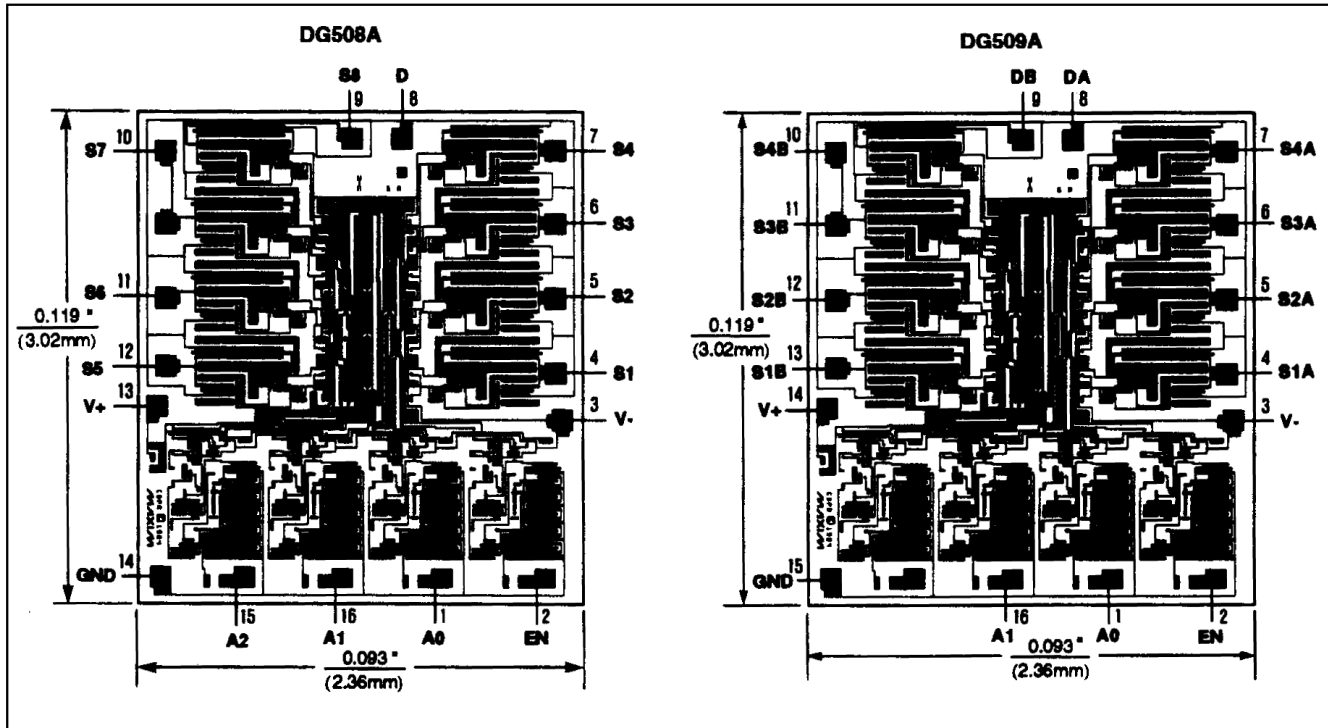
Pin Configurations (continued)



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Chip Topographies

DG508A/DG509A

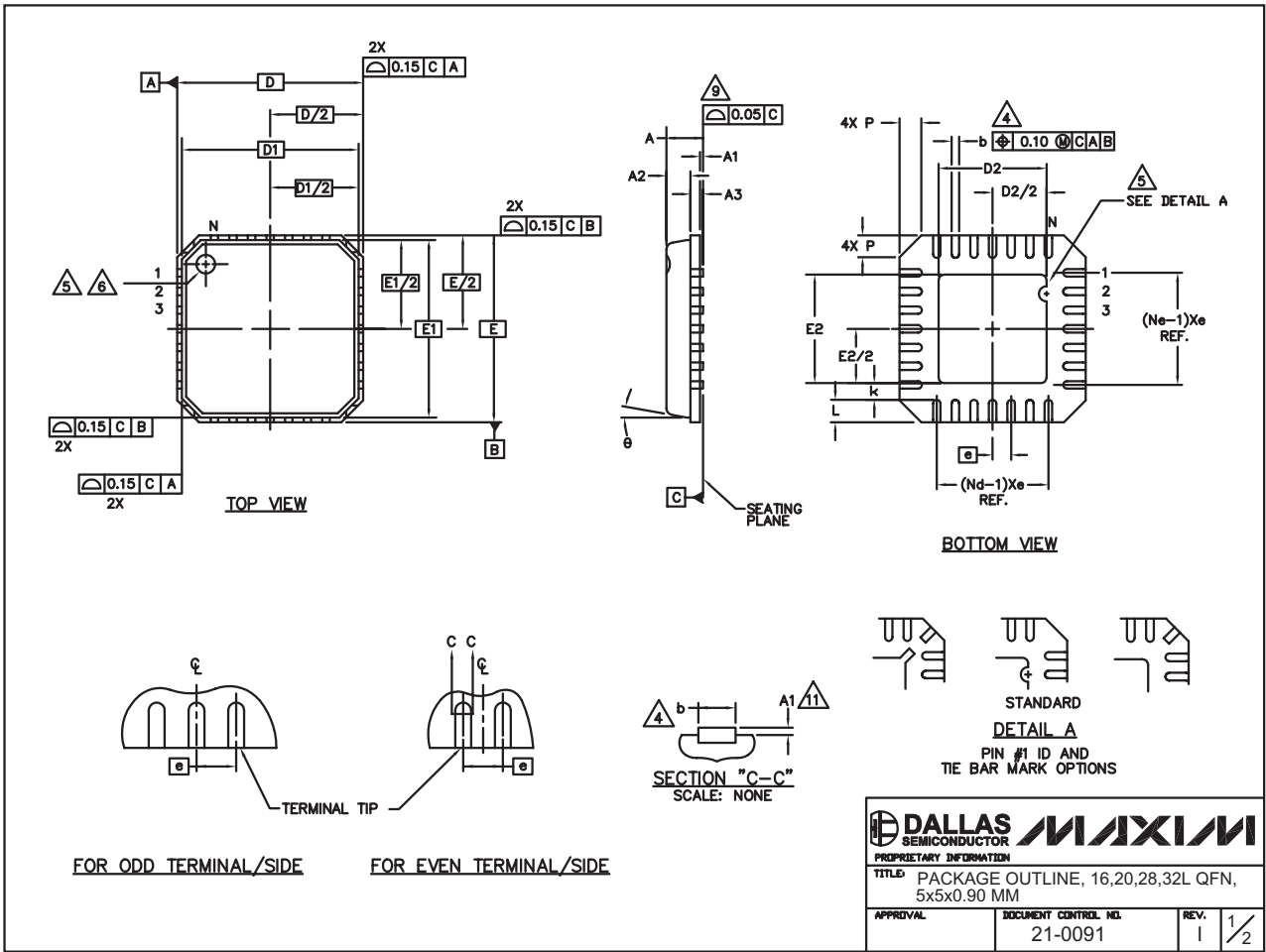


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Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)

32L QFN:EPS



Monolithic CMOS Analog Multiplexers

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)

DG508A/DG509A

COMMON DIMENSIONS												
PKG	16L 5x5			20L 5x5			28L 5x5			32L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.80	0.90	1.00	0.80	0.90	1.00	0.80	0.90	1.00
A1	0.00	0.01	0.05	0.00	0.01	0.05	0.00	0.01	0.05	0.00	0.01	0.05
A2	0.00	0.65	1.00	0.00	0.65	1.00	0.00	0.65	1.00	0.00	0.65	1.00
A3	0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.28	0.33	0.40	0.23	0.28	0.35	0.18	0.23	0.30	0.18	0.23	0.30
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
D1	4.75 BSC			4.75 BSC			4.75 BSC			4.75 BSC		
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E1	4.75 BSC			4.75 BSC			4.75 BSC			4.75 BSC		
e	0.80 BSC			0.65 BSC			0.50 BSC			0.50 BSC		
k	0.25	—	—	0.25	—	—	0.25	—	—	0.25	—	—
L	0.35	0.55	0.75	0.35	0.55	0.75	0.35	0.55	0.75	0.30	0.40	0.50
N	16			20			28			32		
ND	4			5			7			8		
NE	4			5			7			8		
P	0.00	0.42	0.60	0.00	0.42	0.60	0.00	0.42	0.60	0.00	0.42	0.60
ø	0"		12'	0"		12'	0"		12'	0"		12'

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
G1655-3	2.95	3.10	3.25	2.95	3.10	3.25
G2055-1	2.55	2.70	2.85	2.55	2.70	2.85
G2055-2	2.95	3.10	3.25	2.95	3.10	3.25
G2855-1	2.55	2.70	2.85	2.55	2.70	2.85
G2855-2	2.95	3.10	3.25	2.95	3.10	3.25
G3255-1	2.95	3.10	3.25	2.95	3.10	3.25

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. - 1994.
3. N IS THE NUMBER OF TERMINALS.
Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION & Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/LASER MARKED. DETAILS OF PIN #1 IDENTIFIER IS OPTIONAL, BUT MUST BE LOCATED WITHIN ZONE INDICATED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.05mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220; EXCEPT DIMENSION "b".
11. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
12. THIS PACKAGE OUTLINE APPLIES TO ANVIL SINGULATION (STEPPED SIDES).

	
<small>PROPRIETARY INFORMATION</small>	
<small>TITLE</small> PACKAGE OUTLINE, 16,20,28,32L QFN, 5x5x0.90 MM	
<small>APPROVAL</small>	<small>DOCUMENT CONTROL NO.</small> 21-0091
<small>REV.</small> 1	<small>2/2</small>

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