

DS21352DK T1 Single-Chip Transceiver Design Kit Daughter Card

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GENERAL DESCRIPTION

The DS21352 design kit is an evaluation board for the DS21352. The DS21352DK is intended to be used as a daughter card with either the DK2000 or the DK101 motherboards. The board is complete with a single-chip transceiver (SCT), transformers, termination resistors, configuration switches, line protection circuitry, network connectors, and an interface to the motherboard.

ORDERING INFORMATION

PART	DESCRIPTION
DS21352DK	DS21352 Design Kit Daughter Card

FEATURES

- Expedites New Designs by Eliminating First-Pass Prototyping
- Interfaces Directly to the DK101 or DK2000 Motherboards
- Demonstrates Key Functions of the DS21352
- High-Level Software Provides Visual Access to Registers
- Software Controlled (Register Mapped) Configuration Switches to Facilitate Clock and Signal Routing
- Bantam and RJ48 Connectors for 100Ω T1
- Network Interface Protection for Overvoltage and Overcurrent Events
- Testpoints and Prototype Area Available for Further Customization

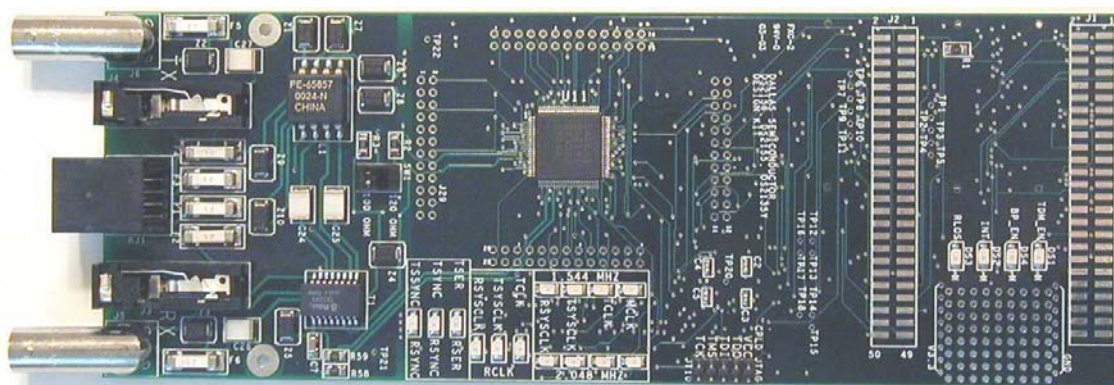


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COMPONENT LIST

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
C1–C5, C8–C12, C15–C19, C21, C22, C29–C34	23	0.1 μ F 10%, 16V ceramic capacitors (0603)	Digi-Key	311-1088-1-ND
C7, C36	2	1 μ F 10%, 16V ceramic capacitors (1206)	Digi-Key	PCC1882CT-ND
C13, C14	2	0.1 μ F 10%, 16V ceramic capacitors (0805)	Digi-Key	311-1142-1-ND
C23	1	0.1 μ F 10%, 25V ceramic capacitor (1206)	Digi-Key	PCC1883CT-ND
C24–C27	4	0.22 μ F, 50V ceramic capacitors	Digi-Key	UNK
C35	1	10 μ F 20%, 16V tantalum capacitor (B case)	Digi-Key	PCS3106CT-ND
DS1, DS4–DS18	16	LED, green, SMD	Digi-Key	P501CT-ND
DS2, DS3	2	LED, red, SMD	Digi-Key	P500CT-ND
F1–F6	6	250V, 1.25A fuse, SMT	Teccor Electronics	F1250T
J1, J2	2	Male 0.1, SMD, 50-pin, dual-row vertical	Samtec	TSM-125-01-T-DV
J3, J4	2	Bantam connectors	SWK	RTT34B02
J5, J6	2	Connector BNC RA 5-pin	Kruvand	UCBJR220
J7–J9	3	Socket, SMD, 50-pin, dual-row vertical	Samtec	TFM-125-02-S-D-LC
JT10	1	Connector, 10-pin, dual-row vertical	Digi-Key	S2012-05-ND
L1	1	Choke, dual 4-line 24 μ H, 8-pin SO	Pulse Engineering	PE-65857
R1, R14, R21	3	51.1 Ω 1%, 1/8W resistors (1206)	Digi-Key	P51.1FCT-ND
R2, R3, R58, R59	4	0 Ω 5%, 1/8W resistors (1206)	Digi-Key	P0.0ETR-ND
R4, R5, R60	3	51.1 Ω 1%, 1/10W resistors (0805)	Digi-Key	P51.1CCT-ND
R6, R9, R10, R13, R15–R19, R22, R23, R25–R29, R32, R37, R38, R44, R47–R49, R61	24	10k Ω 1%, 1/10W resistors (0805)	Digi-Key	P10.0KCCT-ND
R7, R8, R11, R12, R30, R31, R35, R36, R39–R43, R45, R50–R53	18	330 Ω 0.1%, 1/10W MF resistors (0805)	Digi-Key	P330ZCT-ND
R24	1	1.0k Ω 1%, 1/10W resistor (0805)	Digi-Key	P1.00KCCT-ND
R33, R34	2	NOPOP	—	NOPOP
R46	1	4.7k Ω 1%, 1/8W resistor (0805)	Digi-Key	9C08052A4701FK HFT
R54, R55	2	61.9 Ω 1%, 1/8W resistors (1206)	Digi-Key	P61.9FCT-ND
R56, R57	2	49.9 Ω 1%, 1/8W resistors (1206)	Digi-Key	P49.9FCT-ND
RJ1	1	RJ48 connector	Molex	43223
SW1	1	Switch DPDT slide 6-pin TH	Avnet	SSA22
T1	1	XFMR 16-pin SMT	Pulse Engineering	TX1099
U1–U4, U6	5	BBUS switch 10-bit CMOS, 150-mil, 24-pin SO	IDT	IDTQS3R861Q
U5	1	144-pin macrocell CPLD	Avnet	XC95144XL-10TQ100C
U7–U10	4	Quad bus switch, 150-mil, 16-pin SO	IDT	IDTQS3125Q
U11	1	T1/E1/J1 XCVR 100-pin QFP, 0°C to +70°C	Dallas Semiconductor	DS2156L
Z1, Z6–Z8	4	160V, 500A Sidactor	Teccor Electronics	P1800SCMC
Z2, Z3	2	58V, 500A Sidactor	Teccor Electronics	P0640SCMC
Z4, Z5	2	6V, 50A Sidactor	Teccor Electronics	P0080SAMC
Z9, Z10	2	25V, 500A Sidactor	Teccor Electronics	P0300SCMC

BASIC OPERATION

This design kit relies upon several supporting files, which can be downloaded from our website at www.maxim-ic.com/DS21352DK.

Hardware Configuration

Using the DK101 processor board:

- Connect the daughter card to the DK101 processor board.
- Supply 3.3V to the banana-plug receptacles marked GND and VCC_3.3V. (The external 5V connector and the TIM 5V supply headers are unused.)
- All processor board DIP switch settings should be in the ON position with exception for the flash programming switch, which should be OFF.
- From the Programs menu launch the host application named ChipView.exe. Run the ChipView application. If the default installation options were used, click the Start button on the Windows toolbar and select Programs→ChipView→ChipView.

Using the DK2000 processor board:

- Connect the daughter card to the DK2000 processor board.
- Connect J1 to the power supply that is delivered with the kit. Alternately, a PC power supply can be connected to connector J2.
- From the Programs menu launch the host application named ChipView.exe. Run the ChipView application. If the default installation options were used, click the Start button on the Windows toolbar and select Programs→ChipView→ChipView.

General:

- Upon power-up the RLOS LED is lit, as well as the MCLK-2.048MHz and TCLK-2.048MHz LEDs.

Quick Setup (Demo Mode)

- The PC loads the program, offering a choice among Demo Mode, Register View, and Terminal Mode. Select Demo Mode.
- The program requests a configuration file, then select DS21352DK_DRVR.cfg.
- The Demo Mode screen appears. Upon external loopback, the LOS and OOF indicators extinguish.

Quick Setup (Register View)

- The PC loads the program, offering a choice among Demo Mode, Register View, and Terminal Mode. Select Register View.
- The program requests a definition file, then select DS21352.def.
- The Register View screen appears, showing the register names, acronyms, and values. Note: During the definition file load process, all registers are initialized according to the init value filed in the definition file (because the SETUP field in the .def file is turned on).
- Predefined register settings for several functions are available as initialization files.
 - INI files are loaded by selecting the menu **File→Reg Ini File→Load Ini File**.
 - Load the INI file DS21352t1_b8zs_esf.ini.
 - After loading the INI file the following may be observed:
 - The RLOS LED extinguishes upon external loopback.
 - The device is now configured for T1 B8ZS ESF.

Miscellaneous:

- Clock frequencies and certain pin bias levels are provided by a register-mapped CPLD, which is on the DS21352 daughter card.
- The definition file for this CPLD is named DS215x_35x_CPLD_V2.def. See the [CPLD Register Map](#) section for definitions.
- All files referenced above are available for download in the section marked "File Locations."

REGISTER MAP

The DK101 daughter card address space begins at 0x81000000.

The DK2000 daughter card address space begins at:

0x30000000 for slot 0

0x40000000 for slot 1

0x50000000 for slot 2

0x60000000 for slot 3

All offsets given in [Table 1](#) are relative to the beginning of the daughter card address space.

Table 1. Daughter Card Address Map

OFFSET	DEVICE	DESCRIPTION
0X0000 to 0X0015	CPLD	Board identification and clock/signal routing
0X1000 to 0X10ff	Single-Chip Transceiver	Board is populated with one of the following: DS2155, DS2156, DS21352, or DS21354. Please see the data sheet(s) for details.

Registers in the CPLD can be easily modified using ChipView.exe, a host-based user interface software, along with the definition file named *DS215x_35x_CPLD_V2.def*. Definition files for the SCT are named *DS2155.def*, *DS21352.def*, or *DS21354.def*, depending on the board population option.

CPLD Register Map

Table 2. CPLD Register Map

OFFSET	NAME	TYPE	DESCRIPTION
0X0000	BID	Read-Only	Board ID
0X0002	XBIDH	Read-Only	High-Nibble Extended Board ID
0X0003	XBIDM	Read-Only	Middle-Nibble Extended Board ID
0X0004	XBIDL	Read-Only	Low-Nibble Extended Board ID
0X0005	BREV	Read-Only	Board FAB Revision
0X0006	AREV	Read-Only	Board Assembly Revision
0X0007	PREV	Read-Only	PLD Revision
0X0011	SWITCH1	Read-Write	Pin to 1.544MHz
0X0012	SWITCH2	Read-Write	Pin to 2.048MHz
0X0013	SWITCH3	Read-Write	Pin-to-Pin Connect
0X0014	SWITCH4	Read-Write	Pin-to-Pin Connect
0X0015	LEVELS	Read-Write	Set Level On Pin 1 = 3.3V

ID Registers

OFFSET	NAME	TYPE	VALUE	DESCRIPTION
0X0000	BID	Read-Only	0xD	Board ID
0X0002	XBIDH	Read-Only	0x0	High-Nibble Extended Board ID
0X0003	XBIDM	Read-Only	0x0	Middle-Nibble Extended Board ID
0X0004	XBIDL	Read-Only	0x5	Low-Nibble Extended Board ID
0X0005	BREV	Read-Only	Displays current FAB revision	Board FAB Revision
0X0006	AREV	Read-Only	Displays current assembly revision	Board Assembly Revision
0X0007	PREV	Read-Only	Displays current PLD firmware revision	PLD Revision

Control Registers

The control registers are used primarily to control several banks of FET switches that route clocks and backplane signals. Please note that certain register settings cause line contention, e.g., setting SWITCH1.4 and SWITCH2.4 both to 0 would drive MCLK with both 1.544MHz and 2.048MHz.

SWITCH1: PIN TO 1.544MHz (OFFSET = 0x0011) INITIAL VALUE = 0xF

(MSB)

(LSB)

—	—	—	—	MCLK	TCLK	RSYSCLK	TSYSCLK
---	---	---	---	------	------	---------	---------

NAME	POSITION	FUNCTION
MCLK	SWITCH1.3	0 = Connect MCLK to the 1.544MHz clock 1 = Open Switch 1.4
TCLK	SWITCH1.2	0 = Connect TCLK to the 1.544MHz clock 1 = Open Switch 1.3
RSYSCLK	SWITCH1.1	0 = Connect RSYSCLK to the 1.544MHz clock 1 = Open Switch 1.2
TSYSCLK	SWITCH1.0	0 = Connect TSYSCLK to the 1.544MHz clock 1 = Open Switch 1.1

SWITCH2: PIN TO 2.048MHz (Offset = 0X0012) INITIAL VALUE = 0x3

(MSB)

(LSB)

—	—	—	—	MCLK	TCLK	RSYSCLK	TSYSCLK
---	---	---	---	------	------	---------	---------

NAME	POSITION	FUNCTION
MCLK	SWITCH2.3	0 = Connect MCLK to the 2.048MHz clock 1 = Open Switch 2.4
TCLK	SWITCH2.2	0 = Connect TCLK to the 2.048MHz clock 1 = Open Switch 2.3
RSYSCLK	SWITCH2.1	0 = Connect RSYSCLK to the 2.048MHz clock 1 = Open Switch 2.2
TSYSCLK	SWITCH2.0	0 = Connect TSYSCLK to the 2.048MHz clock 1 = Open Switch 2.1

SWITCH3: PIN-TO-PIN CONNECT (Offset = 0X0013) INITIAL VALUE = 0xF

(MSB)

(LSB)

—	—	—	—	TSS_RS	TCL_RC	RSY_RC	TSY_RC
---	---	---	---	--------	--------	--------	--------

NAME	POSITION	FUNCTION
TSS_RS	SWITCH3.3	0 = Connect TSSYNC to RSYNC 1 = Open Switch 3.4
TCL_RC	SWITCH3.2	0 = Connect TCLK to RCLK 1 = Open Switch 3.3
RSY_RC	SWITCH3.1	0 = Connect RSYSCLK to RCLK 1 = Open Switch 3.2
TSY_RC	SWITCH3.0	0 = Connect TSYSCLK to RCLK 1 = Open Switch 3.1

SWITCH4: PIN-TO-PIN CONNECT (Offset = 0X0014) INITIAL VALUE = 0x3**(MSB)****(LSB)**

—	—	—	—	URCLK_2048	UTCLK_2048	RSER_TSER	RSYNC_TSYNC
---	---	---	---	------------	------------	-----------	-------------

NAME	POSITION	FUNCTION		
URCLK_2048	SWITCH4.3	0 = Connect UR_CLK (TSSYNC) to 2.048MHz 1 = Open Switch 4.4		
UTCLK_2048	SWITCH4.2	0 = Connect UT_CLK (TCHCLK) to 2.048MHz 1 = Open Switch 4.3		
RSER_TSER	SWITCH4.1	0 = Connect RER to TSER 1 = Open Switch 4.2		
RSYNC_TSYNC	SWITCH4.0	0 = Connect RSYNC to TSYNC 1 = Open Switch 4.1		

LEVELS: SET LEVEL ON PIN (Offset = 0X0015) INITIAL VALUE = 0x6**(MSB)****(LSB)**

—	—	—	—	—	BP_EN	PPCTDM_EN	TUSEL
---	---	---	---	---	-------	-----------	-------

NAME	POSITION	FUNCTION
—	LEVELS1.3	—
BP_EN	LEVELS1.2	0 = Enable IDT switches that connect the UTOPIA bus to daughter card header
PPCTDM_EN	LEVELS1.1	0 = Enable IDT switches that connect the TDM bus to the daughter card header
TUSEL	LEVELS1.0	0 = Set DS2156.TUSEL to enable TDM backplane 1 = Set DS2156.TUSEL to enable UTOPIA backplane

Note (DS2156 only): When the UTOPIA backplane is enabled (LEVELS.TUSEL = 1) there is a possibility for contention between the UTOPIA bus master and TSYCLK, TSER, and RSER. To avoid this, the following switches should be opened when the UTOPIA backplane is enabled: SWITCH1.0, SWITCH2.0, SWITCH3.0, and SWITCH4.1

DS21352 INFORMATION

For more information about the DS21352, please consult the DS21352 data sheets available on our website at www.maxim-ic.com/DS21352. Software downloads are also available for this design kit.

DS21352DK INFORMATION

For more information about the DS21352DK, including software downloads, please consult the DS21352DK data sheet available on our website at www.maxim-ic.com/DS21352DK.

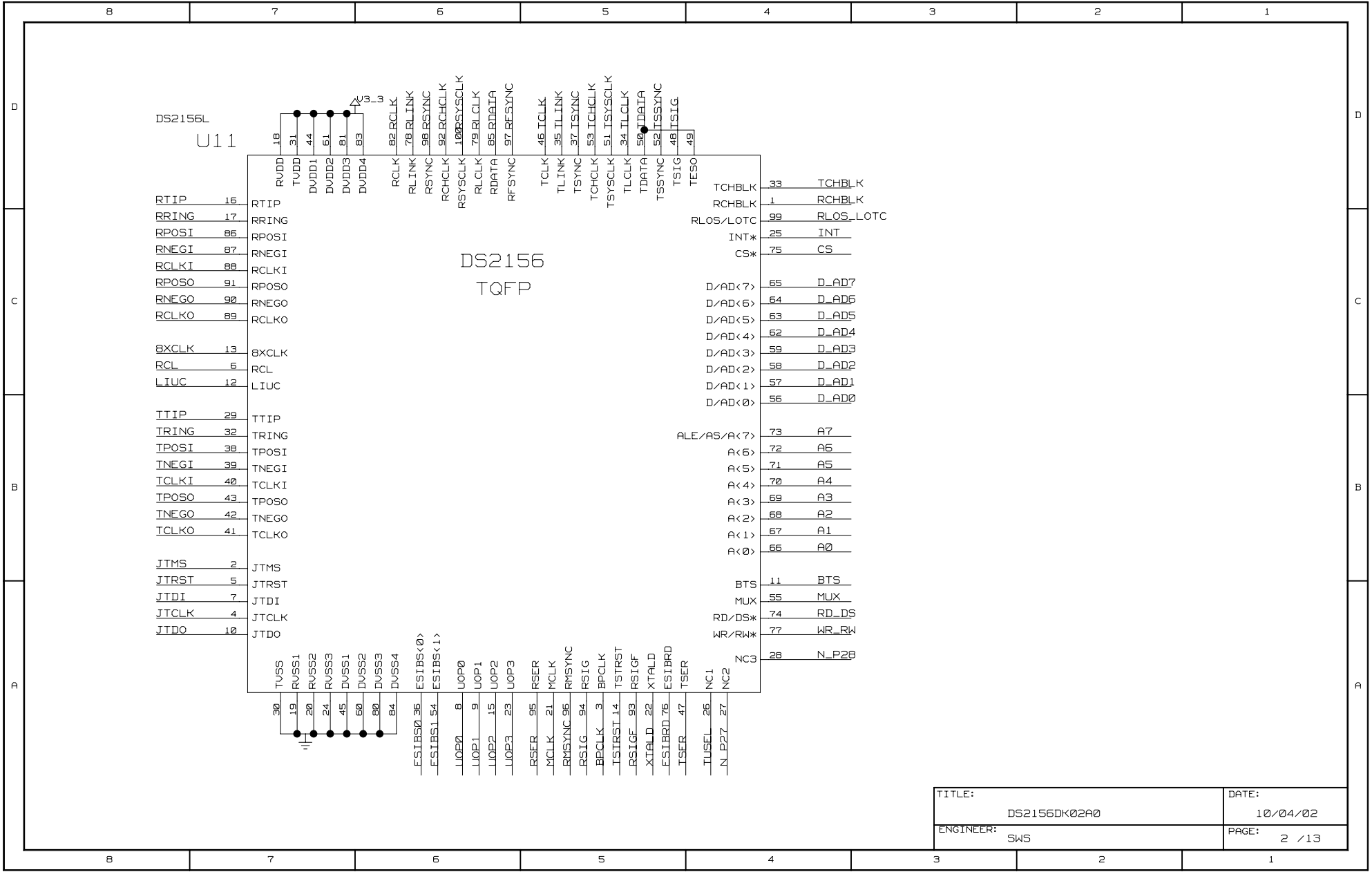
TECHNICAL SUPPORT

For additional technical support, please e-mail your questions to telecom.support@dalsemi.com.

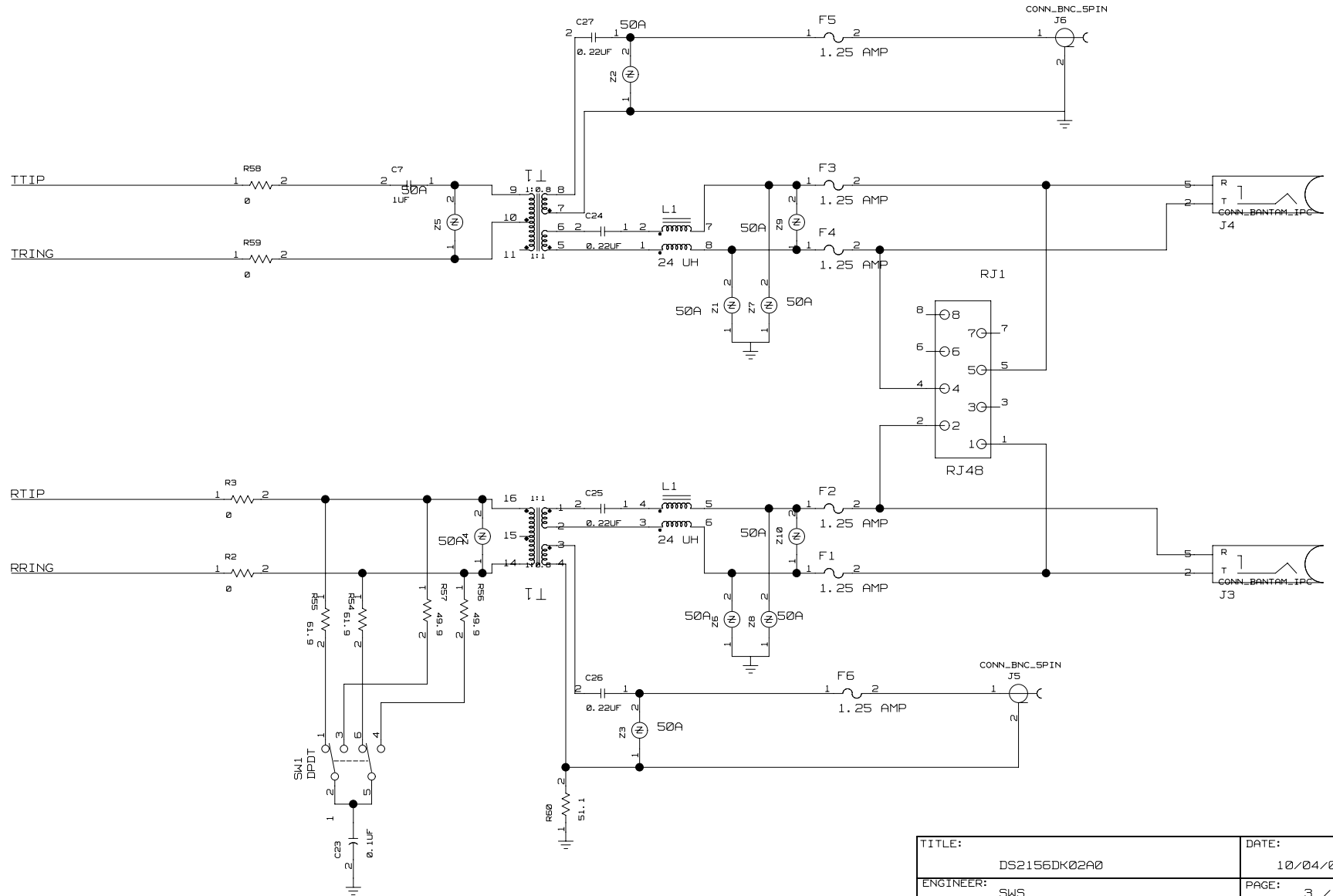
SCHEMATICS

The DS21352DK schematics are featured in the following 13 pages.

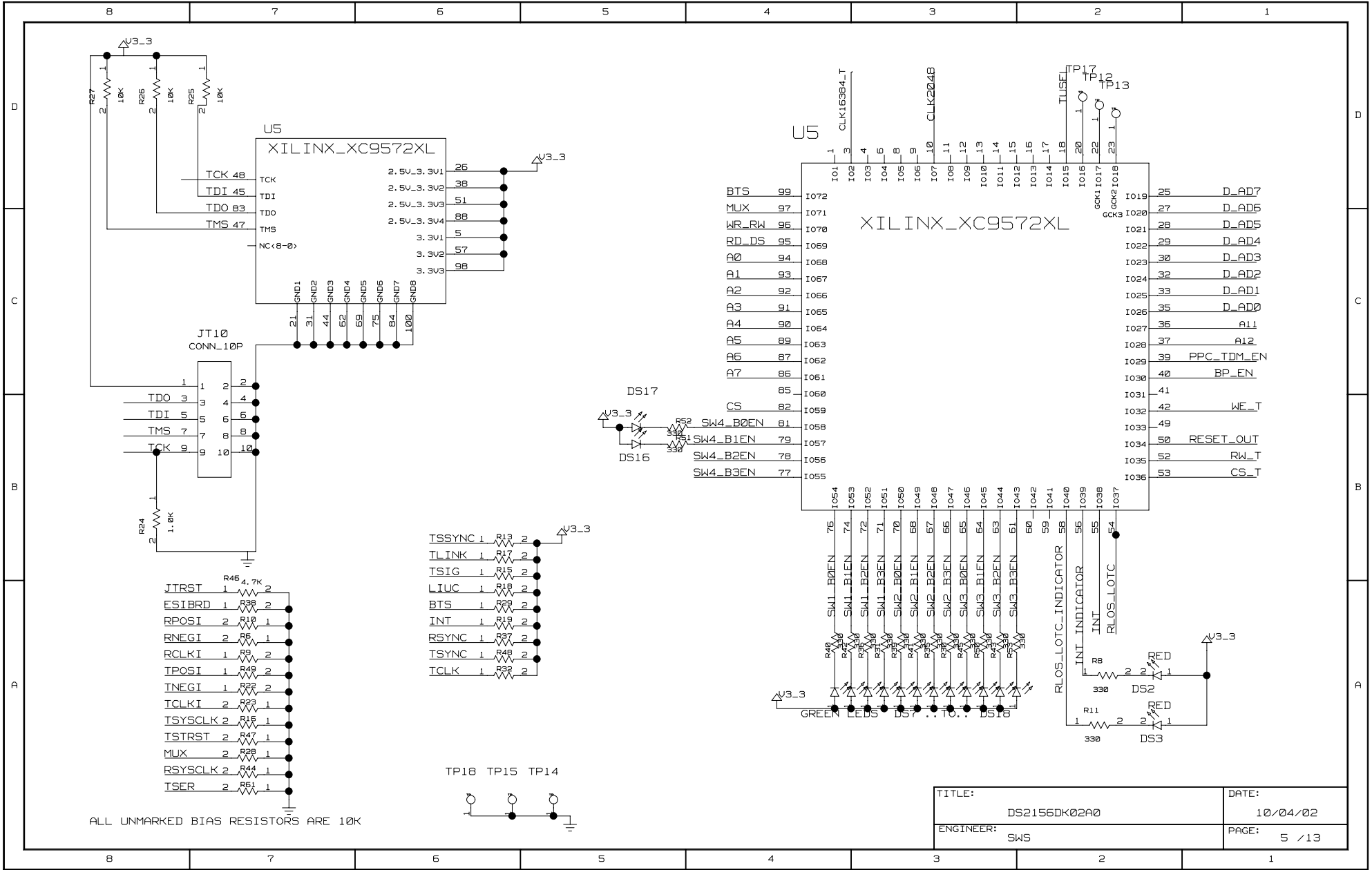
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D																
C	DS2156, DS2155, DS2135Y DESIGN KIT															
B																
A	<div>CONTENTS</div> <div>1. COVER PAGE</div> <div>2. SCT POPULATION OPTION (DS2155, DS2156, DS21352 OR DS21354)</div> <div>3. TX AND RX ANALOG PATHS</div> <div>4. TIM ADDRESS AND DATA BUS</div> <div>5. CPLD ADDRESS DATA CONNECTIONS, BIAS LEVELS FOR SCT</div> <div>6. UTOPIA: TIM HEADER AND BUS SWITCHES</div> <div>7. TESTPOINTS FOR UTOPIA 2</div> <div>8. UTOPIA: NETLIST ASSOCIATIONS</div> <div>9. SWITCHING FOR CLOCKS AND TDM</div> <div>10. SUPPLY DECOUPLING</div> <div>11. SCT TESTPOINTS</div> <div>12. NETLIST CROSS-REFERENCE</div> <div>13. PART CROSS-REFERENCE</div> <div><table><tr><td>TITLE:</td><td>DS2156DK02A0</td><td>DATE:</td><td>10/04/02</td></tr><tr><td>ENGINEER:</td><td>SWS</td><td>PAGE:</td><td>1 / 13</td></tr></table></div>								TITLE:	DS2156DK02A0	DATE:	10/04/02	ENGINEER:	SWS	PAGE:	1 / 13
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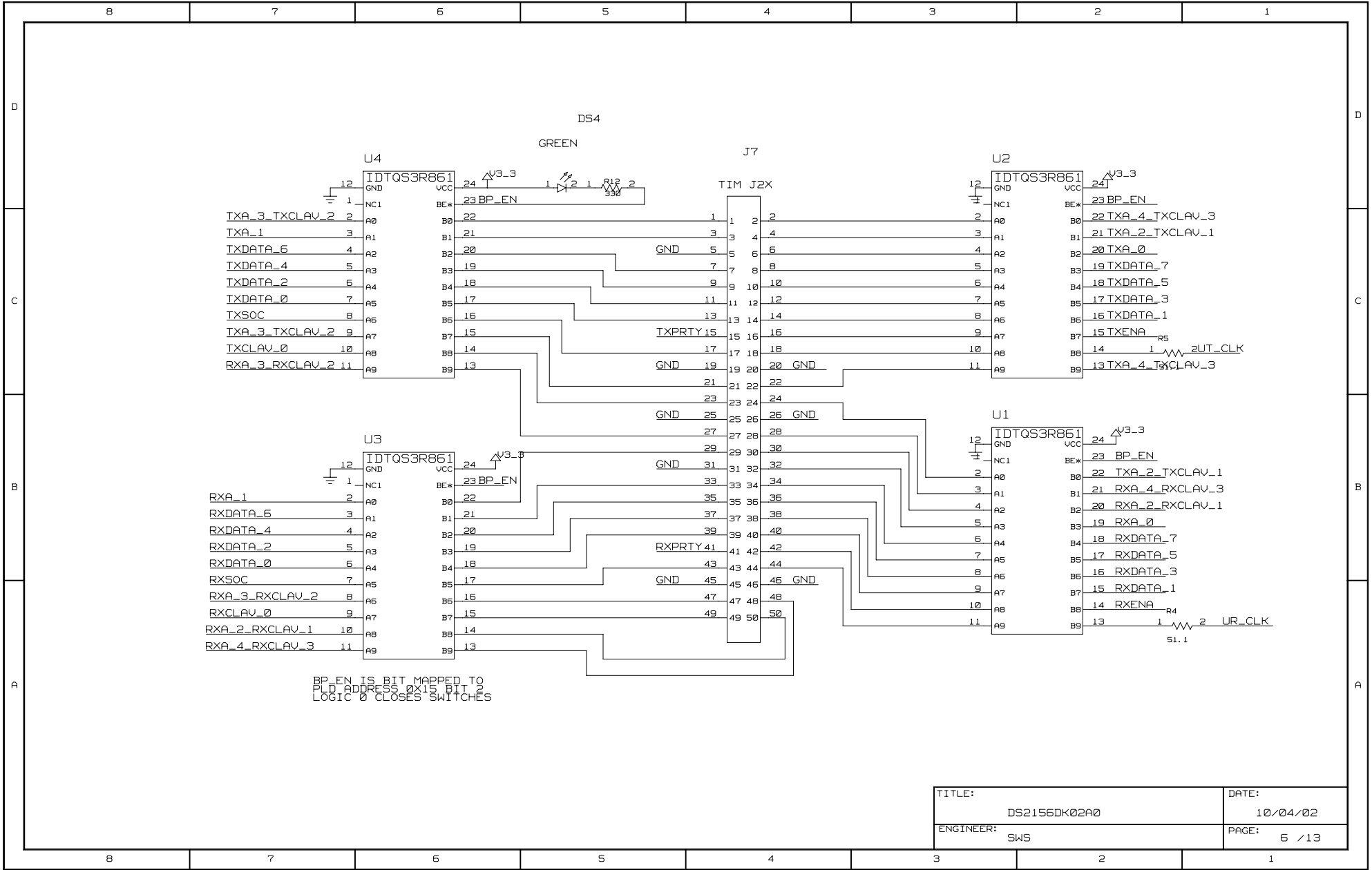


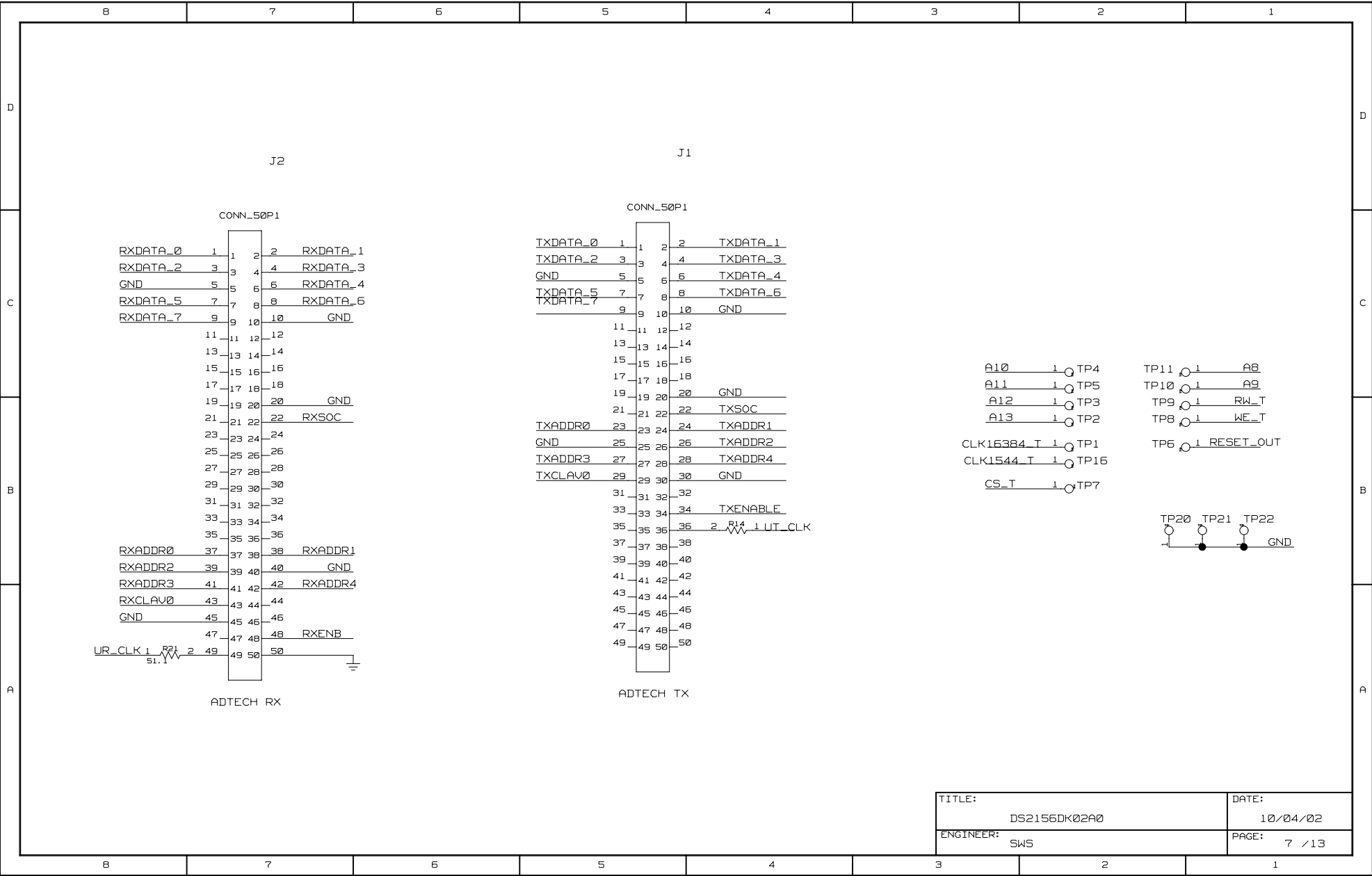
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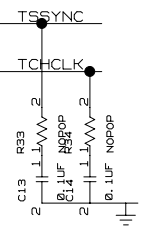
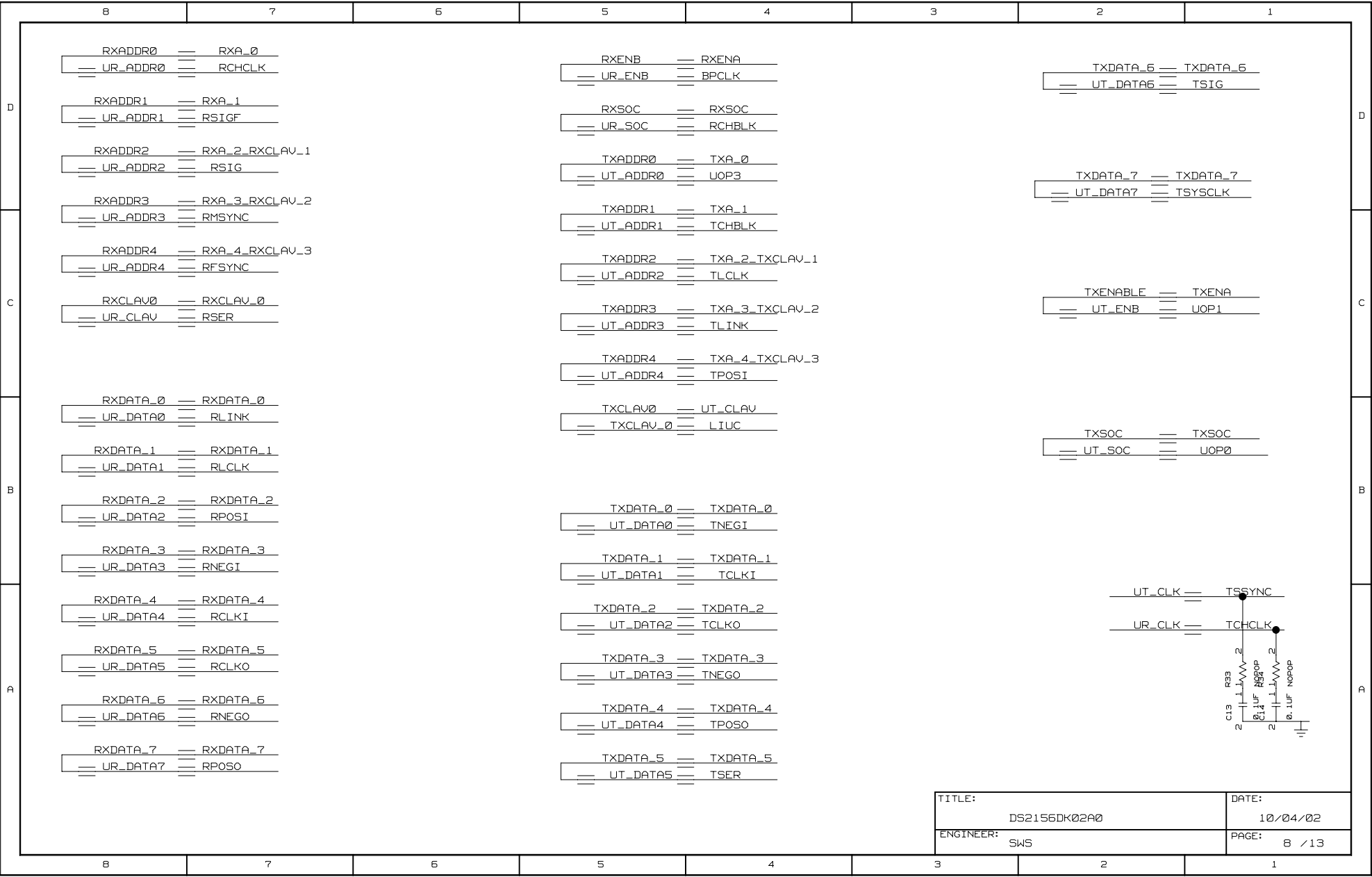


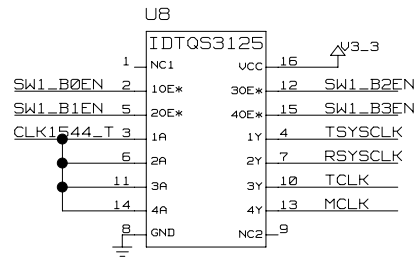
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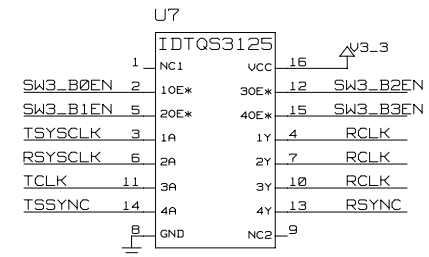




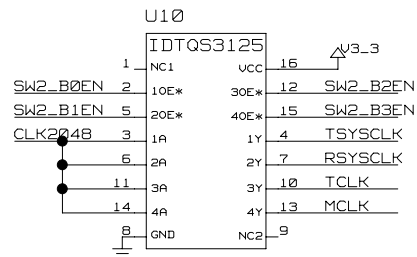




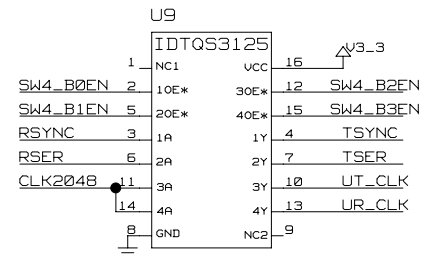
SWITCH 1 IS MEMORY MAPPED
TO PLD REGISTER 0X11
LOGIC 0 CLOSSES SWITCH
LOGIC 1 OPENS SWITCH



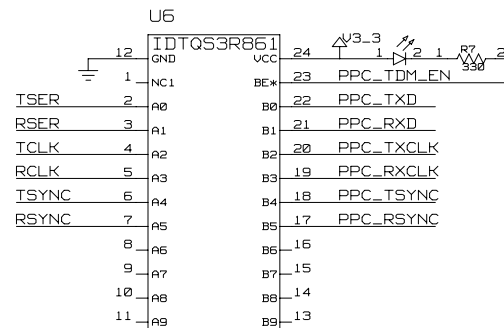
SWITCH 3 IS MEMORY MAPPED
TO PLD REGISTER 0X13
LOGIC 0 CLOSSES SWITCH
LOGIC 1 OPENS SWITCH



SWITCH 2 IS MEMORY MAPPED
TO PLD REGISTER 0X12
LOGIC 0 CLOSSES SWITCH
LOGIC 1 OPENS SWITCH



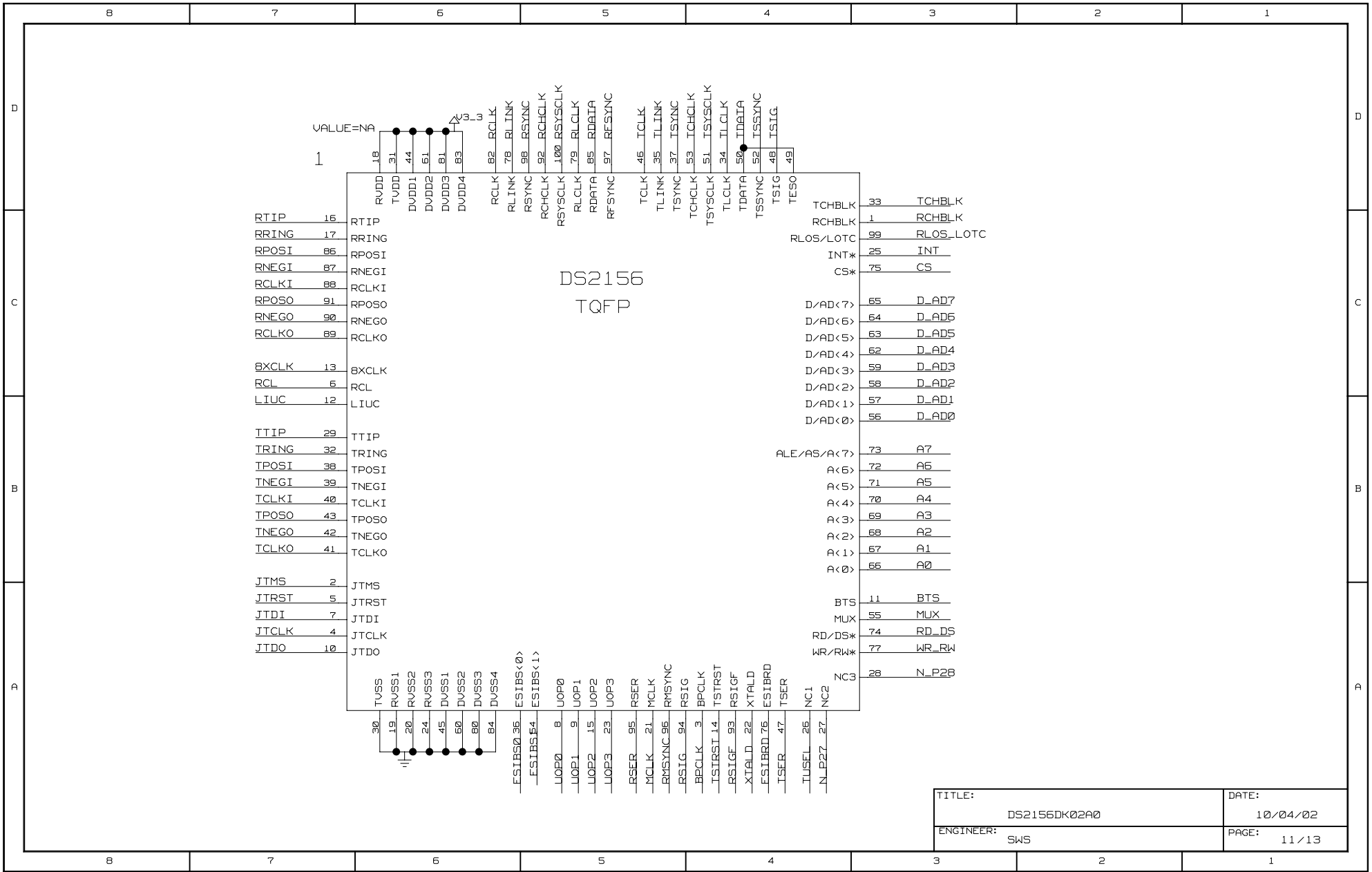
SWITCH 4 IS MEMORY MAPPED
TO PLD REGISTER 0X14
LOGIC 0 CLOSSES SWITCH
LOGIC 1 OPENS SWITCH



PPC TDM EN IS BIT MAPPED TO
PLD ADDRESS 0X15 BIT 1
LOGIC 0 CLOSSES SWITCHES

GREEN DS1

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8		7		6		5		4		3		2		1	
D	*** Part Cross-Reference for the entire design ***														
	1	DS2156_TOFP 11D7													
	C1	CAP 10B5													
	C2	CAP 10B3													
	C3	CAP 10B2													
	C4	CAP 10B2													
	C5	CAP 10B2													
	C7	CAP 3D5													
	C8	CAP 10B4													
	C9	CAP 10B4													
C	C10	CAP 10B4													
	C11	CAP 10B4													
	C12	CAP 10B2													
	C13	CAP 8A1													
	C14	CAP 8A1													
	C15	CAP 10B3													
	C16	CAP 10B3													
	C17	CAP 10B2													
	C18	CAP 10B3													
	C19	CAP 10B3													
B	C21	CAP 10B2													
	C22	CAP 10B5													
	C23	CAP 3A6													
	C24	CAP 3C5													
	C25	CAP 3B5													
	C26	CAP 3A5													
	C27	CAP 3D5													
	C29	CAP 10B4													
	C30	CAP 10B4													
	C31	CAP 10B6													
A	C32	CAP 10B5													
	C33	CAP 10B5													
	C34	CAP 10B5													
	C35	CAP 10B6													
	C36	CAP 10B6													
	DS1	LED 9B4													
	DS2	LED 5A2													
	DS3	LED 5A2													
	DS4	LED 6D5													
	DS5	LED 5A3													
DS6	LED 5A4														
DS7	LED 5A3														
DS8	LED 5A4														
DS9	LED 5A4														
DS10	LED 5A3														
DS11	LED 5A4														
DS12	LED 5A3														
DS13	LED 5A3														
DS14	LED 5A3														
DS15	LED 5A3														
DS16	LED 5B5														
DS17	LED 5B5														
DS18	LED 5A3														
F1	FUSE 3B4														
F2	FUSE 3B4														
F3	FUSE 3D4														
F4	FUSE 3C4														
F5	FUSE 3D4														
F6	FUSE 3A3														
J1	CONN_50P1 7D5														
J2	CONN_50P1 7D7														
J3	CONN_BANTAM_IPC 3B1														
J4	CONN_BANTAM_IPC 3C1														
J5	CONN_BNC_SPIN 3A3														
J6	CONN_BNC_SPIN 3D2														
J7	CONN_50P2 6D4														
J8	CONN_50P2 4D3														
J9	CONN_50P2 4D7														
JT10	CONN_10P 5C8														
L1	CHOKE_DURL_T1 3B4 3C4														
R1	RES1 4B2														
R2	RES 3B7														
R3	RES 3B7														
R4	RES 6A2														
R5	RES 6C2														
R6	RES1 5A7														
R7	RES 9B4														
R8	RES1 5A2														
R9	RES1 5A7														
R10	RES1 5A7														
R11	RES1 5A2														
R12	RES 6D5														
R13	RES1 5B6														
R14	RES1 7B4														
R15	RES1 5B6														
R16	RES1 5A7														
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R19	RES1 5A6														
R21	RES1 7A8														
R22	RES1 5A7														
R23	RES1 5A7														
R24	RES1 5B8														
R25	RES1 5D7														
R26	RES1 5D8														
R27	RES1 5D8														
R28	RES1 5A7														
R29	RES1 5A6														
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R31	RES 5A3														
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R54	RES1 3B6														
R55	RES1 3B6														
R56	RES 3B5														
R57	RES 3B6														
R58	RES 3D7														
R59	RES 3C7														
R60	RES 3A5														
R61	RES1 5A7														
RJ1	RJ48_CON 3C3														
SK1	SWITCH_DPDT_SLIDE_6P 3A6														
T1	XFMR_2IN_4OUT_U 3B5 3D5														
TP1	TSTPNT_SNG 7B2														
TP2	TSTPNT_SNG 7B2														
TP3	TSTPNT_SNG 7B2														
TP4	TSTPNT_SNG 7C2														
TP5	TSTPNT_SNG 7C2														
TP6	TSTPNT_SNG 7B2														
TP7	TSTPNT_SNG 7B2														
TP8	TSTPNT_SNG 7B2														
TP9	TSTPNT_SNG 7B2														
TP10	TSTPNT_SNG 7B2														
TP11	TSTPNT_SNG 7B2														
TP12	TSTPNT_SNG 5D2														
TP13	TSTPNT_SNG 5D2														
TP14	TSTPNT_SNG 5A6														
TP15	TSTPNT_SNG 5A6														
TP16	TSTPNT_SNG 7B2														
TP17	TSTPNT_SNG 5D2														
TP18	TSTPNT_SNG 5A6														
TP20	TSTPNT_SNG 7B2														
TP21	TSTPNT_SNG 7B1														
TP22	TSTPNT_SNG 7B1														
TP23	TSTPNT_SNG 10A7														
TP24	TSTPNT_SNG 10A8														
TP25	TSTPNT_SNG 10A7														
TP26	TSTPNT_SNG 10A7														
TP27	TSTPNT_SNG 10A7														
TP28	TSTPNT_SNG 10A7														
TP29	TSTPNT_SNG 10A7														
TP30	TSTPNT_SNG 10A7														
TP31	TSTPNT_SNG 10A4														
TP32	TSTPNT_SNG 10A4														
TP33	TSTPNT_SNG 10A5														
TP34	TSTPNT_SNG 10A5														
TP35	TSTPNT_SNG 10A5														
TP36	TSTPNT_SNG 10A5														
TP37	TSTPNT_SNG 10A5														
TP38	TSTPNT_SNG 10A5														
U1	IDTQ53R861.U 6B3														
U2	IDTQ53R861.U 6D3														
U3	IDTQ53R861.U 6B6														
U4	IDTQ53R861.U 6D6														
U5	XILINX_XC9572XL 5D4 5D7														
U6	IDTQ53R861.U 9B5														
U7	IDTQ53125.U 9D3														
U8	IDTQ53125.U 9D7														
U9	IDTQ53125.U 9B3														
U10	IDTQ53125.U 9B7														
U11	DS2156_TOFP 2D7														
Z1	SIDACTOR_2 3C4														
Z2	SIDACTOR_2 3D5														
Z3	SIDACTOR_2 3A5														
Z4	SIDACTOR_2 3B5														
Z5	SIDACTOR_2 3C6														
Z6	SIDACTOR_2 3A4														
Z7	SIDACTOR_2 3C4														
Z8	SIDACTOR_2 3A4														
Z9	SIDACTOR_2 3C4														
Z10	SIDACTOR_2 3B4														
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