

SCOPE: QUAD SPST CMOS ANALOG SWITCHES

<u>Device Type</u>	<u>Generic Number</u>	<u>SMD Number</u>
01	DG201AA(x)/883B	7705301
02	HI(x)-201A/883B	7705302

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

<u>Outline Letter</u>	<u>Mil-Std-1835</u>	<u>Case Outline</u>	<u>Package Code</u>
SMD (x for 01) (x for 02)			
X L	CDFP4-F16	16 LEAD FLATPACK	F16
E K 1	GDIP1-T16 or CDIP2-T16	16 LEAD CERDIP	J16
2 Z 4	CQCC1-N20	20-Pin Ceramic LCC	L20

Absolute Maximum Ratings

Supply Voltage (Between V^+ and V^-) for 01	44V
Supply Voltage (Between V^+ and V^-) for 02	40V
Digital Input Voltage (V_{IN}) for 01 $\frac{1}{2}$	$V^- - 0.3V$ dc to V^+
Digital Input Voltage (V_{IN}) for 02 $\frac{1}{2}$	$V^- - 4V$ dc to $V^+ + 4V$
Analog Input Voltage (V_S)	$V^- - 2V$ dc to $V^+ + 2V$
Current, Any terminal except S or D for 01	30mA
Current, Any terminal except S or D for 02	25mA
Continuous Current, S or D for 01	20mA
Continuous Current, S or D for 02	25mA
Peak Current S or D(Pulsed at 1ms, 10% duty cycle max) for 01	70mA
Peak Current S or D(Pulsed at 1ms, 10% duty cycle max) for 02	40mA
Lead Temperature (soldering, 10 seconds)	+300°C
Storage Temperature	-65°C to +150°C

Continuous Power Dissipation	$T_A = +70^\circ\text{C}$
16 lead Flatpack (derate 6.1mW/°C above +70°C)	485mW
16 lead CERDIP(derate 10mW/°C above +70°C)	800mW
20-Pin LCC (derate 9.1mW/°C above +70°C)	727mW
Junction Temperature T_J	+150°C
Thermal Resistance, Junction to Case, θ_{JC} :	
Case Outline 16 lead Flatpack	65°C/W
Case Outline 16 lead CERDIP	50°C/W
Case Outline 20-Pin LCC	20°C/W
Thermal Resistance, Junction to Ambient, θ_{JA} :	
Case Outline 16 lead Flatpack	165°C/W
Case Outline 16 lead CERDIP	100°C/W
Case Outline 20-Pin LCC	110°C/W

Recommended Operating Conditions.

Ambient Operating Range (T_A)	-55°C to +125°C
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NOTE 1: Signals on S_X , D_X , or IN_X exceeding V^+ or V^- are clamped by internal diodes, and are also internally current limited to 25mA.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS

TEST	Symbol	CONDITIONS -55 °C <=T _A <= +125°C V+=+15V, V=-15V, GND=0V Unless otherwise specified	Group A Subgroup	Device type	Limits Min 1/	Limits Max 1/	Units
SWITCH							
Analog-Signal Range	V _{ANALOG}	V _S =±15V NOTE 2	1,2,3	All	-15	15	V
Drain-Source ON Resistance	r _{DS(ON)}	I _D =±1mA, V _D =±10V, V _{IN} =0.8V	1,3 2	01		175 250	Ω
Drain-Source ON Resistance	r _{DS(ON)}	I _D =±1mA, V _S =±10V, V _{IN} =0.8V All unused channels V _A =2.4V	1 2,3	02		70 100	Ω
Source OFF Leakage Current	I _{S(OFF)}	V _S =+/-14V, V _D =-/ +14V, V _{IN} =2.4V	1 2,3	All	-2 -100	2 100	nA
Drain OFF Leakage Current	I _{D(OFF)}	V _S =+/-14V, V _D =-/ +14V, V _{IN} =2.4V	1 2,3	01	-1 -100	1 100	nA
Drain OFF Leakage Current	I _{D(OFF)}	V _S =+/-14V, V _D =-/ +14V, V _{IN} =2.4V	1 2,3	02	-2 -100	2 100	nA
Drain ON Leakage Current	I _{D(ON)}	V _D =V _S =±14V, V _{IN} =0.8V	1 2,3	01	-1 -200	1 200	nA
Drain ON Leakage Current	I _{D(ON)}	V _D =V _S =±14V, V _{IN} =0.8V	1 2,3	02	-2 -200	2 200	nA
INPUT							
Low Level Input Voltage	V _{IL}		1,2,3	All		0.8	V
High Level Input Voltage	V _{IH}		1,2,3	All	2.4		V
Input Leakage Current High	I _{IH}	V _{IN} =2.4V, 15V	1 2	01		±1 ±10	μA
			1 2,3	02		±0.5 ±1.0	
Input Leakage Current Low	I _{IL}	V _{IN} = 0V	1 2	01		±1 ±10	μA
		V _{IN} =0.8V	1 2,3	02		±0.5 ±1.0	
SUPPLY							
Positive Supply Current	I+	V _{IN} =0V	1,2 3	01		4 6.5	mA
		V _{IN} =5V	1,2 3			3 4.5	
Negative Supply Current	I-	V _{IN} =0.8V or 2.4V	1,2 3	02		1.5 2.0	mA

TEST	Symbol	CONDITIONS -55 °C ≤ T _A ≤ +125 °C V ₊ =+15V, V ₋ = -15V, GND=0V Unless otherwise specified	Group A Subgroup	Device type	Limits Min 1/	Limits Max 1/	Units
DYNAMIC							
Turn ON time	t _{ON}	R _L =1kΩ, CL=35pF, V _{IH} =+3V, V _{IL} =0V	9,10,11	01		1000	ns
		R _L =1kΩ, CL=100pF, V _{IH} =+4V, V _{IL} =0V	9 10,11	02		600 800	
Turn OFF time	t _{OFF}	R _L =1kΩ, CL=35pF, V _{IH} =+3V, V _{IL} =0V	9 10,11	01		500 650	ns
		R _L =1kΩ, CL=100pF, V _{IH} =+4V, V _{IL} =0V	9 10,11	02		500 650	

NOTE 1: The limiting terms “min” (minimum) and “max” (maximum) shall be considered to apply to magnitudes only. Negative current shall be defined as conventional current flow out of a device terminal.

NOTE 2: Guaranteed, if not tested, to the limits specified.

FIGURE 1: SWITCHING TIME TEST CIRCUIT: See Commercial Data Sheet

TRUTH TABLE

TERMINAL CONNECTION

Device Type	Logic	Switch		Terminal NUMBER	DG201A & Hlx-201	DG201A & Hlx-201
01 & 02	0	ON			J16 & F16	L20
	1	OFF		1	IN ₁	NC
				2	D ₁	IN ₁
				3	S ₁	D ₁
				4	V-	S ₁
				5	GND	V-
				6	S ₄	NC
				7	D ₄	GND
				8	IN ₄	S ₄
				9	IN ₃	D ₄
				10	D ₃	IN ₄
				11	S ₃	NC
				12	NC (01)	IN ₃
				3/ 12	V _{REF} (02)	IN3
ORDERING	INFORMATION			13	V+	D ₃
SMD #	Maxim #	Pkg.		14	S ₂	S ₃
7705301EA	DG201AAK/883B	J16		15	D ₂	NC (01)
7705301XC	DG201AAL/883B	F16		3/ 15	D ₂	V _{REF} (02)
77053012C	DG201AAZ/883B	L20		16	IN ₂	NC
7705302EA	HI1-201/883B	J16		17		V+
77053022C	HI4-201/883B	L20		18		S ₂
				19		D ₂
				20		IN ₂

NOTE 3: V_{REF} is normally floating, but voltage up to 10V can be applied to raise the threshold voltage.

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

- a. End-point electrical parameters shall be specified in Table 1.
- b. Steady-state life test, Method 1005 of Mil-Std-883:
 1. Test condition A, B, C, D.
 2. TA = +125°C, minimum.
 3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 9
Group A Test Requirements Method 5005	1, 2, 3, 9, 10, 11
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.