19-1438; Rev 0; 3/99

EVALUATION KIT MANUAL FOLLOWS DATA SHEET

Wireless and Satellite Handset Power-Management ICs

General Description

The MAX886/MAX888 power-management ICs are complete power systems for wireless and satellite handsets. The devices operate from 3 to 6-cell NiCd/NiMH batteries or from 1 or 2-cell Li-Ion batteries. They incorporate a high-efficiency, step-down DC-DC converter, a regulated 5V charge pump, and four linear regulators. The regulators supply power to the SIM, LCD, BB, DSP, and RF sections of a cellular telephone handset. The step-down converter and linear regulator outputs are adjustable by internal 4-bit DACs, programmable through the I^2C™-compatible serial interface. A pushbutton on/off scheme activates a 5µA low-power shutdown mode. The devices also feature a low-battery detector output and an internal start-up timer.

The MAX886/MAX888 differ in output voltage range and power-on reset voltage. The MAX886 has a higher preset voltage range and is intended for 2-cell Li-Ion or 5/6-cell NiCd/NiMH batteries. The MAX888 has a lower preset voltage range and is intended for 1-cell Li-Ion or 3/4-cell NiCd/NiMH batteries. Both devices are available in a space-saving, 32-pin TQFP package.

Applications

Satellite Phones
Private Mobile Radio (PMR)
Wireless Handsets
GSM Cellular/PCS Telephones

Pin Configuration appears at end of data sheet.

Features

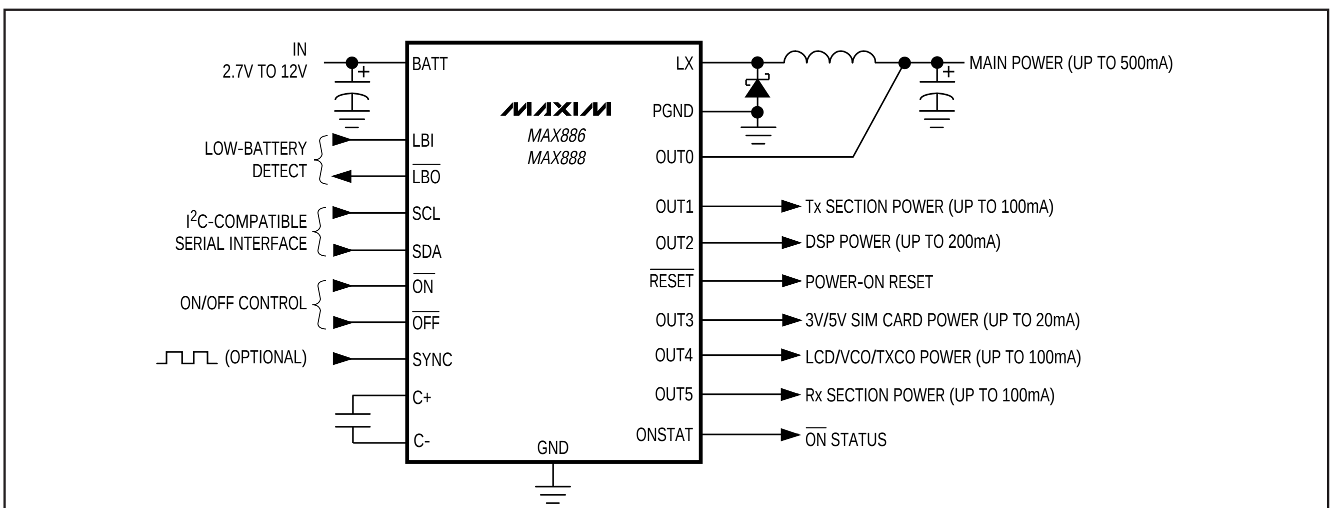
- **90% Efficient, 500mA Step-Down Converter**
- **Two 100mA DAC-Controlled LDOs**
  One 200mA DAC-Controlled LDO
  One 20mA DAC-Controlled LDO
- **3 to 6-Cell NiCd or NiMH Operation**
  1 or 2-Cell Li-Ion Operation
- **+2.7V to +12V Input Voltage Range**
- **250µA Standby (PFM) Quiescent Current**
- **5µA Shutdown Current**
- **I^2C-Compatible Serial Interface**
- **Selectable 375kHz, 535kHz, 670kHz, 925kHz (or Synchronizable) Switching Frequency**
- **Power-On Reset and Start-Up Timer**
- **Thermal Overload Protection**
- **Pushbutton On/Off Control**
- **Space-Saving 32-Pin TQFP Package (7mm x 7mm)**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX886ECJ*	-40°C to +85°C	32 TQFP
MAX888ECJ	-40°C to +85°C	32 TQFP

** Future product—contact factory for availability.*

Typical Operating Circuit



I^2C is a trademark of Philips Corp.

Wireless and Satellite Handset Power-Management ICs

ABSOLUTE MAXIMUM RATINGS

BATT, IN0, IN1 to GND ....-0.3V to +13V
CVH to IN0 ....-6V to +0.3V
PGND, DGND to GND ....-0.3V to +0.3V
ONSTAT to GND ....-0.3V to (V_{OUT2} + 0.3V)
LX to PGND ....-0.3V to (V_{OUT0} + 0.3V)
OUT1 to GND ....-0.3V to (V_{IN1} + 0.3V)
OUT2 to GND ....-0.3V to (V_{IN2} + 0.3V)
OUT3 to GND ....-0.3V to (V_{IN3} + 0.3V)
OUT5 to GND ....-0.3V to (V_{IN5} + 0.3V)
SYNC, $\overline{RESET}$, SCL, SDA, CVL, LBI, LBHYS, OUT0
REF, $\overline{LBO}$, C+, C-, OUT4, IN2, IN3, IN4, IN5,
$\overline{ON}$, $\overline{OFF}$ to GND ....-0.3V to +6V
Continuous Power Dissipation (T_A = +70°C)
TQFP (derate 11.1mW/°C above +70°C) 889mW
Operating Temperature Range. ....-40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10sec) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{BATT} = V_{IN0} = V_{IN1} = +5.5V, GND = PGND = DGND, $V_{\overline{OFF}}$ = V_{SYNC} = 2.8V, V_{IN2} = V_{IN3} = V_{IN4} = V_{IN5} = +3.8V, V_{OUT4} = +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
BATT, IN0, IN1 Operating Voltage Range	V_{BATT}, V_{IN0}, V_{IN1}			2.7		12	V
IN2, IN3, IN4, IN5 Operating Voltage Range	V_{IN2}, V_{IN3}, V_{IN4}, V_{IN5}			2.7		5.5	V
Undervoltage Lockout	V_{UVLOF}	V_{BATT} falling		2.35	2.45		V
	V_{UVLOR}	V_{BATT} rising			2.55	2.65	V
Supply Current, PFM Mode	$I_{BATTPFM}$	SYNC = GND			250	600	µA
Supply Current, PWM Mode	$I_{BATTPWM}$	f_{OSC} = 375kHz			2		mA
		f_{OSC} = 535kHz			3		
		f_{OSC} = 670kHz			4		
		f_{OSC} = 925kHz			5.5	12	
Supply Current, Shutdown Mode	I_{STNBY}	$\overline{OFF}$ = GND	T_A = 0°C to +85°C		5	10	µA
			T_A = -40°C to +85°C			15	
REFERENCE							
Reference Output Voltage	V_{REF}	I_{REF} = 0	T_A = 0°C to +85°C	1.23	1.25	1.27	V
			T_A = -40°C to +85°C	1.225		1.275	
Reference Load Regulation		1µA < I_{REF} < 100µA			5	15	mV
Reference Supply Rejection		2.7V < V_{OUT0} < 3.75V			0.2	5	mV
DC-DC BUCK REGULATOR 0 (IN0, OUT0)							
Input Voltage Range	V_{IN0}			2.7		12	V
Output Accuracy		I_{OUT0} = 0		-3		3	%
Nominal Output Adjustment Range	V_{OUT0}	MAX886		2.625		3.750	V
		MAX888		1.527		3.027	
Output Ready Threshold		V_{OUT0} = 3.75V (MAX886), V_{OUT0} = 2.027V (MAX888)		-7.5	-5	-3	% of V_{OUT0}

ELECTRICAL CHARACTERISTICS (continued)

(V_{BATT} = V_{IN0} = V_{IN1} = +5.5V, GND = PGND = DGND, $V_{\overline{OFF}}$ = V_{SYNC} = 2.8V, V_{IN2} = V_{IN3} = V_{IN4} = V_{IN5} = +3.8V, V_{OUT4} = +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Load Regulation		I_{OUT0} = 0.1mA to 500mA			-1.5		%
Line Regulation		3V < V_{IN0} < 12V		-0.3	0	0.3	%
Maximum Duty Cycle		V_{LX} = 12V		100			%
LX Leakage Current		V_{LX} = 12V			0.1	10	µA
Internal Switch On-Resistance	R_{ON}	V_{IN0} = 3.8V			0.4	1	Ω
PFM to PWM Threshold		I_{OUT0}		63	98	180	mA
Internal Switch Current Limit	I_{LIMIT}			0.6	0.9	1.2	A
OSCILLATOR FREQUENCY (OUT0, OUT4)							
Oscillator Frequency Accuracy	f_{OSC}	Table 4	T_A = 0°C to +85°C	-20		20	%
			T_A = -40°C to +85°C	-23		23	
SYNC Range				0.8 · f_{OSC}	f_{OSC}	1.2 · f_{OSC}	kHz
LDO REGULATOR 1 (IN1, OUT1)							
Input Voltage Range	V_{IN1}			2.7		12	V
Output Accuracy		I_{OUT1} = 0.1mA to 100mA		-3		3	%
Nominal Output Adjustment Range	V_{OUT1}	MAX886		2.70		4.95	V
		MAX888		1.25		3.5	
Dropout Voltage		I_{OUT1} = 1mA			1		mV
		I_{OUT1} = 100mA			90	200	
Output Load Regulation		I_{OUT1} = 0.1mA to 100mA		-0.01		0.01	%/mA
Line Regulation		3V < V_{IN1} < 12V, 0h code		-0.1	0	0.1	%/V
Current Limit				100	250		mA
LDO REGULATOR 2 (IN2, OUT2)							
Input Voltage Range	V_{IN2}			2.7		5.5	V
Output Accuracy		I_{OUT2} = 0.1mA to 200mA		-3		3	%
Nominal Output Adjustment Range	V_{OUT2}	MAX886		2.175		3.30	V
		MAX888		1.527		3.027	
Output Ready Threshold	V_{RDY2}	V_{OUT2} = 3.3V (MAX886), V_{OUT2} = 1.527V (MAX888)		-7.5	-5	-3	% of V_{OUT2}
Dropout Voltage		I_{OUT2} = 1mA			1		mV
		I_{OUT2} = 200mA			90	200	
Output Load Regulation		I_{OUT2} = 0.1mA to 200mA		-0.005		0.002	%/mA
Line Regulation		2.7V < V_{IN2} < 3.8V, 0h code		-0.3		0.3	%/V
Current Limit				200	500		mA
LDO REGULATOR 3 (IN3, OUT3)							
Input Voltage Range	V_{IN3}			2.7		5.5	V
Output Accuracy		I_{OUT3} = 0.1mA to 20mA		-3		3	%

ELECTRICAL CHARACTERISTICS (continued)

(V_{BATT} = V_{IN0} = V_{IN1} = +5.5V, GND = PGND = DGND, $V_{\overline{OFF}}$ = V_{SYNC} = 2.8V, V_{IN2} = V_{IN3} = V_{IN4} = V_{IN5} = +3.8V, V_{OUT4} = +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Nominal Output Voltage	V_{OUT3}	V_{IN3} = 5.5V, Table 5		0		V
				2.85		
				4.65		
				V_{OUT2}		
Dropout Voltage		I_{OUT3} = 1mA		1		mV
		I_{OUT3} = 20mA		20	50	
Output Load Regulation		I_{OUT3} = 0.1mA to 20mA	-0.035		0.02	%/mA
Line Regulation		3.8V < V_{IN3} < 5.5V, V_{OUT3} = 2.85V	-0.3		0.3	%/V
Current Limit		V_{OUT3} = 2.85V or 4.65V only	20	50		mA
CHARGE-PUMP REGULATOR 4 (IN4, OUT4)						
Switching Frequency				f_{OSC} / 2		kHz
Output Voltage	V_{OUT4}	No load	5.10	5.25	5.41	V
		I_{OUT4} = 50mA		5.21		
LDO REGULATOR 5 (IN5, OUT5)						
Input Voltage Range	V_{IN5}		2.7		5.5	V
Output Accuracy		I_{OUT5} = 0.1mA to 100mA	-3		3	%
Nominal Output Adjustment Range	V_{OUT5}	MAX886	2.175		3.300	V
		MAX888	1.25		3.50	
Dropout Voltage		I_{OUT5} = 1mA		1		mV
		I_{OUT5} = 100mA		72	200	
Output Load Regulation		I_{OUT5} = 0.1mA to 100mA	-0.01		0.01	%/mA
Line Regulation		2.7V < V_{IN5} < 3.8V, 0h code	-0.3		0.3	%/V
Current Limit			100	250		mA
LOW-BATTERY COMPARATOR						
LBI Input Current		V_{LBI} = 1.23V	-0.2		0.2	µA
LBI Threshold			V_{REF} - 15mV	V_{REF}	V_{REF} + 15mV	V
LBI Propagation Delay		V_{LBI} = step from 1.23V to 1.27V		10		µs
$\overline{LBO}$/LBHYS Output Low Voltage		$V_{\overline{LBO}}$ = I_{LBHYS} = 1mA, V_{LBI} = V_{REF} - 15mV			0.5	V
$\overline{LBO}$/LBHYS Leakage Current		$V_{\overline{LBO}}$ = V_{LBHYS} = 12V, V_{LBI} = V_{REF} + 15mV	-0.2		0.2	µA
RESET AND START-UP TIMER						
Reset Timeout Period			56	75	94	ms
Start-Up Timeout Period			28	37	47	ms
LOGIC AND CONTROL INPUTS						
$\overline{ON}$ Input Voltage	V_{IL}				0.4	V
	V_{IH}		1.2			

ELECTRICAL CHARACTERISTICS (continued)

(V_{BATT} = V_{IN0} = V_{IN1} = +5.5V, GND = PGND = DGND, $V_{\overline{OFF}}$ = V_{SYNC} = 2.8V, V_{IN2} = V_{IN3} = V_{IN4} = V_{IN5} = +3.8V, V_{OUT4} = +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

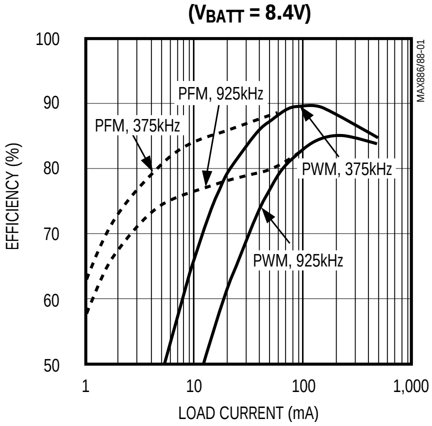
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{ON}$ Input Current	I_{IL}	$V_{\overline{ON}}$ = 0		-16	-40	µA
	I_{IH}	1.2V < $V_{\overline{ON}}$ < V_{OUT2}		-5	-10	
SYNC Input Voltage	V_{IL}				0.8	V
	V_{IH}		2.0			
SYNC Input Current	I_{SYNC}	0 < V_{SYNC} < V_{OUT2}		0.25	1	µA
ONSTAT OUTPUT						
ONSTAT Output Voltage	$V_{ONSTATL}$	I_{ONSTAT} = 1mA			0.5	V
ONSTAT Output Voltage	$V_{ONSTATH}$	I_{ONSTAT} = 0	V_{OUT2} - 0.5			V
$\overline{RESET}$ OUTPUT						
Output Low Voltage	$V_{\overline{RESET}L}$	$I_{\overline{RESET}}$ = 1mA			0.5	V
Output High Voltage	$V_{\overline{RESET}H}$	$I_{\overline{RESET}}$ = 0, internal 10kΩ pull-up resistor to OUT2	V_{OUT2} - 0.5			V
THERMAL SHUTDOWN						
Threshold Temperature				160		°C
I²C-COMPATIBLE SERIAL INTERFACE						
SCL Clock Frequency	f_{SCL}				400	kHz
SCL Low Period	t_{LOW}		1.3			µs
SCL High Period	t_{HIGH}		0.6			µs
Data Set-Up Time	t_{DSU}		100			ns
Data Hold Time	t_{DHOLD}		0		0.9	µs
$\overline{OFF}$, SDA, SCL Input Voltage	V_{IL}				0.6	V
	V_{IH}		1.4			
$\overline{OFF}$, SDA, SCL Input Current	I_{ILH}	0 < V_{ILH} < V_{OUT2}			1	µA
SDA Output Low Voltage		I_{SDA} = 3mA			0.4	V
		I_{SDA} = 6mA			0.6	
$\overline{LBO}$, LBHYST Leakage Current		$V_{\overline{LBO}}$ = V_{LBHYST} = 12V, V_{LBI} = V_{REF} + 15mV	-0.2		0.2	µA

Note 1: Specifications to -40°C are guaranteed by design, not production tested.

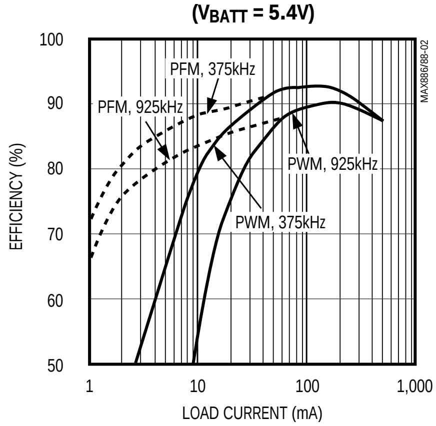
Typical Operating Characteristics

(Circuit of Figure 2, REG0 to REG5 outputs at POR states, V_{OUT0} = 3.75V, V_{OUT4} = 5.25V, V_{OUT1} = V_{OUT2} = V_{OUT3} = V_{OUT5} = 3.3V, T_A = +25°C, unless otherwise noted.)

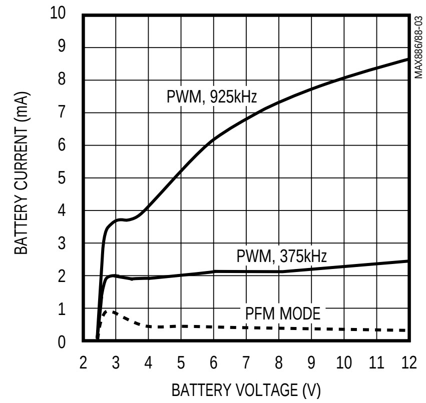
MAX886
REG0 EFFICIENCY vs. LOAD CURRENT
(V_{BATT} = 8.4V)



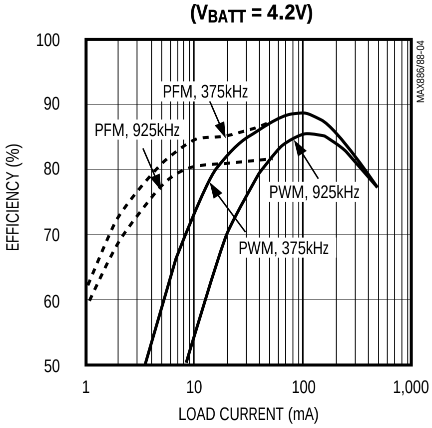
MAX886
REG0 EFFICIENCY vs. LOAD CURRENT
(V_{BATT} = 5.4V)



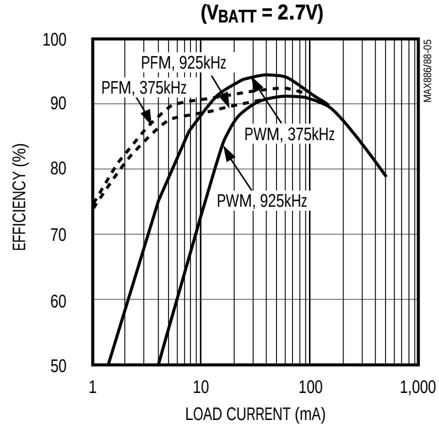
MAX886
NO-LOAD BATTERY CURRENT
vs. BATTERY VOLTAGE



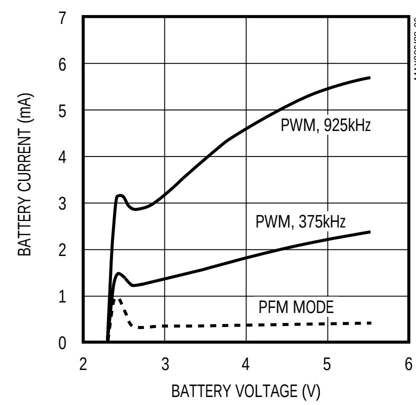
MAX888
REG0 EFFICIENCY vs. LOAD CURRENT
(V_{BATT} = 4.2V)



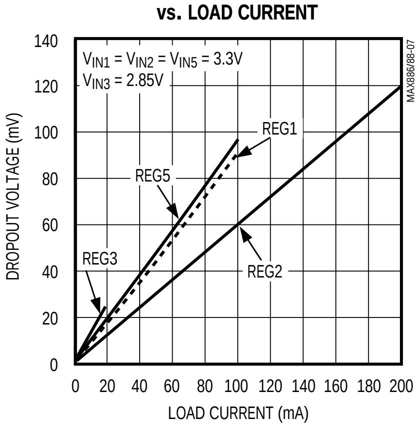
MAX888
REG0 EFFICIENCY vs. LOAD CURRENT
(V_{BATT} = 2.7V)



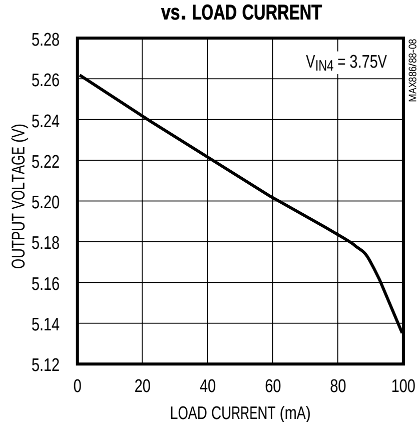
MAX888
NO LOAD BATTERY CURRENT
vs. BATTERY VOLTAGE



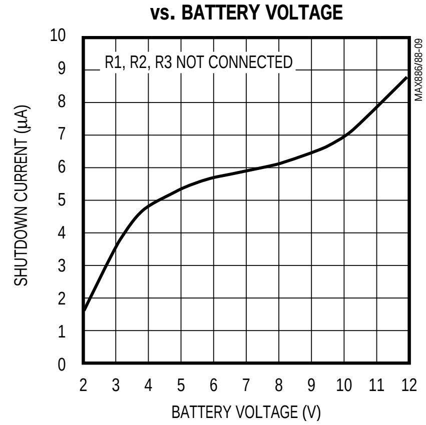
DROPOUT VOLTAGE
vs. LOAD CURRENT



REG4 OUTPUT VOLTAGE
vs. LOAD CURRENT



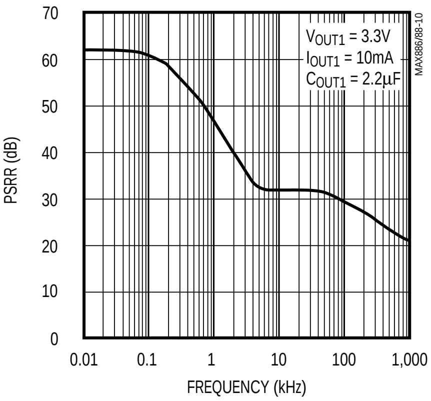
SHUTDOWN CURRENT
vs. BATTERY VOLTAGE



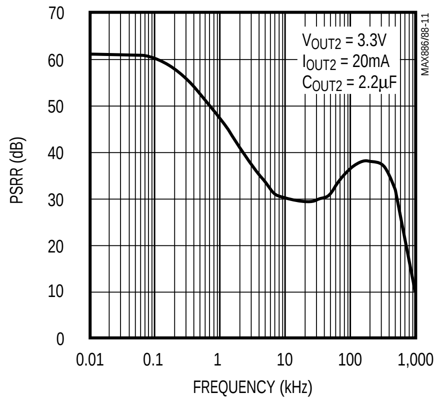
Typical Operating Characteristics (continued)

(Circuit of Figure 2, REG0 to REG5 outputs at POR states, V_{OUT0} = 3.75V, V_{OUT4} = 5.25V, V_{OUT1} = V_{OUT2} = V_{OUT3} = V_{OUT5} = 3.3V, T_A = +25°C, unless otherwise noted.)

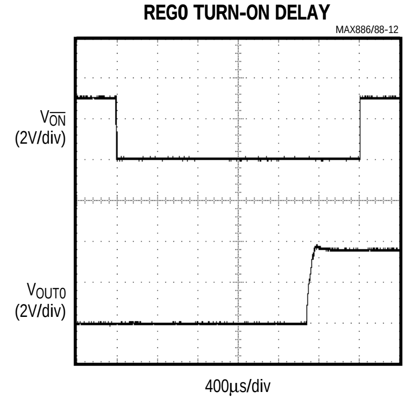
REG1 POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



REG2 POWER-SUPPLY REJECTION RATIO vs. FREQUENCY

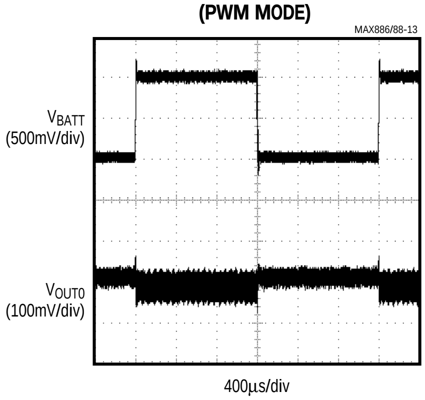


REG0 TURN-ON DELAY



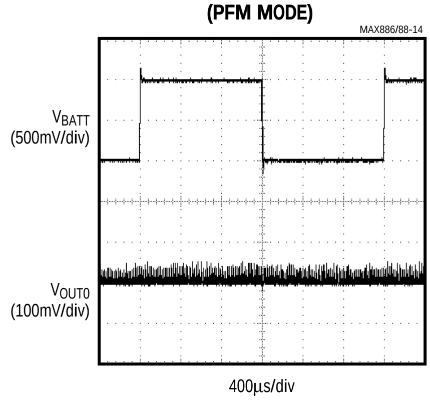
I_{OUT0} = 20mA

REG0 LINE-TRANSIENT RESPONSE (PWM MODE)



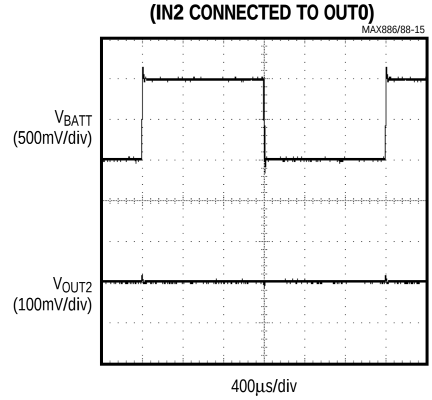
V_{BATT} = 7V TO 8V, I_{OUT0} = 500mA, V_{OUT0} = 3.75V, AC-COUPLED

REG0 LINE-TRANSIENT RESPONSE (PFM MODE)



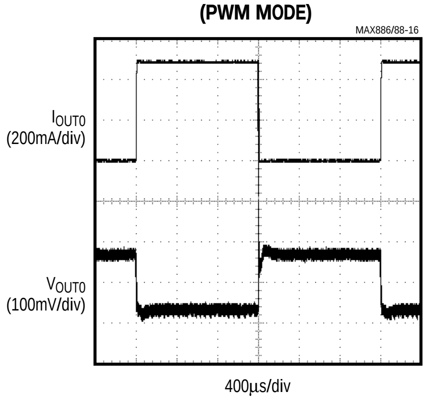
V_{BATT} = 7V TO 8V, I_{OUT0} = 5mA, V_{OUT0} = 3.75V, AC-COUPLED

REG2 LINE-TRANSIENT RESPONSE (IN2 CONNECTED TO OUT0)



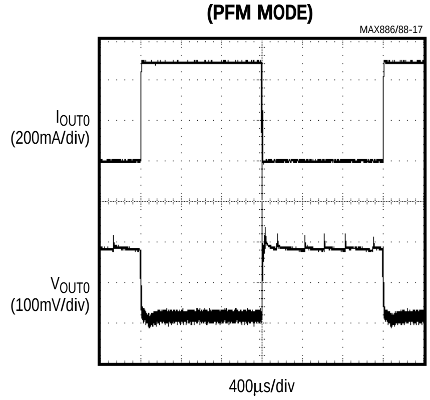
V_{BATT} = 7V TO 8V, I_{OUT2} = 5mA, V_{OUT2} = 3.3V, AC-COUPLED

REG0 LOAD-TRANSIENT RESPONSE (PWM MODE)



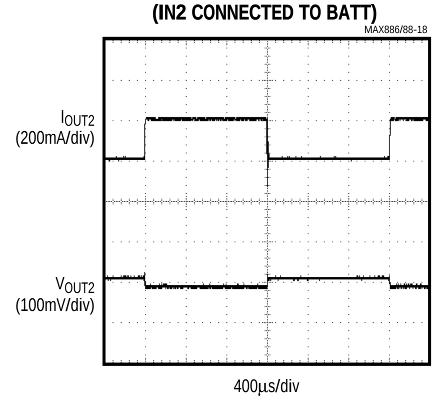
V_{BATT} = 5.4V, I_{OUT0} = 0 TO 500mA, V_{OUT0} = 3.75V, AC-COUPLED

REG0 LOAD-TRANSIENT RESPONSE (PFM MODE)



V_{BATT} = 5.4V, I_{OUT0} = 0 TO 500mA, V_{OUT0} = 3.75V, AC-COUPLED

REG2 LOAD-TRANSIENT RESPONSE (IN2 CONNECTED TO BATT)



V_{BATT} = V_{IN2} = 5.4V, I_{OUT2} = 0 TO 200mA, V_{OUT2} = 3.3V, AC-COUPLED

Wireless and Satellite Handset Power-Management ICs

Pin Description

PIN	NAME	FUNCTION
1	LX	Inductor Input. Drain of the internal p-channel MOSFET.
2	PGND	Power Ground
3	OUT0	Switching Regulator 0 Output. Bypass with a 10µF, low-ESR capacitor to PGND. Up to 500mA is available from OUT0.
4	CVL	Low-Side Drive Bypass. Bypass with a 1µF capacitor to GND.
5	REF	Reference Output. Bypass with a 0.22µF capacitor to GND. REF can source up to 100µA.
6	GND	Ground
7	BATT	Supply Voltage Input. Bypass with a 0.1µF and a 10µF capacitor to PGND as close to BATT as possible.
8	OUT4	Charge-Pump Regulator 4 Output. Bypass with a 10µF, low-ESR capacitor to DGND.
9	C+	Charge-Pump Capacitor Positive Connection
10	IN4	Regulator 4 Power-Supply Input
11	C-	Charge-Pump Capacitor Negative Connection
12	DGND	Digital Ground
13	LBI	Low-Battery Detector Input. $\overline{LBO}$ goes low when V_{LBI} drops below V_{REF}. Connect LBI to the center of a resistor voltage divider between BATT and GND.
14	LBHYS	Low-Battery Detector Hysteresis Control. An open-drain output to set the hysteresis of the Low-Battery Detector Comparator.
15	$\overline{LBO}$	Low-Battery Output. Open-drain output of the Low-Battery Detector Comparator. $\overline{LBO}$ is high impedance when device is shutdown or $V_{LBI} > V_{REF}$. $V_{\overline{LBO}}$ is low when $V_{LBI} < V_{REF}$. Typically, connect a 200kΩ pull-up resistor between $\overline{LBO}$ and OUT2.
16	$\overline{RESET}$	Reset Output. $\overline{RESET}$ remains low during initial power-up for 75ms after OUT2 is ready. $\overline{RESET}$ has an internal 10kΩ pull-up resistor connected to OUT2. $\overline{RESET}$ is valid for V_{BATT} down to 1V.
17	IN2	Linear Regulator 2 Power-Supply Input
18	OUT2	Linear Regulator 2 Output. Bypass with a 2.2µF, low-ESR capacitor to GND. Up to 200mA is available from OUT2. The reset circuit monitors this voltage.
19	OUT3	Linear Regulator 3 Output. Bypass with a 1µF, low-ESR capacitor to GND. Up to 20mA is available from OUT3.
20	IN3	Regulator 3 Power-Supply Input
21	IN5	Regulator 5 Power-Supply Input
22	OUT5	Linear Regulator 5 Output. Bypass with a 1µF, low-ESR capacitor to GND. Up to 100mA is available from OUT5.
23	IN1	Regulator 1 Power-Supply Input

Pin Description (continued)

PIN	NAME	FUNCTION
24	OUT1	Linear Regulator 1 Output. Bypass with a 2.2µF, low-ESR capacitor to GND. Up to 100mA is available from OUT1.
25	$\overline{\text{OFF}}$	Power-Off Input. Drive $\overline{\text{OFF}}$ high before the start-up timer has expired in order to keep the IC powered on. Drive $\overline{\text{OFF}}$ low to shut down the IC. $\overline{\text{OFF}}$ has an internal 100kΩ pull-down resistor to GND.
26	$\overline{\text{ON}}$	Power-On Input. Pulse the $\overline{\text{ON}}$ pin low to turn on the IC. $\overline{\text{ON}}$ has an internal 16µA pull-up.
27	ONSTAT	$\overline{\text{ON}}$ Status Output. Push/pull logic output indicating the state of the $\overline{\text{ON}}$ input. The logic state of this pin follows the logic state of the $\overline{\text{ON}}$ pin. The logic high output voltage is the output voltage of OUT2.
28	SDA	Serial Interface Data Input
29	SCL	Serial Interface Clock Input
30	SYNC	Sync Input. Drive SYNC with a logic-level square wave to synchronize the internal oscillator. The capture range for external clock is ±20% of the selected internal oscillator frequency. Drive SYNC low for more than 10µs to force low-power PFM mode (standby mode). Drive SYNC high to force PWM mode.
31	CVH	High-Side Drive Bypass Input. Bypass CVH with a 0.1µF capacitor connected to IN0.
32	IN0	Regulator 0 Power-Supply Input. Connect to BATT. Source of the internal p-channel MOSFET.

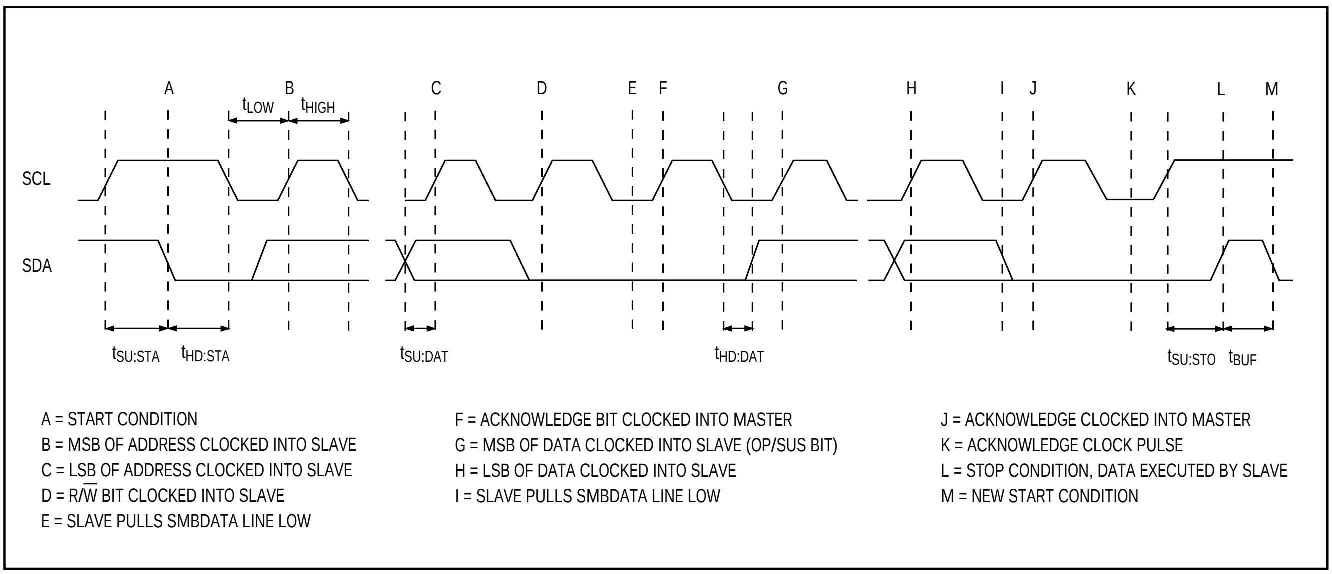


Figure 1. I²C-Compatible Serial-Interface Timing Diagram

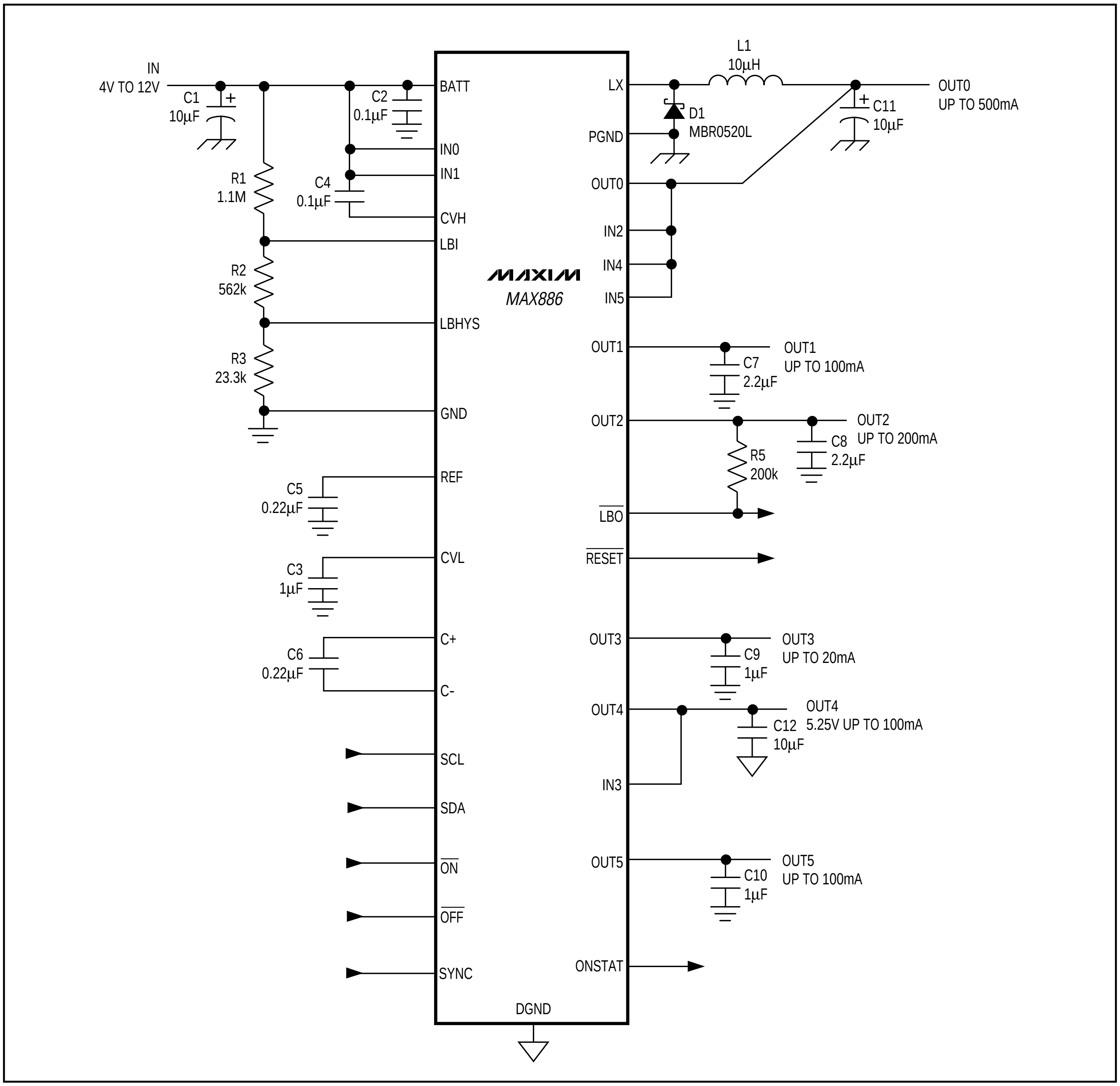


Figure 2a. Typical 2 Li+ or 5 to 6 Ni-Cell Application Circuit (MAX886)

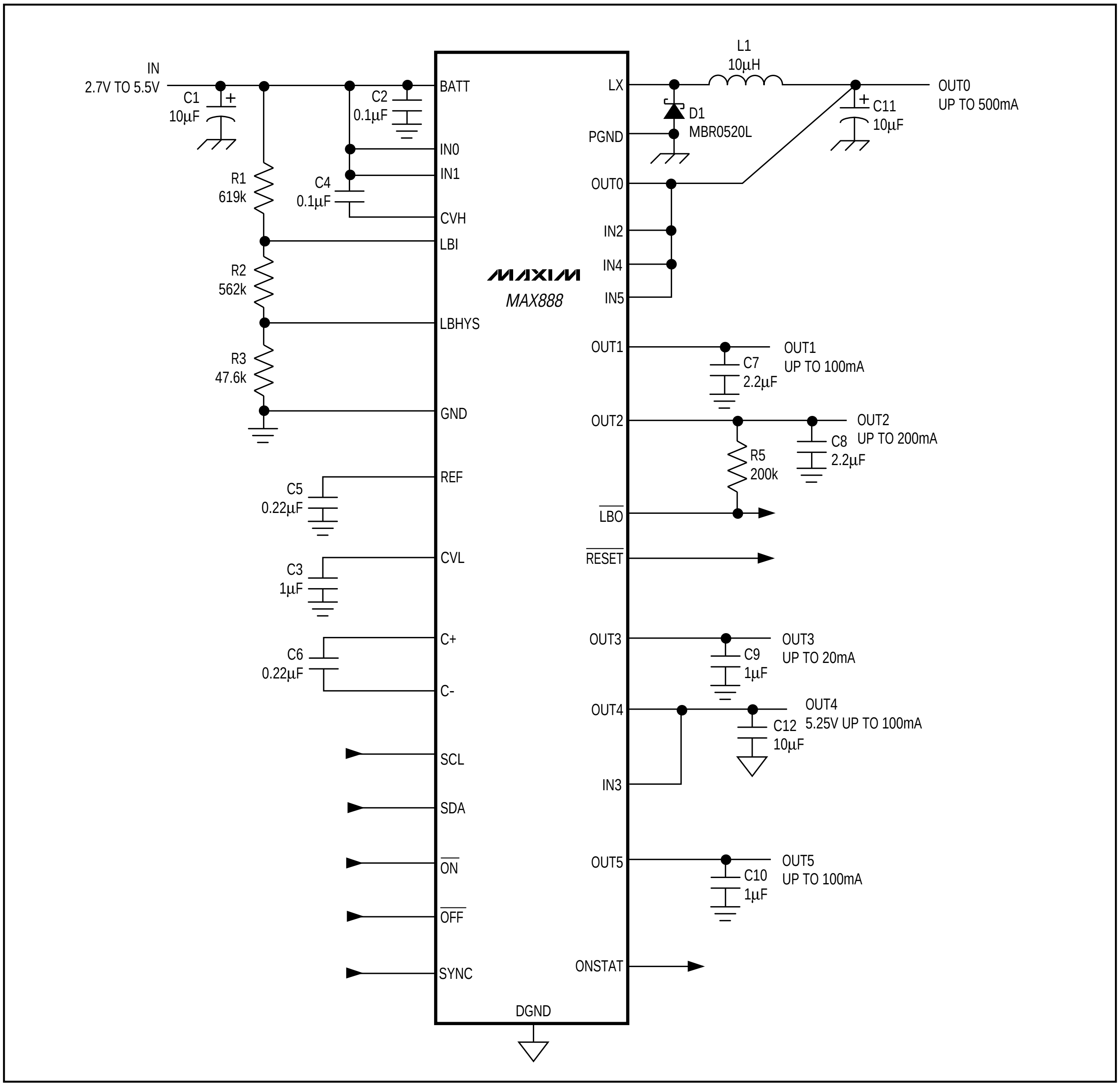


Figure 2b. Typical 1 Li+ or 3 to 4 Ni-Cell Application Circuit (MAX888)

Detailed Description

The MAX886/MAX888 contain one high-efficiency, step-down DC-DC converter, four low-dropout linear regulators, and one regulated charge pump. The output voltages of the switching regulator and the linear regulators are software-programmable through the serial interface. The regulated charge-pump output is factory set at 5.25V. The devices also include reset and start-up timers and a low-battery detect comparator (Figure 3).

500mA DC-DC Buck Regulator 0

Regulator 0 is a low-noise, step-down, synchronous DC-DC converter that can source a minimum of 500mA. High operating frequency (up to 925kHz) minimizes output voltage ripple and reduces the size and cost of external components. Guaranteed 100% duty-cycle operation provides the lowest possible dropout voltage, extending the useful life of the battery supply.

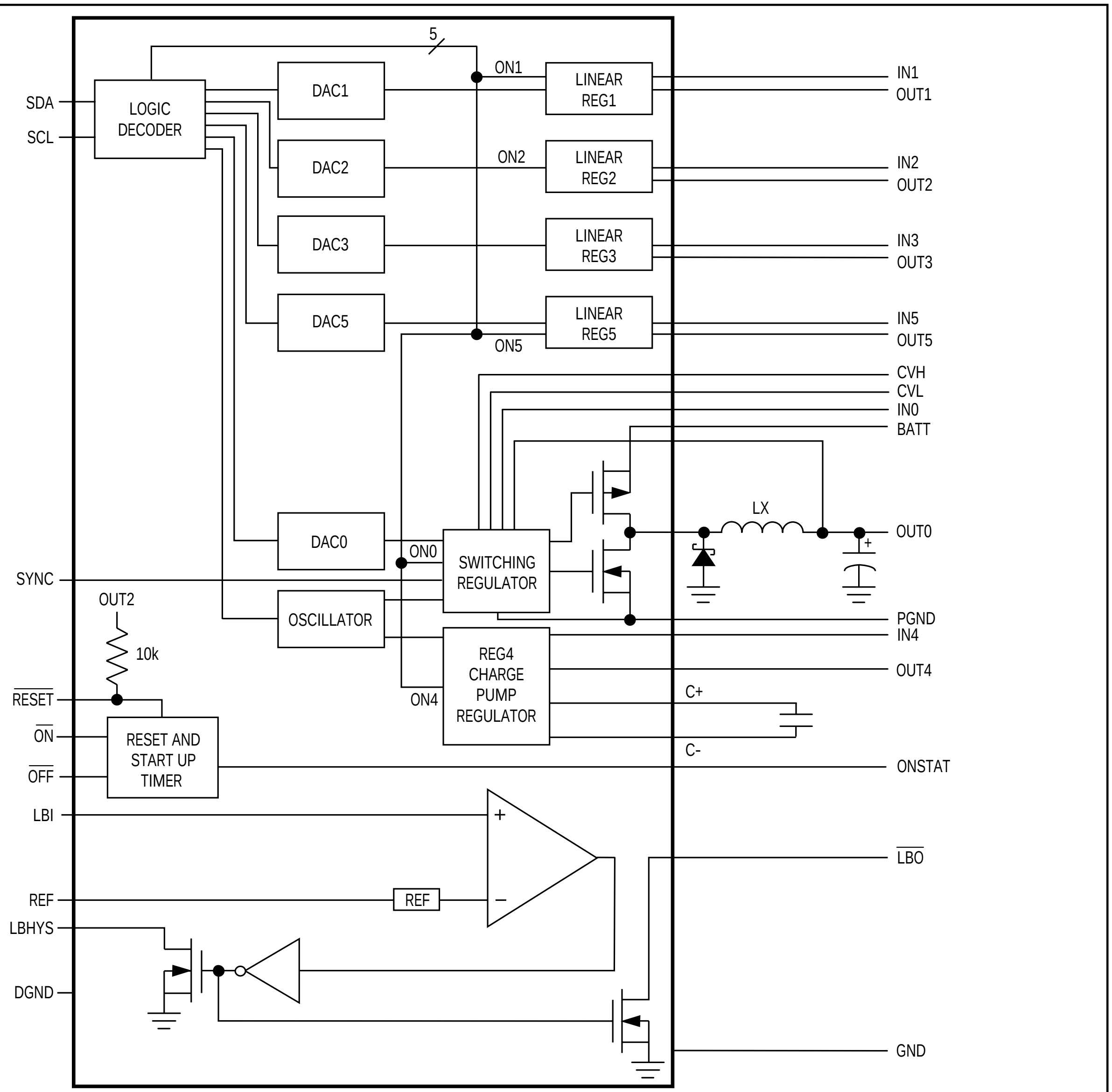


Figure 3. Functional Diagram

The serial interface programs V_{OUT0} from 2.625V to 3.75V in 75mV steps for the MAX886 (Tables 1 and 2), or from 1.527V to 3.027V in 100mV steps for the MAX888 (Tables 1 and 3).

Regulator 0 operates in one of four preset frequencies, from 375kHz to 925kHz, programmable through the serial interface (Table 4).

For the device to power up properly, V_{IN0} must be high enough for REG0 to get into regulation. For the MAX886, Regulator 0's default voltage is 3.75V. Since the rest of the regulators do not power up until Regulator 0 is ready, V_{IN0} must be greater than approximately 4V for the device to power up properly. The Regulator 0 default voltage for the MAX888 is 2.027V, so the minimum V_{IN0} required to start up is limited by the minimum operating voltage range (2.7V). After power-up, the device operates until V_{BATT} drops below $V_{\overline{UVLOF}}$ (undervoltage lockout falling threshold).

Sync Mode

The SYNC input allows the MAX886/MAX888 to synchronize with an external clock applied to SYNC, ensuring that switching harmonics are kept away from sensitive IF bands. The SYNC detector triggers on SYNC's falling edge.

PWM Mode

Regulator 0 is in PWM mode when SYNC is connected to CVL or driven to a logic-high voltage. Two internal switches operate at a preset frequency even when there is no load. The P-channel MOSFET turns on to charge the inductor until the error comparator or current-limit comparator turns it off. The N-channel MOSFET then turns on to discharge the inductor. To prevent the output from soaring with no load in PWM mode, the N-channel switch stays on long enough to allow the inductor current to go negative. Once the N-channel switch turns off, the voltage at LX rises (rings) until the next cycle when the P-channel switch turns on again. As the load increases and the inductor enters continuous conduction, ringing is no longer present and the LX waveform looks like a square wave whose duty cycle depends on the input and output voltages. As the input voltage approaches the same level as the output voltage, the P-channel switch stays on 100% of the time, providing the lowest possible dropout.

PFM Mode

Regulator 0 operates in PFM mode when SYNC is driven to a logic low voltage or connected to GND. When V_{OUT0} drops below the regulation threshold, the P-channel switch turns on to charge the inductor until the error comparator or current-limit comparator turns it off. At light loads, the N-channel then turns on to discharge the inductor until the current in the inductor reaches zero. In PFM mode, the inductor current does not go negative to discharge the output. At no-load there is a long period between pulses of inductor current. As the load current increases, the period between pulses becomes shorter until the pulses become continuous. At load currents above this point, Regulator 0 automatically switches to PWM mode, and the V_{LX} waveform looks like a square wave whose duty cycle depends on the input and output voltages. As the input voltage approaches the same level as the output voltage, the P-channel switch stays on 100% of the time, providing the lowest possible dropout. It is typically more efficient to use the PFM mode when the load current is less than 100mA.

100mA LDO Regulator 1

Regulator 1, a low-dropout linear regulator, sources a minimum of 100mA and operates from voltages at IN1 of up to 12V. The serial interface programs V_{OUT1} from 2.7V to 4.95V in 75mV steps for the MAX886 (Tables 1 and 2), or from 1.25V to 3.50V in 150mV steps for the MAX888 (Tables 1 and 3). IN1 may be powered from the battery, OUT0, or any other voltage source.

200mA LDO Regulator 2

Regulator 2, a low-dropout linear regulator, sources a minimum of 200mA. The serial interface programs V_{OUT2} from 2.175V to 3.3V in 75mV steps for the MAX886 (Tables 1 and 2), or from 1.527V to 3.027V in 100mV steps for the MAX888 (Tables 1 and 3). IN2 may be powered from the battery, OUT0, or any other voltage source less than 5.5V.

20mA LDO Regulator 3

Regulator 3, a low-dropout linear regulator, sources a minimum of 20mA. The serial interface programs V_{OUT3} to one of four different output voltages: 0V, 2.85V, 4.65V, or V_{OUT2} (Tables 1 and 5). Although this is a general-purpose output, OUT3 is intended for the SIM supply. IN3 may be powered from OUT4 or from any regulated 5V supply.

When programmed to 0V or V_{OUT2}, OUT3 is either actively discharged to GND (for 0V mode) or connected to OUT2 (for V_{OUT2}), and Regulator 3 is disabled to conserve power.

100mA Charge-Pump Regulator 4

Regulator 4, a regulated charge pump, generates 5.25V and delivers up to 100mA. An oscillator synchronized to the PWM clock regulates OUT4 to minimize noise. It operates at one-half the frequency of the PWM oscillator to ensure 50% duty-cycle outputs. IN4 may be powered from the battery, OUT0, or any other voltage source less than 5.5V.

To save space and cost, use a small ceramic flying capacitor. See Table 6 for recommended flying capacitor values.

Wireless and Satellite Handset Power-Management ICs

100mA LDO Regulator 5

Regulator 5, a low-dropout linear regulator, can source a minimum of 100mA. The output voltage is programmable from 2.175V to 3.3V in 75mV steps for the MAX886 (Tables 1 and 2), or 1.25V to 3.50V in 150mV steps for the MAX888 (Tables 1 and 3). IN5 may be powered from the battery, OUT0, or any other voltage source less than 5.5V.

Control Data Byte

The control byte is eight bits long (four address bits, four data bits). Each regulator has a DAC that sets the output regulation voltage. Control codes are summarized in Table 1.

Table 1. Control Data Byte

FUNCTION	ADDRESS				DATA			
	A3 MSB	A2	A1	A0	D3	D2	D1	D0 LSB
OUT0 Output Voltage	0	0	0	0	DAC0			
OUT1 Output Voltage	0	0	0	1	DAC1			
OUT2 Output Voltage	0	0	1	0	DAC2			
OUT3 Output Voltage, f_{OSC}	0	0	1	1	DAC3		f_{OSC}	
OUT5 Output Voltage	0	1	0	0	DAC5			
OUT1, 2, 4, 5 On/Off Control	0	1	0	1	ON5	ON4	ON2	ON1
OUT0 On/Off Control	0	1	1	0	X	X	X	ON0
Not Available	0	1	1	1	X	X	X	X
Not Available	1	X	X	X	X	X	X	X

Table 2. MAX886 Output Voltage Settings

REGULATOR OUTPUT VOLTAGE (V)				DACX DATA			
OUT5	OUT2	OUT1	OUT0	D3	D2	D1	D0
2.175	2.175	2.70	2.625	0	0	0	0
2.250	2.250	2.85	2.700	0	0	0	1
2.325	2.325	3.00	2.775	0	0	1	0
2.400	2.400	3.15	2.850	0	0	1	1
2.475	2.475	**3.30**	2.925	0	1	0	0
2.550	2.550	3.45	3.000	0	1	0	1
2.625	2.625	3.60	3.075	0	1	1	0
2.700	2.700	3.75	3.150	0	1	1	1
2.775	2.775	3.90	3.225	1	0	0	0
2.850	2.850	4.05	3.300	1	0	0	1
2.925	2.925	4.20	3.375	1	0	1	0
3.000	3.000	4.35	3.450	1	0	1	1
3.075	3.075	4.50	3.525	1	1	0	0
3.150	3.150	4.65	3.600	1	1	0	1
3.225	3.225	4.80	3.675	1	1	1	0
3.300	**3.300**	4.95	**3.750**	1	1	1	1

Note: *The output voltage of each regulator can be set independently. The POR states are in boldface.*

Table 3. MAX888 Output Voltage Settings

REGULATOR OUTPUT VOLTAGE (V)				DACX DATA			
OUT5	**OUT2**	**OUT1**	**OUT0**	**D3**	**D2**	**D1**	**D0**
1.25	1.527	1.25	1.527	0	0	0	0
1.40	1.627	1.40	1.627	0	0	0	1
1.55	1.727	**1.55**	1.727	0	0	1	0
1.70	1.827	1.70	1.827	0	0	1	1
1.85	1.927	1.85	1.927	0	1	0	0
2.00	2.027	2.00	**2.027**	0	1	0	1
2.15	2.127	2.15	2.127	0	1	1	0
2.30	2.227	2.30	2.227	0	1	1	1
2.45	2.327	2.45	2.327	1	0	0	0
2.60	2.427	2.60	2.427	1	0	0	1
2.75	2.527	2.75	2.527	1	0	1	0
2.90	2.627	2.90	2.627	1	0	1	1
3.05	2.727	3.05	2.727	1	1	0	0
3.20	**2.827**	3.20	2.827	1	1	0	1
3.35	2.927	3.35	2.927	1	1	1	0
3.50	3.027	3.50	3.027	1	1	1	1

Note: *The output voltage of each regulator can be set independently. The POR states are in boldface.*

Table 4. Oscillator Frequency Setting

ADDRESS 03h DATA f_{OSC} (kHz)	D3	D2	D1	D0
375	X	X	0	0
535	X	X	0	1
670	X	X	1	0
925	X	X	**1**	**1**

Note: *The POR states are in boldface.*

Table 5. OUT3 Output Voltage Setting

ADDRESS 03h DATA	D3	D2	D1	D0
0V (REG3 Off)	0	0	X	X
2.85V	0	1	X	X
4.65V	1	0	X	X
VOUT2 (REG3 Off)	**1**	**1**	X	X

Note: *The POR states are in boldface.*

Low-Battery Detector

A low-battery comparator detects low-battery conditions. The trip threshold is internally set to V_{REF} (1.25V typ). LBHYS sets the hysteresis with external resistors. $\overline{LBO}$ and LBHYS have open-drain outputs. The externally set low-battery threshold must be higher than the UVLOF threshold (2.45V typical).

Set the threshold and hysteresis by connecting resistors R1 (between BATT and LBI), R2 (between LBI and LBHYS), and R3 (LBHYS and GND) (Figure 2).

After choosing the upper and lower thresholds, calculate the resistor values as follows:

1) Choose a value for R1. Typical values range from 500kΩ to 1.5MΩ.
2) Calculate R2:

$$R2 = \frac{R1}{\left(\frac{V_{THR}}{V_{REF}}\right) - 1}$$

3) Calculate R3:

$$R3 = \frac{R2\left(V_{THF} - V_{REF}\right) - R1 \cdot V_{REF}}{V_{REF} - V_{THF}}$$

For example:

V_{REF} = 1.25V

V_{THF} = falling threshold = 2.52V

V_{HYS} = hysteresis = 0.1V

V_{THR} = rising threshold = V_{THF} + V_{HYS} = 2.62V

R1 = 619kΩ (1%)

R2 = 562kΩ (1%)

R3 = 47.6kΩ (1%)

Power-On Sequence (Including RESET and Start-Up Timers)

Drive ON low to begin the power-up sequence. To reduce overall system cost and complexity, the MAX886/MAX888 incorporate RESET and start-up timers with the power-on sequence.

The MAX886/MAX888 turn on the reference when ON goes low. Once the reference is fully powered up, if the input voltage exceeds the internal undervoltage-lockout threshold (UVLOR), Regulator 0 turns on. Once OUT0 is in regulation, OUT2 and OUT4 turn on. Once OUT2 is in regulation, OUT1 and OUT5 turn on and the 75ms reset timer begins. RESET remains low from the time OUT2 is valid until the reset timer times out. After the reset period expires, a 50ms start-up timer begins. The MAX886/MAX888 shut down if the external logic or controller fails to drive OFF high before the start-up timer expires. Drive OFF high to continue operation. Driving OFF low turns off the IC.

There is no required sequence to power off any regulator after the device has turned on. Regulators can be powered off selectively by sending the correct code through the serial interface (Table 1).

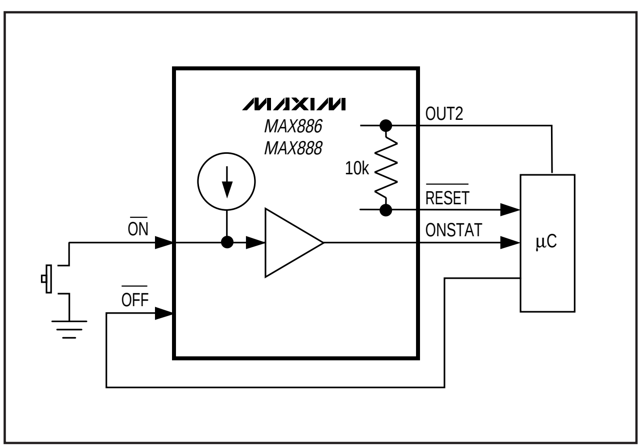


Figure 4. One-Button On/Off Control with ONSTAT

ONSTAT Output

ONSTAT is a logic output that follows ON. Connect ONSTAT to the external logic or controller to sense when the ON pin has been brought low to request shutdown. This allows easy implementation of a one-button on/off control scheme (Figure 4).

Thermal Overload Protection

An internal thermal sensor shuts the MAX886/MAX888 down when the maximum temperature limit is exceeded (160°C typical).

I²C-Compatible Serial Interface

Use an I^2C-compatible serial interface to turn the MAX886/MAX888 on and off, as well as control each regulator's output voltage and program the DC-DC converter and charge pump's oscillator frequency. Use standard I^2C-compatible receive-byte commands to program the IC. This part is always a slave to the bus master. **The chip address is 1001 111.**

POR State

The power-on reset state of all the DAC and frequency registers is 0Fh, except for DAC1 which is 04h. The power-on reset state of the ONX bits is 1 (Table 1). The power-on voltage for each regulator is shown in bold in Tables 2, 3, and 5.

Applications Information

Inductor Selection

The essential parameters for inductor selection are inductance and current rating. The MAX886/MAX888 operate with a wide range of inductance values. In many applications, values between 10µH and 68µH take best advantage of the controller's high switching frequency.

Calculate the minimum inductance value using the simplified equation:

$$L_{(MIN)} = \frac{4\left(V_{BATT(MAX)} - V_{OUT0}\right)}{\left(I_{PEAK} \cdot f_{OSC} \cdot V_{BATT} / V_{OUT0}\right)}$$

where I_{PEAK} is the peak inductor current (0.9A) and f_{OSC} is the switching frequency.

For example, for a 6V battery voltage, a desired V_{OUT0} is 3.3V, the oscillator frequency is 375kHz, and 15µH is the minimum inductance required.

Diode Selection

The MAX886/MAX888's high switching frequency demands a high-speed rectifier. Schottky diodes, such as the 1N5817–1N5822 family or surface-mount MBR0520L series are recommended. Ultra-high-speed rectifiers with reverse recovery times around 50ns or faster, such as the MUR series, are acceptable. Ensure that the diode's peak current rating exceeds the peak current (1A), and that its breakdown voltage exceeds V_{BATT}. Schottky diodes are preferred for heavy loads due to their low forward voltage, especially in low-voltage applications.

Capacitor Selection

Choose filter capacitors to service input and output peak currents with acceptable voltage ripple. The capacitor's equivalent series resistance (ESR) is a major contributor to ripple; therefore, low-ESR capacitors are recommended for OUT1–OUT5. A tantalum capacitor is recommended for OUT0 (refer to Figures 2a and 2b, and Table 6).

The input filter capacitor reduces peak currents drawn from the power source, and reduces noise and voltage ripple on the input, which are caused by the circuit's switching action. Since the current from the battery is interrupted each time the PMOS switch opens, pay special attention to the ripple current rating of the input filter capacitor and use a low-ESR capacitor. Choose input capacitors with working voltage ratings higher than the maximum input voltage. Input capacitors prevent spikes and ringing on the power source from obscuring the current-feedback signal and causing jitter.

Bypass REF with 0.22µF to GND. The capacitor should be placed within 0.2 inches of the IC, next to REF, with a direct trace to GND.

Table 6. OUT0 and OUT4 Regulator Component Recommendations

f_{OSC} (kHz)	C11 (µF)	L1 (µH)	C6 (µF)	C12 (µF)
925	10	10	0.22	10
670	15	15	0.33	15
535	22	22	0.47	22
375	33	33	1	33

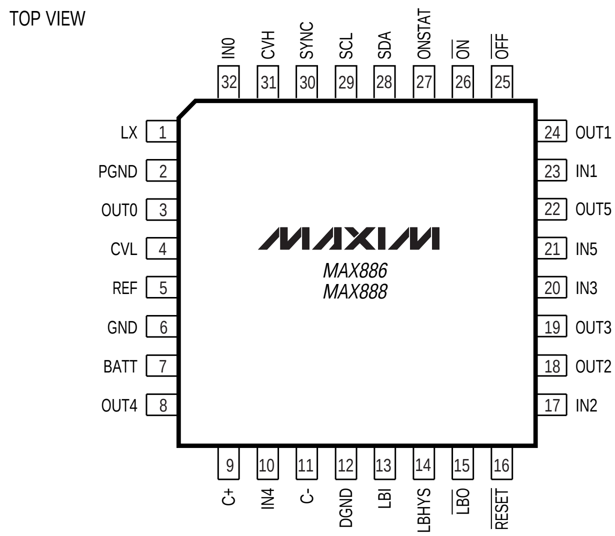
Table 7. Component Suppliers

COMPANY	PHONE	FAX
AVX	803-946-0690	803-626-3123
Coilcraft	847-639-6400	847-639-1469
Coiltronics	516-241-7876	516-241-9339
Dale	605-668-4131	605-665-1627
Internal Rectifier	310-322-3331	310-322-3332
Motorola	602-303-5454	602-994-6430
Sanyo	619-661-6835	619-661-1055
Sprague	408-988-8000	408-970-3950
Sumida	847-956-0666	847-956-0702

Layout Considerations

High-frequency switching regulators are sensitive to PC board layout. Poor layout introduces switching noise into the current and voltage-feedback signals, resulting in jitter, instability, or degraded performance. Place the anode of the Schottky diode and the ground pins of the input and output capacitors close together, and route them to a common "star-ground" point. Place components and route ground paths so as to prevent high currents from causing large voltage gradients between the ground pin of the output filter capacitor, the controller IC, and the reference bypass capacitor. Keep the extra copper on the component and solder sides of the PC board rather than etching it away, and connect it to ground for use as a pseudo-ground plane. Refer to the MAX886/MAX888 evaluation kit for a two-layer PC board layout example.

Pin Configuration

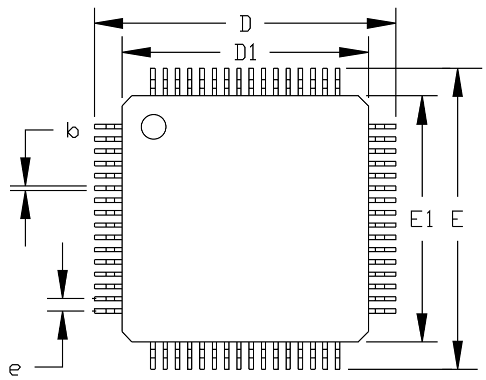


Chip Information

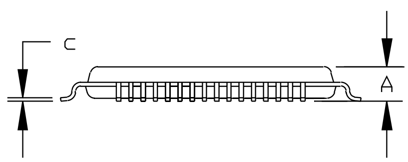
TRANSISTOR COUNT: 2042

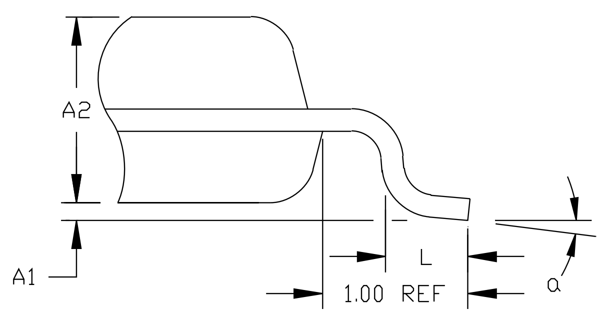
Package Information

TQFPPO.EPS



	JEDEC VARIATION					
	BC		BE		BJ	
	32 LEAD		48 LEAD		64 LEAD	
	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
A	---	1.60	---	1.60	---	1.60
A_1	0.05	0.15	0.05	0.15	0.05	0.15
A_2	1.35	1.45	1.35	1.45	1.35	1.45
D	8.90	9.10	8.90	9.10	12.00 BSC.	
D_1	7.00 BSC.		7.00 BSC.		10.00 BSC.	
E	8.90	9.10	8.90	9.10	12.00 BSC.	
E_1	7.00 BSC.		7.00 BSC.		10.00 BSC.	
e	0.8 BSC.		0.5 BSC.		0.5 BSC.	
L	0.45	0.75	0.45	0.75	0.45	0.75
b	0.30	0.45	0.17	0.27	0.17	0.27
c	0.09	0.20	0.09	0.20	0.09	0.20
α	0°	7°	0°	7°	0°	7°





NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATIONS BC, BE AND BJ.

MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TQFP

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0054	C	1/1

NOTES