

### Logic Diagram

**DESCRIPTION:**

- Maxwell Technologies' 33LV408 high-density 4 Megabit SRAM microcircuit features a greater than 100 krad (Si) total dose tolerance, depending upon space mission. Using Maxwell's radiation-hardened RAD-PAK® packaging technology, the 33LV408 realizes a high density, high performance, and low power consumption. Its fully static design eliminates the need for external clocks, while the CMOS circuitry reduces power consumption and provides higher reliability. The 33LV408 is equipped with eight common input/output lines, chip select and output enable, allowing for greater system flexibility and eliminating bus contention. The 33LV408 features the same advanced 512K x 8-bit SRAM, high-speed, and low-power demand as the commercial counterpart.

Maxwell Technologies' patented RAD-PAK® packaging technology incorporates radiation shielding in the microcircuit package. It eliminates the need for box shielding while providing the required radiation shielding for a lifetime in orbit or space mission. In a GEO orbit, RAD-PAK® provides greater than 100 krad (Si) radiation dose tolerance. This product is available with screening up to Class S.

TABLE 1. PINOUT DESCRIPTION

PIN	SYMBOL	DESCRIPTION
12-5, 27, 26, 23, 25, 4, 28, 3, 31, 2, 30, 1	A0-A18	Address Inputs
29	$\overline{WE}$	Write Enable
22	$\overline{CS}$	Chip Select
24	$\overline{OE}$	Output Enable
13-15, 17-21	I/O 1-I/O 8	Data Inputs/Outputs
32	$V_{CC}$	Power
16	$V_{SS}$	Ground

TABLE 2. 33LV408 ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Voltage on $V_{CC}$ supply relative to $V_{SS}$	$V_{CC}$	-0.5	7.0	V
Voltage on any pin relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-0.5	$V_{CC} + 0.5$	V
Power Dissipation	$P_D$	--	1.0	W
Storage Temperature	$T_S$	-65	+150	°C
Operating Temperature	$T_A$	-55	+125	°C

TABLE 3. DELTA LIMITS

PARAMETER	VARIATION
$I_{CC}$	±10% of stated vaule in Table 6
$I_{SB}$	±10% of stated vaule in Table 6
$I_{SB1}$	±10% of stated vaule in Table 6

TABLE 4. 33LV408 RECOMMENDED OPERATING CONDITIONS

(V<sub>CC</sub> = 3.3 ± 10%, T<sub>A</sub> = -55 TO +125 °C, UNLESS OTHERWISE NOTED)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage	V <sub>CC</sub>	3.0	3.6	V
Ground	V <sub>SS</sub>	0	0	V
Input High Voltage <sup>1</sup>	V <sub>IH</sub>	2.2	V <sub>CC</sub> +0.3	V
Input Low Voltage <sup>2</sup>	V <sub>IL</sub>	-0.3	0.8	V
Thermal Impedance	Θ <sub>JC</sub>	--	1.21	°C/W
Weight			12	Grams

1. V<sub>IH</sub> (max) = V<sub>CC</sub> + 2.0V ac (pulse width ≤ 10 ns) for I ≤ 20 mA2. V<sub>IL</sub> (min) = -2.0V ac (pulse width ≤ 10 ns) for I ≤ 20 mA

TABLE 5. 33LV408 CAPACITANCE

(f = 1.0 MHz, V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNITS
Input Capacitance <sup>1</sup> CS1 - CS4, OE, WE I/O0-7, I/O8-15, I/O16-23, I/O24-31	C <sub>IN</sub>	V <sub>IN</sub> = 0 V	7 28 7	pF
Input / Output Capacitance <sup>1</sup>	C <sub>OUT</sub>	V <sub>I/O</sub> = 0 V	8	pF

1. Guaranteed by design.

TABLE 6. 33LV408 DC ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = 3.3V ± 10%, T<sub>A</sub> = -55 TO +125 °C, UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	CONDITION	SUBGROUPS	MIN	MAX	UNIT
Input Leakage Current	I <sub>LI</sub>	V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub>	1, 2, 3	-2	2	μA
Output Leakage Current	I <sub>LO</sub>	CS=V <sub>IH</sub> or OE=V <sub>IH</sub> or WE=V <sub>IL</sub> , V <sub>OUT</sub> =V <sub>SS</sub> to V <sub>CC</sub>	1, 2, 3	-2	2	μA
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8mA	1, 2, 3	--	0.4	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4mA	1, 2, 3	2.4	--	V
Operating Current -20 -25 -30	I <sub>CC</sub>	Min cycle, 100% Duty, CS=V <sub>IL</sub> , I <sub>OUT</sub> =0mA, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	1, 2, 3	-- -- --	150 140 130	mA
Standby Power Supply Current	I <sub>SB</sub>	CS = V <sub>IH</sub> , Min Cycle	1, 2, 3	--	60	mA

TABLE 6. 33LV408 DC ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = 3.3V ± 10%, T<sub>A</sub> = -55 TO +125 °C, UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	CONDITION	SUBGROUPS	MIN	MAX	UNIT
Standby Power Supply Current - CMOS	I <sub>SB1</sub>	$\overline{CS} \geq V_{CC} - 0.2V$ ; V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> < 0.2V	1, 2, 3	--	10	mA
Input Capacitance <sup>1</sup>	C <sub>IN</sub>	V <sub>IN</sub> = 0V, f = 1MHz, T <sub>A</sub> = 25 °C	1, 2, 3	--	7	pF
Output Capacitance <sup>1</sup>	C <sub>I/O</sub>	V <sub>I/O</sub> = 0V	1, 2, 3	--	8	pF

1. Guaranteed by design.

TABLE 7. 33LV408 AC OPERATING CONDITIONS AND CHARACTERISTICS

(V<sub>CC</sub> = 3.3 ± 10%, T<sub>A</sub> = -55 TO +125 °C, UNLESS OTHERWISE NOTED)

PARAMETER	MIN	TYP	MAX	UNITS
Input Pulse Level	0.0	--	3.0	V
Output Timing Measurement Reference Level	--	--	1.5	V
Input Rise/Fall Time	--	--	3.0	ns
Input Timing Measurement Reference Level	--	--	1.5	V

TABLE 8. 33LV408 AC CHARACTERISTICS FOR READ CYCLE

(V<sub>CC</sub> = 3.3V ± 10%, T<sub>A</sub> = -55 TO +125 °C, UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	SUBGROUPS	MIN	TYP	MAX	UNIT
Read Cycle Time	t <sub>RC</sub>	9, 10, 11				ns
-20			20	--	--	
-25			25	--	--	
-30			30	--	--	
Address Access Time	t <sub>AA</sub>	9, 10, 11				ns
-20			--	--	20	
-25			--	--	25	
-30			--	--	30	
Chip Select Access Time	t <sub>CO</sub>	9, 10, 11				ns
-20			--	--	20	
-25			--	--	25	
-30			--	--	30	
Output Enable to Output Valid	t <sub>OE</sub>	9, 10, 11				ns
-20			--	--	10	
-25			--	--	12	
-30			--	--	14	
Chip Enable to Output in Low-Z	t <sub>LZ</sub>	9, 10, 11				ns
-20			--	3	--	
-25			--	3	--	
-30			--	3	--	

TABLE 8. 33LV408 AC CHARACTERISTICS FOR READ CYCLE

(V<sub>CC</sub> = 3.3V ± 10%, T<sub>A</sub> = -55 TO +125 °C, UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	SUBGROUPS	MIN	TYP	MAX	UNIT
Output Enable to Output in Low-Z -20 -25 -30	t <sub>OLZ</sub>	9, 10, 11	-- -- --	0 0 0	-- -- --	ns
Chip Deselect to Output in High-Z -20 -25 -30	t <sub>HZ</sub>	9, 10, 11	-- -- --	5 6 8	-- -- --	ns
Output Disable to Output in High-Z -20 -25 -30	t <sub>OHZ</sub>	9, 10, 11	-- -- --	5 6 8	-- -- --	ns
Output Hold from Address Change -20 -25 -30	t <sub>OH</sub>	9, 10, 11	3 5 6	-- -- --	-- -- --	ns
Chip Select to Power Up Time -20 -25 -30	t <sub>PU</sub>	9, 10, 11	-- -- --	0 0 0	-- -- --	ns
Chip Select to Power Down Time -20 -25 -30	t <sub>PD</sub>	9, 10, 11	-- -- --	10 15 20	-- -- --	ns

TABLE 9. 33LV408 FUNCTIONAL DESCRIPTION

$\overline{\text{CS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	MODE	I/O PIN	SUPPLY CURRENT
H	X <sup>1</sup>	X <sup>1</sup>	Not Select	High-Z	I <sub>SB</sub> , I <sub>SB1</sub>
L	H	H	Output Disable	High-Z	I <sub>CC</sub>
L	H	L	Read	D <sub>OUT</sub>	I <sub>CC</sub>
L	L	X <sup>1</sup>	Write	D <sub>IN</sub>	I <sub>CC</sub>

1. X = don't care.

TABLE 10. 33LV408 AC CHARACTERISTICS FOR WRITE CYCLE  
 $(V_{CC} = 3.3V \pm 10\%, T_A = -55 \text{ TO } +125^\circ\text{C}, \text{ UNLESS OTHERWISE SPECIFIED})$

PARAMETER	SYMBOL	SUBGROUPS	MIN	TYP	MAX	UNIT
Write Cycle Time -20 -25 -30	$t_{WC}$	9, 10, 11	20 25 30	-- -- --	-- -- --	ns
Chip Select to End of Write -20 -25 -30	$t_{CW}$	9, 10, 11	14 15 17	-- -- --	-- -- --	ns
Address Setup Time -20 -25 -30	$t_{AS}$	9, 10, 11	0 0 0	-- -- --	-- -- --	ns
Address Valid to End of Write -20 -25 -30	$t_{AW}$	9, 10, 11	14 15 17	-- -- --	-- -- --	ns
Write Pulse Width (OE High) -20 -25 -30	$t_{WP}$	9, 10, 11	14 15 17	-- -- --	-- -- --	ns
Write Recovery Time -20 -25 -30	$t_{WR}$	9, 10, 11	0 0 0	-- -- --	-- -- --	ns
Write to Output in High-Z -20 -25 -30	$t_{WHZ}$	9, 10, 11	-- -- --	5 5 6	-- -- --	ns
Write Pulse Width (OE Low) -20 -25 -30	$t_{WP1}$	9, 10, 11	-- -- --	20 25 30	-- -- --	ns
Data to Write Time Overlap -20 -25 -30	$t_{DW}$	9, 10, 11	9 10 11	-- -- --	-- -- --	ns
End Write to Output Low-Z -20 -25 -30	$t_{OW}$	9, 10, 11	-- -- --	6 7 8	-- -- --	ns

TABLE 10. 33LV408 AC CHARACTERISTICS FOR WRITE CYCLE

 $(V_{CC} = 3.3V \pm 10\%, T_A = -55 \text{ TO } +125^\circ\text{C}, \text{ UNLESS OTHERWISE SPECIFIED})$ 

PARAMETER	SYMBOL	SUBGROUPS	MIN	TYP	MAX	UNIT
Data Hold from Write Time	$t_{DH}$	9, 10, 11				ns
-20			0	--	--	
-25			0	--	--	
-30			0	--	--	

FIGURE 1: TIMING WAVEFORM OF READ CYCLE(1)

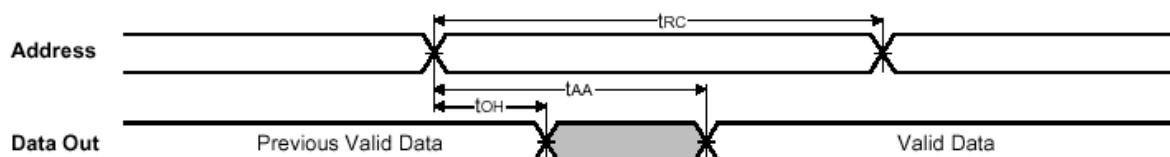
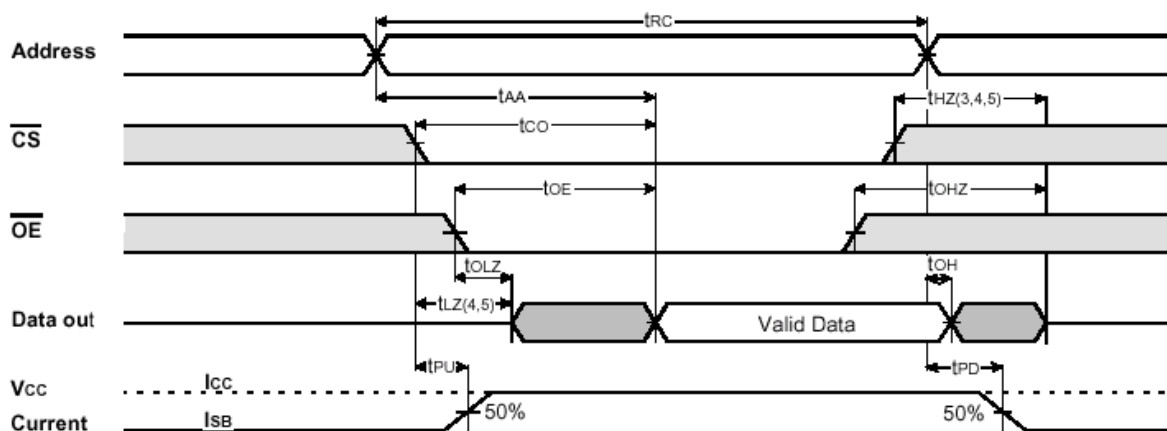
TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled,  $\overline{CS}=\overline{OE}=V_{IL}$ ,  $\overline{WE}=V_{IH}$ )

FIGURE 2: TIMING WAVEFORM OF READ CYCLE (2)

TIMING WAVEFORM OF READ CYCLE(2) ( $\overline{WE}=V_{IH}$ )Read Cycle Notes:

1.  $\overline{WE}$  is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit condition and are not referenced to  $V_{OH}$  or  $V_{OL}$  levels.
4. At any given temperature and voltage condition,  $t_{HZ(max)}$  is less than  $t_{LZ(min)}$  both for a given device and from device to device.
5. Transition is measured + 200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with  $\overline{CS} = V_{IL}$ .
7. Address valid prior to coincident with  $\overline{CS}$  transition low.
8. For common I/O applications, minimization or elimination of bus contention condition is necessary during read and write cycle.

FIGURE 3: TIMING WAVEFORM OF WRITE CYCLE(1)

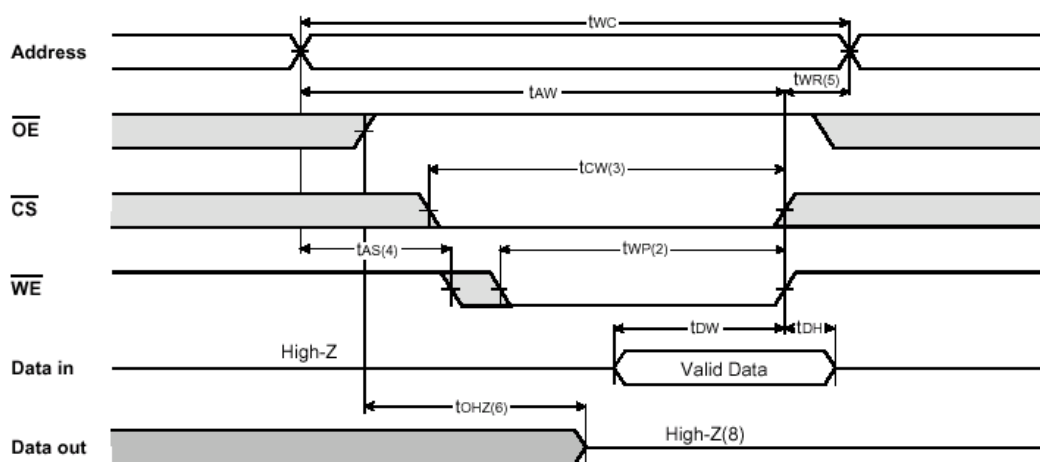
TIMING WAVEFORM OF WRITE CYCLE(1) ( $\overline{OE}$ = Clock)

FIGURE 4: TIMING WAVEFORM OF WRITE CYCLE(2)

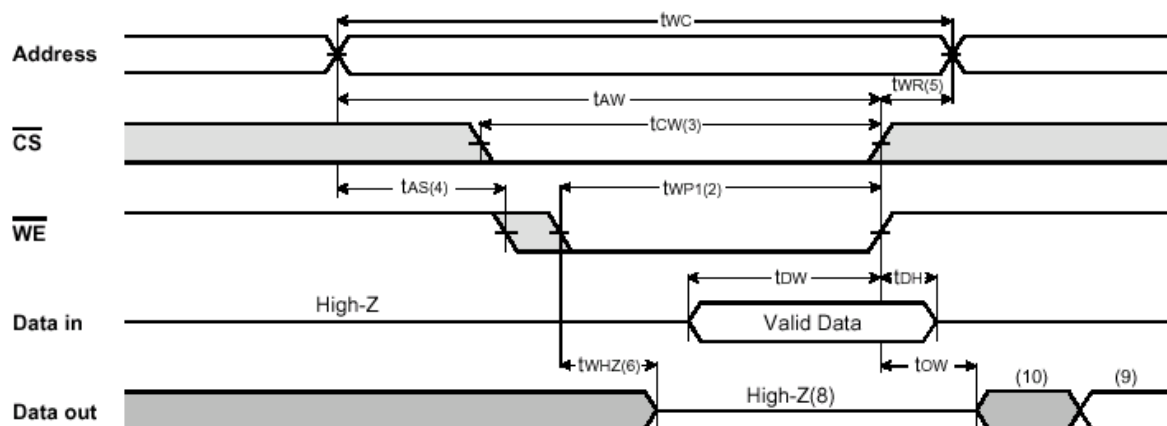
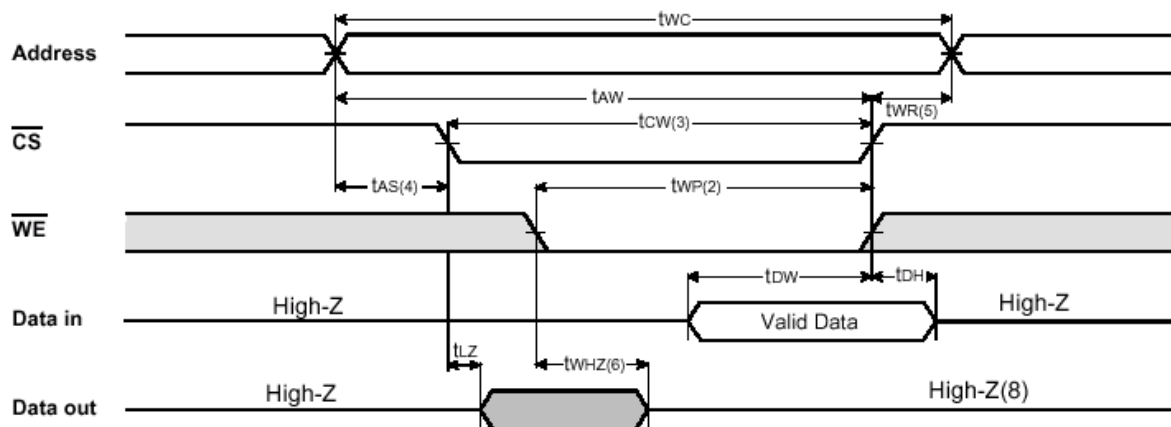
TIMING WAVEFORM OF WRITE CYCLE(2) ( $\overline{OE}$ =Low Fixed)

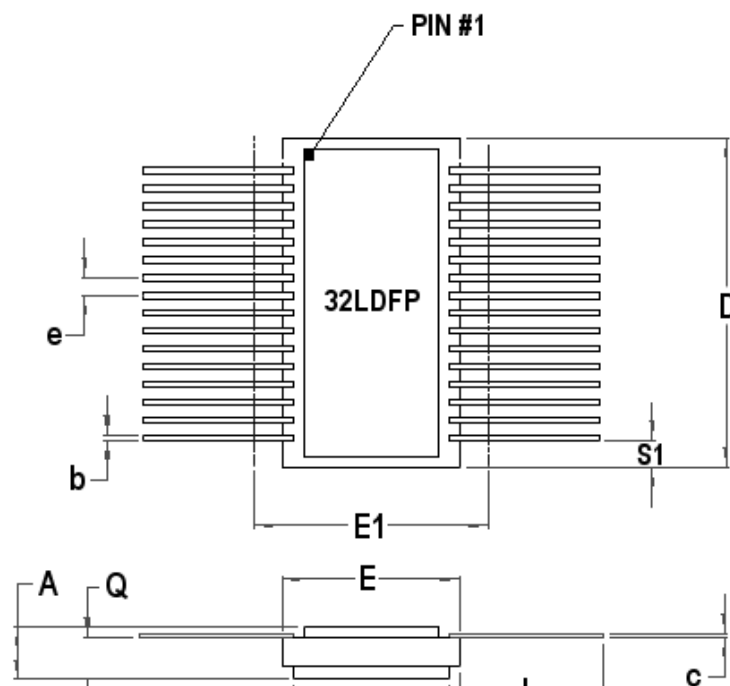


FIGURE 5: TIMING WAVEFORM OF WRITE CYCLE (3)

TIMING WAVEFORM OF WRITE CYCLE(3) ( $\overline{CS}$  = Controlled)

## WRITE CYCLE NOTE:

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low  $\overline{CS}$  and a low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CS}$  going low and  $\overline{WE}$  going low: A write ends at the earliest transition among  $\overline{CS}$  going high and  $\overline{WE}$  going high.  $t_{wp}$  is measured from beginning of write to the end of write.
3.  $t_{cw}$  is measured from the later of  $\overline{CS}$  going low to end of write.
4.  $t_{as}$  is measured from the address valid to the beginning of write.
5.  $t_{wr}$  is measured from the end of write to the address change. TWR applied in case a write ends as  $\overline{CS}$ , or  $\overline{WE}$  going high.
6. If  $\overline{OE}$ ,  $\overline{CS}$  and  $\overline{WE}$  are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If  $\overline{CS}$  goes low simultaneously with  $\overline{WE}$  going low or after  $\overline{WE}$  going low, the outputs remain high impedance state.
9.  $D_{out}$  is the read data of the new address.
10. When  $\overline{CS}$  is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.



32 PIN RAD-PAK® FLAT PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.122	0.135	0.155
b	0.015	0.017	0.019
c	0.008	0.010	0.012
D	--	0.930	0.940
E	0.635	0.645	0.655
E1	--	--	0.690
E2	0.550	0.565	--
E3	--	0.040	--
e	0.050 BSC		
L	0.390	0.400	0.410
Q	0.088	0.098	.108
S1	--	0.082	--
N	32		

Note: All dimensions in inches

## Important Notice:

These data sheets are created using the chip manufacturers published specifications. Maxwell Technologies verifies functionality by testing key parameters either by 100% testing, sample testing or characterization.

The specifications presented within these data sheets represent the latest and most accurate information available to date. However, these specifications are subject to change without notice and Maxwell Technologies assumes no responsibility for the use of this information.

Maxwell Technologies' products are not authorized for use as critical components in life support devices or systems without express written approval from Maxwell Technologies.

Any claim against Maxwell Technologies must be made within 90 days from the date of shipment from Maxwell Technologies. Maxwell Technologies' liability shall be limited to replacement of defective parts.

# 4 Megabit (512K x 8-Bit) CMOS SRAM

# 33LV408

## Product Ordering Options

