



32M-BIT MASK ROM (16/32 BIT OUTPUT)

- Bit organization
 - 2M x 16 (word mode)
 - 1M x 32 (double word mode)
- Fast access time
 - Random access: 100ns (max.)
 - Page access: 30ns (max.)
- Page
 - 8 double words per page
- Current
 - Operating:60mA
 - Standby:50uA
- Supply voltage
 - 3.3V±10%
- Package
 - 70 pin SSOP (500mil)

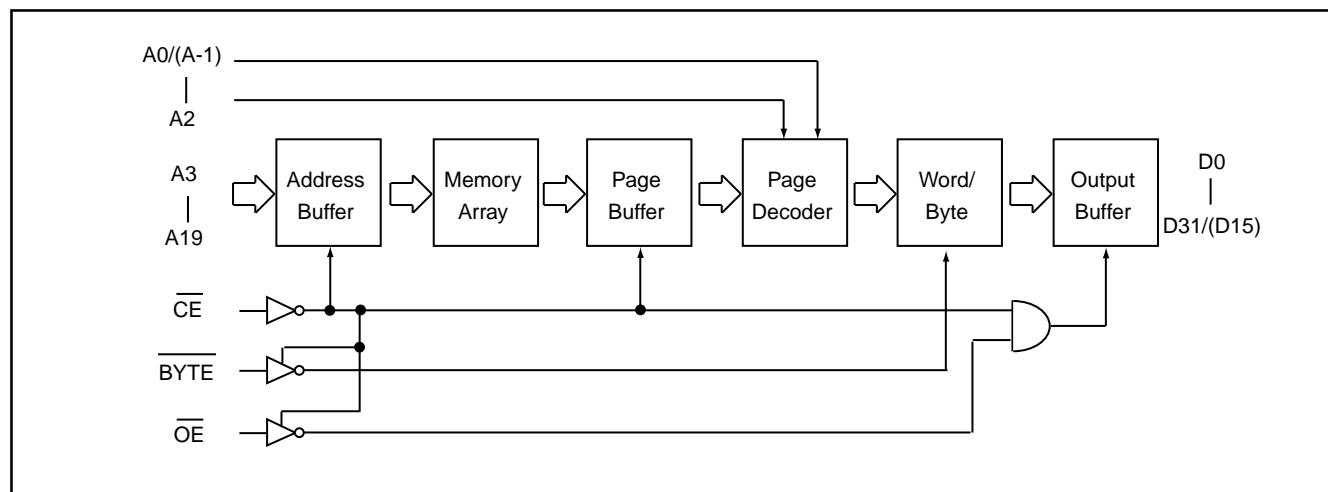
A0	○	70	NC
A1	2	69	NC
A2	3	68	NC
A3	4	67	WORD
A4	5	66	OE
A5	6	65	CE
VCC	7	64	VSS
D0	8	63	D31/A-1
D16	9	62	D15
D1	10	61	D30
D17	11	60	D14
VSS	12	59	VSS
VCC	13	58	VCC
D2	14	57	D29
D18	15	56	D13
D3	16	55	D28
D19	17	54	D12
D4	18	53	D27
D20	19	52	D11
D5	20	51	D26
D21	21	50	D10
VSS	22	49	VSS
VCC	23	48	VCC
D6	24	47	D25
D22	25	46	D9
D7	26	45	D24
D23	27	44	D8
VSS	28	43	VCC
A6	29	42	A19
A7	30	41	A18
A8	31	40	A17
A9	32	39	A16
A10	33	38	A15
A11	34	37	A14
A12	35	36	A13

Symbol	Pin Function
A0~A19	Address Inputs
D0~D30	Data Outputs
D31/A-1	D15 (Word Mode)/ LSB Address (Byte Mode)
$\overline{\text{CE}}$	Chip Enable Input
$\overline{\text{OE}}$	Output Enable Input
$\overline{\text{WORD}}$	Double Word/ Word Mode Selection
VCC	Power Supply Pin
VSS	Ground Pin
NC	No Connection

Part No.	Access Time	Page Access Time	Package
MX23L3222MC-10	100ns	30ns	70 pin SSOP
MX23L3222MC-12	120ns	45ns	70 pin SSOP

MODE SELECTION

$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WORD}}$	D31/A-1	D0~D15	D16~D31	Mode	Power
H	X	X	X	High Z	High Z	-	Stand-by
L	H	X	X	High Z	High Z	-	Active
L	L	H	Output	D0~D15	D16~D31	Double Word	Active
L	L	L	Input	D0~D15	High Z	Word	Active

BLOCK DIAGRAM


ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings
Voltage on any Pin Relative to VSS	VIN	-1.3V to VCC+2.0V (Note)
Ambient Operating Temperature	Topr	0°C to 70°C
Storage Temperature	Tstg	-65°C to 125°C

Note: Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may undershoot VSS to -1.3V for periods of up to 20ns. Maximum DC voltage on input or I/O pins is VCC+0.5V. During voltage transitions, input may overshoot VCC to VCC+2.0V for periods of up to 20ns.

DC CHARACTERISTICS (Ta = 0°C ~ 70°C, VCC = 3.3V±10%)

Item	Symbol	MIN.	MAX.	Conditions
Output High Voltage	VOH	2.4V	-	IOH = -0.4mA
Output Low Voltage	VOL	-	0.4V	IOL = 1.6mA
Input High Voltage	VIH	2.2V	VCC+0.3V	
Input Low Voltage	VIL	-0.3V	0.8V	
Input Leakage Current	ILI	-	5uA	0V, VCC
Output Leakage Current	ILO	-	5uA	0V, VCC
Operating Current	ICC1	-	60mA	tRC = 100ns, all output open
Standby Current (TTL)	ISTB1	-	1mA	\overline{CE} = VIH
Standby Current (CMOS)	ISTB2	-	50uA	\overline{CE} > VCC-0.2V
Input Capacitance	CIN	-	10pF	Ta = 25°C, f = 1MHZ
Output Capacitance	COUT	-	10pF	Ta = 25°C, f = 1MHZ

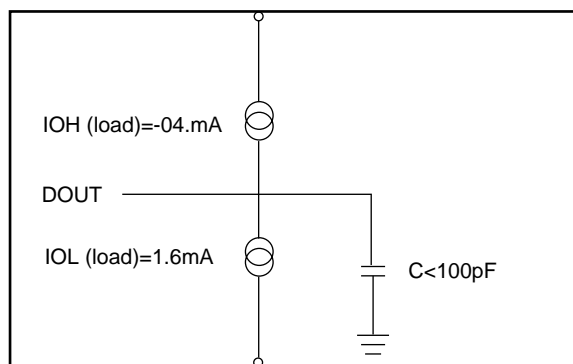
AC CHARACTERISTICS (Ta = 0°C ~ 70°C, VCC = 3.3V±10%)

Item	Symbol	23L3222-10		23L3222-12	
		MIN.	MAX.	MIN.	MAX.
Read Cycle Time	tRC	100ns	-	120ns	-
Address Access Time	tAA	-	100ns	-	120ns
Chip Enable Access Time	tACE	-	30ns	-	45ns
Page Mode Access Time	tPA	-	30ns	-	45ns
Output Enable Time	tOE	-	30ns	-	45ns
Output Hold After Address	tOH	0ns	-	0ns	-
Output High Z Delay	tHZ	-	20ns	-	20ns

Note: Output high-impedance delay (tHZ) is measured from \overline{OE} or \overline{CE} going high, and this parameter guaranteed by design over the full voltage and temperature operating range - not tested.

AC Test Conditions

Input Pulse Levels	0.4V~ 2.4V
Input Rise and Fall Times	10ns
Input Timing Level	1.5V
Output Timing Level	0.8V and 2.0V
Output Load	See Figure



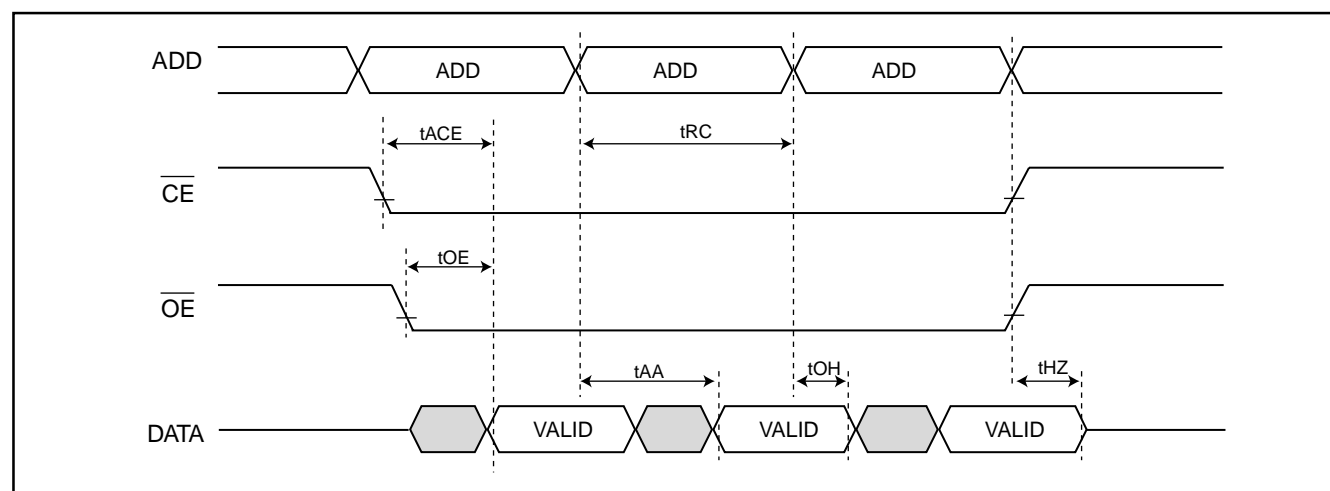
Note: No output loading is present in tester load board.

Active loading is used and under software programming control.

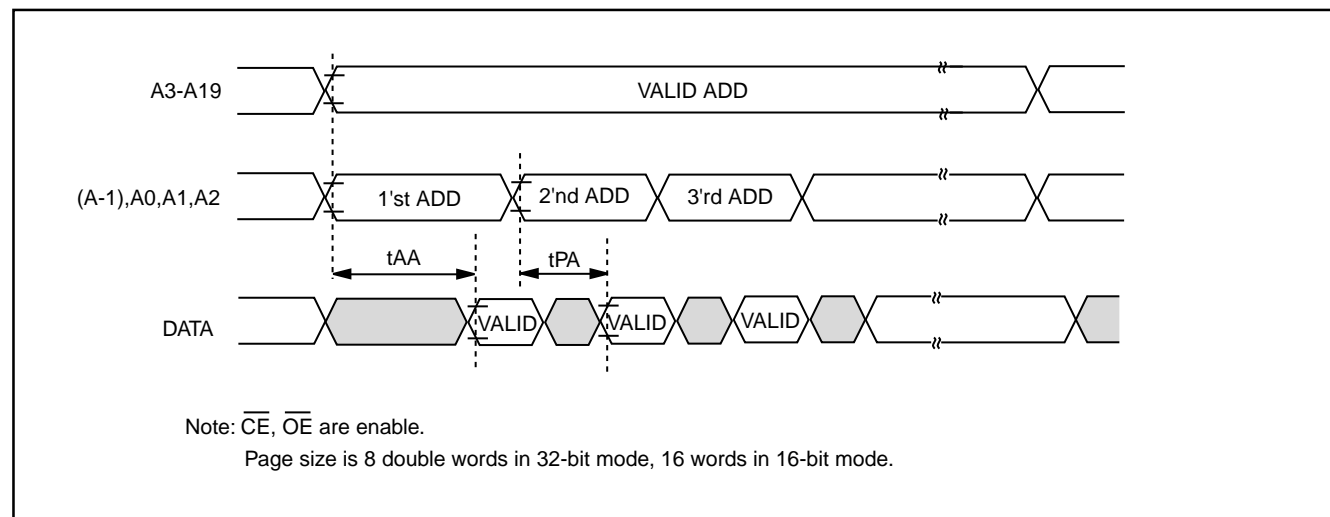
Output loading capacitance includes load board's and all stray capacitance.

TIMING DIAGRAM

RANDOM READ



PAGE READ



REVISION HISTORY

Revision	Description	Page	Date
1.8	AC Characteristics: The page mode access time (tPA) and output enable time (tOE) are changed as 45ns instead of 50ns. Added 100ns speed grade. Package: Added 100 pin TQFP package, dimension is 14mm x 14mm x 1mm.		MAR/25/1998
1.9	AC CHARACTERISTICS tOH 10ns-->0ns	P3	JAN/29/1999
2.0	Delete package:100-pin TQFP	P1,2	OCT/19/2001



MX23L3222

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