



#### FEATURES

##### GENERAL

- Serial Peripheral Interface (SPI) compatible -- Mode 0 and Mode 3
- 16,777,216 x 1 bit structure
- 32 Equal Sectors with 64K byte each
  - Any sector can be erased
- Single Power Supply Operation
  - 2.7 to 3.6 volt for read, erase, and program operations
- Latch-up protected to 100mA from -1V to Vcc +1V
- Low Vcc write inhibit is from 1.5V to 2.5V

##### PERFORMANCE

- High Performance
  - Fast access time: 50MHz serial clock (30pF + 1TTL Load)
  - Fast program time: 3ms/page (typical, 256-byte per page)
  - Fast erase time: 1s/sector (typical, 64K-byte per sector) and 32s/chip (typical)
  - Acceleration mode:
    - Program time: 2.4ms/page (typical)
    - Erase time: 0.8s/sector (typical) and 25s/chip (typical)
- Low Power Consumption
  - Low active read current: 30mA (max.) at 50MHz
  - Low active programming current: 30mA (max.)
  - Low active erase current: 38mA (max.)
  - Low standby current: 50uA (max.)
  - Deep power-down mode 1uA (typical)
- Minimum 10K erase/program cycle for array
- Minimum 100K erase/program cycle for additional 4Kb

##### SOFTWARE FEATURES

- Input Data Format
  - 1-byte Command code
- Auto Erase and Auto Program Algorithm

- Automatically erases and verifies data at selected sector
- Automatically programs and verifies data at selected page by an internal algorithm that automatically times the program pulse widths (Any page to be programmed should have page in the erased state first)
- Status Register Feature
- Electronic Identification
  - JEDEC 2-byte Device ID
  - RES command, 1-byte Device ID
  - REMS command, ADD=00H will output the manufacturer's ID first and ADD=01H will output device ID first
- Additional 4Kb sector independent from main memory for parameter storage to eliminate EEPROM from system

##### HARDWARE FEATURES

- SCLK Input
  - Serial clock input
- SI Input
  - Serial Data Input
- SO/PO7
  - Serial Data Output or Parallel mode Data output/input
- WP#/ACC Pin
  - Hardware write protection and Program/erase acceleration
- HOLD# pin
  - pause the chip without deselecting the chip (not for parallel mode, please connect HOLD# pin to VCC during parallel mode)
- PO0~PO6
  - for parallel mode data output/input
- PACKAGE
  - 8-land SON (8x6mm)

## GENERAL DESCRIPTION

The MX25L1605 is a CMOS 16,777,216 bit serial eLiteFlash™ Memory, which is configured as 2,097,152 x 8 internally. The MX25L1605 features a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). SPI access to the device is enabled by CS# input.

The MX25L1605 provide sequential read operation on whole chip. User may start to read from any byte of the array. While the end of the array is reached, the device will wrap around to the beginning of the array and continuously outputs data until CS# goes high.

After program/erase command is issued, auto program/erase algorithms which program/erase and verify the specified page locations will be executed. Program command is executed on a page (256 bytes) basis, and erase command is executed on both chip and sector (64K bytes) basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion and error flag status of a program or erase operation.

To increase user's factory throughputs, a parallel mode is provided. The performance of read/program is dramatically improved than serial mode on programmer machine.

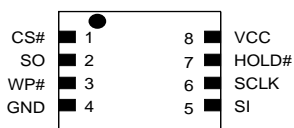
When the device is not in operation and CS# is high, it is put in standby mode and draws less than 50uA DC current.

The additional 4Kb sector with 100K erase/program endurance cycles is suitable for parameter storage and replaces the EEPROM on system.

The MX25L1605 utilizes MXIC's proprietary memory cell which reliably stores memory contents even after 10K program and erase cycles.

## PIN CONFIGURATIONS

### 8-LAND SON (8x6mm small outline no-lead)

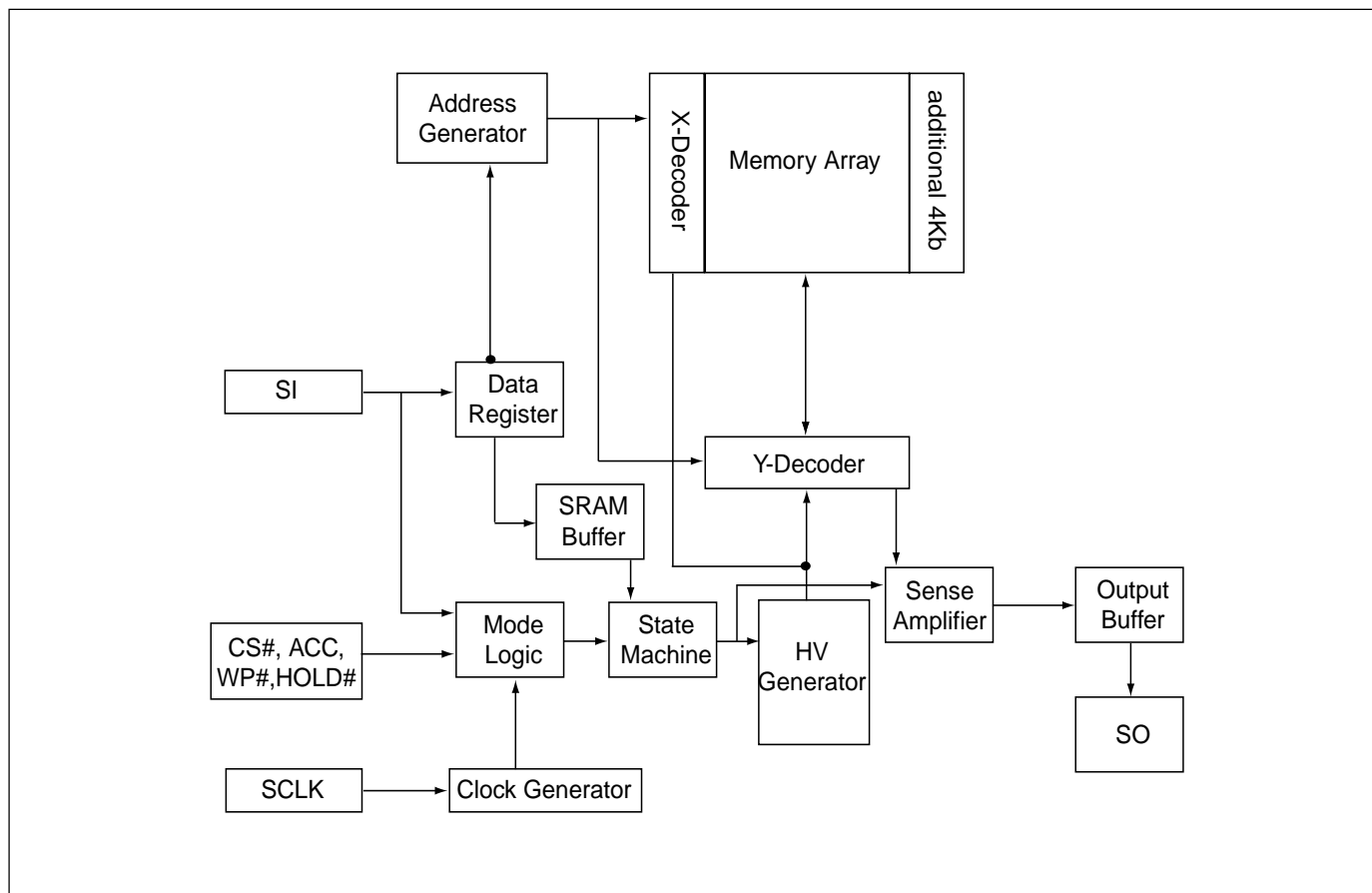


## PIN DESCRIPTION

| SYMBOL    | DESCRIPTION  |
|-----------|--|
| CS#       | Chip Select  |
| SI        | Serial Data Input  |
| SO/PO7(1) | Serial Data Output or Parallel Data output/input                                     |
| SCLK      | Clock Input  |
| HOLD#(2)  | Hold, to pause the serial communication (HOLD# is not for parallel mode)             |
| WP#/ACC   | Write Protection: connect to GND; 12V for program/erase acceleration: connect to 12V |
| VCC       | + 3.3V Power Supply  |
| GND       | Ground   |
| PO0~PO6   | Parallel data output/input (PO0~PO6 can be connected to NC in serial mode)           |
| NC        | No Internal Connection   |

Note:  
HOLD# is recommended to connect to VCC during parallel mode.

## BLOCK DIAGRAM



## DATA PROTECTION

The MX25L1605 are designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transition. During power up the device automatically resets the state machine in the Read mode. In addition, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from VCC power-up and power-down transition or system noise.

- Power-On Reset and an internal timer (tPUW) can provide protection against inadvertent changes while the power supply is outside the operating specification.
- Program, Erase and Write Status Register instructions are checked that they consist of a number of clock pulses that is a multiple of eight, before they are accepted for execution.
- All instructions that modify data must be preceded by a Write Enable (WREN) instruction to set the Write Enable Latch (WEL) bit. This bit is returned to its reset state by the following events:
  - Power-up
  - Write Disable (WRDI) instruction completion
  - Write Status Register (WRSR) instruction completion
  - Page Program (PP) instruction completion
  - Sector Erase (SE) instruction completion
  - Chip Erase (CE) instruction completion
- The Block Protect (BP2, BP1, BP0) bits allow part of the memory to be configured as readonly. This is the Software Protected Mode (SPM).
- The Write Protect (WP#) signal allows the Block Protect (BP2, BP1, BP0) bits and Status Register Write Disable (SRWD) bit to be protected. This is the Hardware Protected Mode (HPM).
- In addition to the low power consumption feature, the Deep Power-down mode offers extra software protection from inadvertent Write, Program and Erase instructions, as all instructions are ignored except one particular instruction (the Release from Deep Powerdown instruction).
- To avoid unexpected changes by system power supply transition, the Power-On Reset and an internal timer (tPUW) can protect the device.
- Before the Program, Erase, and Write Status Register execution, instruction length will be checked on following the clock pulse number to be multiple of eight base.
- Write Enable (WREN) instruction must set to Write Enable Latch (WEL) bit before writing other instructions to modify data. The WEL bit will return to reset state by following situations:
  - Power-up
  - Write Disable (WRDI) instruction completion
  - Write Status Register (WRSR) instruction completion
  - Page Program (PP) instruction completion
  - Sector Erase (SE) instruction completion
  - Chip Erase (CE) instruction completion
- The Software Protected Mode (SPM) use (BP2, BP1, BP0) bits to allow part of memory to be protected as read only.
- The Hardware Protected Mode (HPM) use WP# to protect the (BP2, BP1, BP0) bits and SRWD bit.
- Deep-Power Down Mode also protects the device by ignoring all instructions except Release from Deep-Power Down (RDP) instruction and RES instruction.

**Table 1. Protected Area Sizes**

| Status bit |     |     | Protection Area                          |
|------------|-----|-----|--|
| BP2        | BP1 | BP0 | 16Mb                                     |
| 0          | 0   | 0   | None                                     |
| 0          | 0   | 1   | Upper 32nd (Sector 31)                   |
| 0          | 1   | 0   | Upper sixteenth (two sectors: 30 and 31) |
| 0          | 1   | 1   | Upper eighth (four sectors: 28 to 31)    |
| 1          | 0   | 0   | Upper quarter (eight sectors: 24 to 31)  |
| 1          | 0   | 1   | Upper half (sixteen sectors: 16 to 31)   |
| 1          | 1   | 0   | All                                      |
| 1          | 1   | 1   | All                                      |

**Note:**

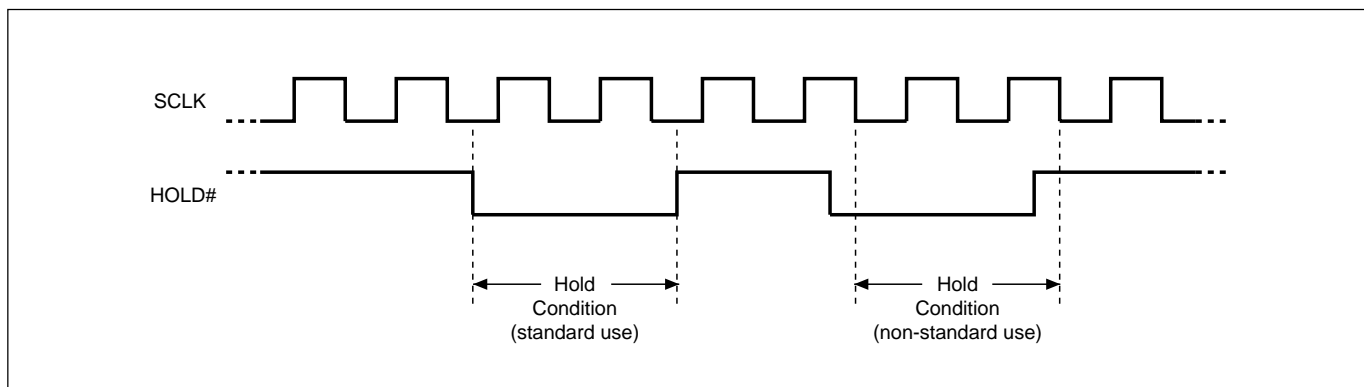
1. The device is ready to accept a Chip Erase instruction if, and only if, all Block Protect (BP2, BP1, BP0) are 0.

## HOLD FEATURE

HOLD# pin signal goes low to hold any serial communications with the device. The HOLD feature will not stop the operation of write status register, programming, or erasing in progress.

The operation of HOLD requires Chip Select(CS#) keeping low and starts on falling edge of HOLD# pin signal while Serial Clock (SCLK) signal is being low (if Serial Clock signal is not being low, HOLD operation will not start until Serial Clock signal being low). The HOLD condition ends on the rising edge of HOLD# pin signal while Serial Clock(SCLK) signal is being low( if Serial Clock signal is not being low, HOLD operation will not end until Serial Clock being low), see Figure 1.

**Figure 1. Hold Condition Operation**



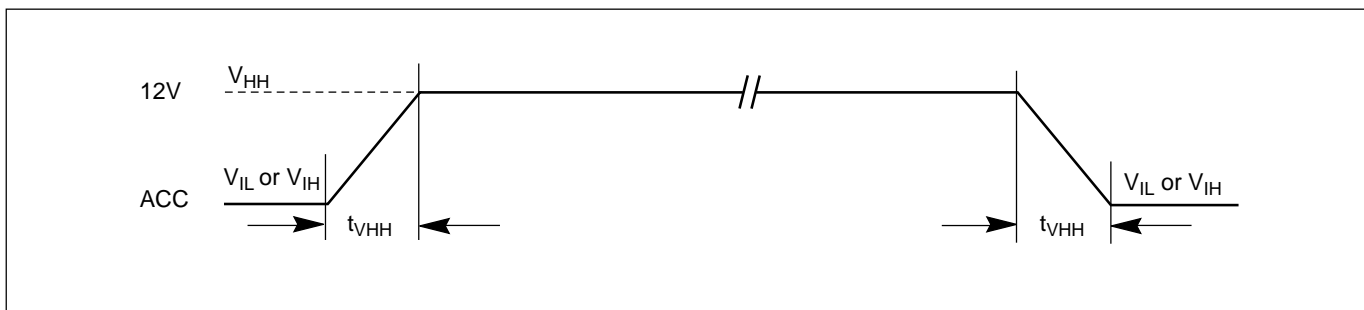
The Serial Data Output (SO) is high impedance, both Serial Data Input (SI) and Serial Clock (SCLK) are don't care during the HOLD operation. If Chip Select (CS#) signal goes high during HOLD operation, it has the effect on resetting the internal logic of the device. It is necessary to drive HOLD# signal to high, and then to drive CS# to low for restarting communication with the device.

The HOLD operation is not recommended to use during parallel mode.

## PROGRAM/ERASE ACCELERATION

To activate the program/erase acceleration function requires ACC pin connecting to 12V voltage (see Figure 2), and then to be followed by the normal program/erase process. By utilizing the program/erase acceleration operation, the performances are improved as shown on table of "ERASE AND PROGRAM PERFORMACE".

**Figure 2. ACCELERATED PROGRAM TIMING DIAGRAM**



Note: t<sub>VHH</sub> (V<sub>HH</sub> Rise and Fall Time) min. 250ns

**Table 2. COMMAND DEFINITION**

| COMMAND<br>(byte) | WREN<br>(write<br>Enable)                         | WRDI<br>(write<br>disable)                         | RDID<br>(read ident-<br>ification)                       | RDSR<br>(read status<br>register)     | WRSR<br>(write status<br>register)               | READ<br>(read data)                              | Fast Read<br>(fast read<br>data) | Parallel<br>Mode  |
|-------------------|---|--|--|---------------------------------------|--|--|----------------------------------|---|
| 1st               | 06 Hex  | 04 Hex   | 9F Hex   | 05 Hex                                | 01 Hex   | 03 Hex   | 0B Hex                           | 55 Hex  |
| 2nd               |   |  |  |                                       |  | AD1  | AD1                              |   |
| 3rd               |   |  |  |                                       |  | AD2  | AD2                              |   |
| 4th               |   |  |  |                                       |  | AD3  | AD3                              |   |
| 5th               |   |  |  |                                       |  |  | x                                |   |
| Action            | sets the<br>(WEL)<br>write<br>enable<br>latch bit | reset the<br>(WEL)<br>write<br>enable<br>latch bit | output the<br>manufacturer<br>ID and 2-byte<br>device ID | to read out<br>the status<br>register | to write new<br>values to the<br>status register | n bytes<br>read out<br>until<br>CS# goes<br>high |                                  | Enter and<br>stay in<br>Parallel<br>Mode until<br>power off |

| COMMAND<br>(byte) | SE<br>(Sector<br>Erase) | CE<br>(Chip<br>Erase) | PP<br>(Page<br>Program) | DP<br>(Deep<br>Power<br>Down) | EN4K<br>(Enter<br>4Kb<br>sector)            | EX4K<br>(Exit<br>4Kb<br>sector)            | RDP<br>(Release<br>from Deep<br>Power-down) | RES(Read<br>Electronic<br>ID) | REMS(Read<br>Electronic<br>Manufacturer<br>& Device ID) |
|-------------------|-------------------------|-----------------------|-------------------------|-------------------------------|---|--|---|-------------------------------|---|
| 1st               | 20 or<br>D8 Hex         | 60 or<br>C7 Hex       | 02 Hex                  | B9 Hex                        | A5 Hex                                      | B5 Hex                                     | AB Hex                                      | AB Hex                        | 90 Hex  |
| 2nd               | AD1                     |                       | AD1                     |                               |   |  |   | x                             | x   |
| 3rd               | AD2                     |                       | AD2                     |                               |   |  |   | x                             | x   |
| 4th               | AD3                     |                       | AD3                     |                               |   |  |   | x                             | ADD (1)   |
| 5th               |                         |                       |                         |                               |   |  |   |                               |   |
| Action            |                         |                       |                         |                               | Enter<br>the<br>additional<br>4Kb<br>sector | Exit<br>the<br>additional<br>4Kb<br>sector |   |                               | Output the<br>manufacturer<br>ID and device<br>ID       |

(1) ADD=00H will output the manufacturer's ID first and ADD=01H will output device ID first

**Table 3. Memory Organization**

| Sector | Address Range |           |
|--------|---------------|-----------|
| 31     | 1F0000h       | 1FFFFFFh  |
| 30     | 1E0000h       | 1EFFFFFFh |
| 29     | 1D0000h       | 1DFFFFFFh |
| 28     | 1C0000h       | 1CFFFFFFh |
| 27     | 1B0000h       | 1BFFFFFFh |
| 26     | 1A0000h       | 1AFFFFFFh |
| 25     | 190000h       | 19FFFFFFh |
| 24     | 180000h       | 18FFFFFFh |
| 23     | 170000h       | 17FFFFFFh |
| 22     | 160000h       | 16FFFFFFh |
| 21     | 150000h       | 15FFFFFFh |
| 20     | 140000h       | 14FFFFFFh |
| 19     | 130000h       | 13FFFFFFh |
| 18     | 120000h       | 12FFFFFFh |
| 17     | 110000h       | 11FFFFFFh |
| 16     | 100000h       | 10FFFFFFh |

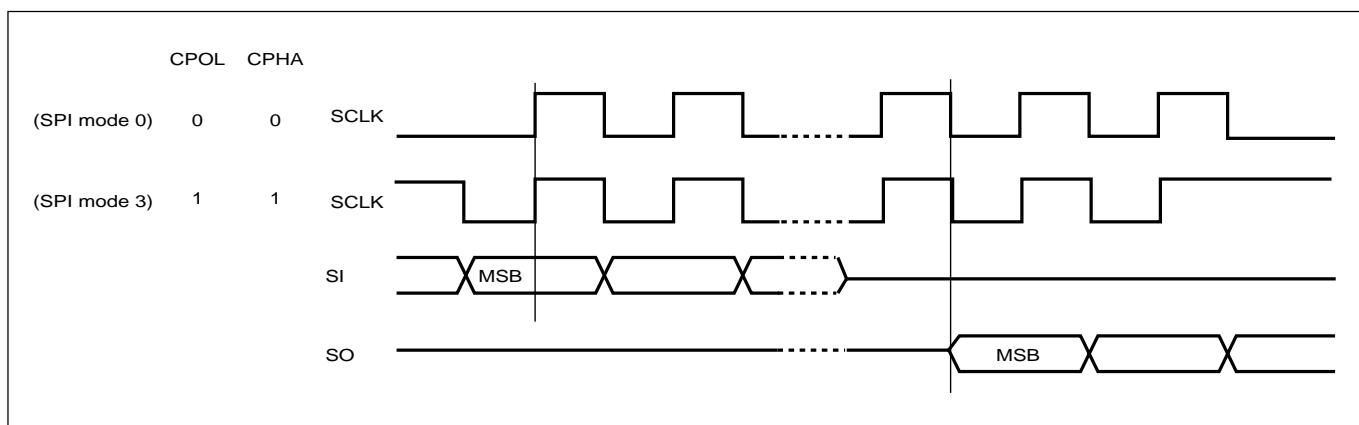
| Sector | Address Range |           |
|--------|---------------|-----------|
| 15     | 0F0000h       | 0FFFFFFh  |
| 14     | 0E0000h       | 0EFFFFFFh |
| 13     | 0D0000h       | 0DFFFFFFh |
| 12     | 0C0000h       | 0CFFFFFFh |
| 11     | 0B0000h       | 0BFFFFFFh |
| 10     | 0A0000h       | 0AFFFFFFh |
| 9      | 090000h       | 09FFFFFFh |
| 8      | 080000h       | 08FFFFFFh |
| 7      | 070000h       | 07FFFFFFh |
| 6      | 060000h       | 06FFFFFFh |
| 5      | 050000h       | 05FFFFFFh |
| 4      | 040000h       | 04FFFFFFh |
| 3      | 030000h       | 03FFFFFFh |
| 2      | 020000h       | 02FFFFFFh |
| 1      | 010000h       | 01FFFFFFh |
| 0      | 000000h       | 00FFFFFFh |



## DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.
2. When incorrect command is inputted to this LSI, this LSI becomes standby mode and keeps the standby mode until next CS# falling edge. In standby mode, SO pin of this LSI should be High-Z.
3. When correct command is inputted to this LSI, this LSI becomes active mode and keeps the active mode until next CS# rising edge.
4. Input data is latched on the rising edge of Serial Clock(SCLK) and data shifts out on the falling edge of SCLK. The difference of SPI mode 0 and mode 3 is shown as Figure 3.

**Figure 3. SPI Modes Supported**



5. For the following instructions: RDID, RDSR, READ, FAST\_READ, RES, and REMS-the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, Parallel Mode, SE, CE, PP, EN4K, EX4K, RDP and DP the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.
6. During the progress of Write Status Register, Program, Erase operation, to access the memory array is neglected and not affect the current operation of Write Status Register, Program, Erase.

**COMMAND DESCRIPTION****(1) Write Enable (WREN)**

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP, SE, CE, and WRSR, which are intended to change the device content, should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low-> sending WREN instruction code-> CS# goes high. (see Figure 12)

**(2) Write Disable (WRDI)**

The Write Disable (WRDI) instruction is for re-setting Write Enable Latch (WEL) bit.

The sequence of issuing WRDI instruction is: CS# goes low-> sending WRDI instruction code-> CS# goes high. (see Figure 13)

The WEL bit is reset by following situations:

- Power-up
- Write Disable (WRDI) instruction completion
- Write Status Register (WRSR) instruction completion
- Page Program (PP) instruction completion
- Sector Erase (SE) instruction completion
- Chip Erase (CE) instruction completion

**(3) Read Identification (RDID)**

The RDID instruction is for reading the manufacturer ID of 1-byte and followed by Device ID of 2-byte. The MXIC Manufacturer ID is C2(hex), the memory type ID is 20(hex) as the first-byte device ID, and the individual device ID of second-byte ID is as followings: 15(hex) for MX25L1605.

The sequence of issuing RDID instruction is: CS# goes low-> sending RDID instruction code -> 24-bits ID data out on SO -> to end RDID operation can use CS# to high at any time during data out. (see Figure. 14)

While Program/Erase operation is in progress, it will not decode the RDID instruction, so there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

#### (4) Read Status Register (RDSR)

The RDSR instruction is for reading Status Register Bits. The Read Status Register can be read at any time (even in program/erase/write status register condition) and continuously. It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.

The sequence of issuing RDSR instruction is: CS# goes low-> sending RDSR instruction code-> Status Register data out on SO (see Figure. 15)

The definition of the status register bits is as below:

**WIP bit.** The Write in Progress (WIP) bit, a volatile bit, indicates whether the device is busy in program/erase/write status register progress. When WIP bit sets to 1, which means the device is busy in program/erase/write status register progress. When WIP bit sets to 0, which means the device is not in progress of program/erase/write status register cycle.

**WEL bit.** The Write Enable Latch (WEL) bit, a volatile bit, indicates whether the device is set to internal write enable latch. When WEL bit sets to 1, which means the internal write enable latch is set, the device can accept program/erase/write status register instruction. When WEL bit sets to 0, which means no internal write enable latch; the device will not accept program/erase/write status register instruction.

**BP2, BP1, BP0 bits.** The Block Protect (BP2, BP1, BP0) bits, non-volatile bits, indicate the protected area(as defined in table 1) of the device to against the program/erase instruction without hardware protection mode being set. To write the Block Protect (BP2, BP1, BP0) bits requires the Write Status Register (WRSR) instruction to be executed. Those bits define the protected area of the memory to against Page Program (PP), Sector Erase (SE), and Chip Erase(CE) instructions (only if all Block Protect bits set to 0, the CE instruction can be executed)

**Program/erase error bit.** When the program/erase bit set to 1, there is an error occurred in last program/erase operation. The Flash may accept a new program/erase command to re-do program/erase operation.

**SRWD bit.** The Status Register Write Disable (SRWD) bit, non-volatile bit, is operated together with Write Protection (WP#) pin for providing hardware protection mode. The hardware protection mode requires SRWD sets to 1 and WP# pin signal is low stage. In the hardware protection mode, the Write Status Register (WRSR) instruction is no longer accepted for execution and the SRWD bit and Block Protect bits (BP2, BP1, BP0) are read only.

| bit 7                                       | bit 6                      | bit 5 | bit 4                                     | bit 3                                     | bit 2                                     | bit 1                                   | bit 0  |
|---|----------------------------|-------|---|---|---|---|--|
| SRWD<br>Status<br>Register Write<br>Protect | Program/<br>erase<br>error | 0     | BP2<br>the level of<br>protected<br>block | BP1<br>the level of<br>protected<br>block | BP0<br>the level of<br>protected<br>block | WEL<br>(write enable<br>latch)          | WIP<br>(write in progress<br>bit)                |
| 1= status<br>register write<br>disable      | 1=error                    |       | (note 1)                                  | (note 1)                                  | (note 1)                                  | 1=write enable<br>0=not write<br>enable | 1=write operation<br>0=not in write<br>operation |

Note: 1. See the table "Protected Area Sizes".

## (5) Write Status Register (WRSR)

The WRSR instruction is for changing the values of Status Register Bits. Before sending WRSR instruction, the Write Enable (WREN) instruction must be decoded and executed to set the Write Enable Latch (WEL) bit in advance. The WRSR instruction can change the value of Block Protect (BP2, BP1, BP0) bits to define the protected area of memory (as shown in table 1). The WRSR also can set or reset the Status Register Write Disable (SRWD) bit in accordance with Write Protection (WP#) pin signal. The WRSR instruction cannot be executed once the Hardware Protected Mode (HPM) is entered.

The sequence of issuing WRSR instruction is: CS# goes low-> sending WRSR instruction code-> Status Register data on SI-> CS# goes high. (see Figure 16)

The WRSR instruction has no effect on b6, b5, b1, b0 of the status register.

The CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

**Table 4. Protection Modes**

| WP#<br>Signal | SRWD<br>Bit | Mode                           | Write Protection of the<br>Status Register   | Memory Content  |  |
|---------------|-------------|--------------------------------|--|---|--|
|               |             |                                |  | Protected Area <sup>1</sup>                                       | Unprotected Area <sup>1</sup>                                    |
| 1             | 0           | Software<br>Protected<br>(SPM) | Status Register is<br>Writable (if the WREN<br>instruction has set the<br>WEL bit)<br>The values in the SRWD,<br>BP2, BP1 and BP0<br>bits can be changed | Protected against Page<br>Program, Sector Erase<br>and Chip Erase | Ready to accept Page<br>Program and Sector<br>Erase instructions |
| 0             | 0           |                                |  |   |  |
| 1             | 1           |                                |  |   |  |
| 0             | 1           | Hardware<br>Protected<br>(HPM) | Status Register is<br>Hardware write protected<br>The values in the SRWD,<br>BP2, BP1 and BP0<br>bits cannot be changed                                  | Protected against Page<br>Program, Sector Erase<br>and Chip Erase | Ready to accept Page<br>Program and Sector<br>Erase instructions |

Note:

1. As defined by the values in the Block Protect (BP2, BP1, BP0) bits of the Status Register, as shown in Table 1.

As the above table showing, the summary of the Software Protected Mode (SPM) and Hardware Protected Mode (HPM).

Software Protected Mode (SPM):

- When SRWD bit=0, no matter WP# is low or high, the WREN instruction may set the WEL bit and can change the values of SRWD, BP2, BP1, BP0. The protected area, which is defined by BP2, BP1, BP0, is at software protected mode (SPM).
- When SRWD bit=1 and WP# is high, the WREN instruction may set the WEL bit can change the values of SRWD, BP2, BP1, BP0. The protected area, which is defined by BP2, BP1, BP0, is at software protected mode (SPM)

Note: If SRWD bit=1 but WP# is low, it is impossible to write the Status Register even if the WEL bit has previously been set. It is rejected to write the Status Register and not be executed.

Hardware Protected Mode (HPM):

- When SRWD bit=1, and then WP# is low (or WP# is low before SRWD bit=1), it enters the hardware protected mode (HPM). The data of the protected area is protected by software protected mode by BP2, BP1, BP0 and hardware protected mode by the WP# to against data modification.

Note: to exit the hardware protected mode requires WP# driving high once the hardware protected mode is entered. If the WP# pin is permanently connected to high, the hardware protected mode can never be entered; only can use software protected mode via BP2, BP1, BP0.

## **(6) Read Data Bytes (READ)**

The read instruction is for reading data out. The address is latched on rising edge of SCLK, and data shifts out on the falling edge of SCLK at a maximum frequency fC. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing READ instruction is: CS# goes low-> sending READ instruction code-> 3-byte address on SI -> data out on SO-> to end READ operation can use CS# to high at any time during data out. (see Figure. 17)

## **(7) Read Data Bytes at Higher Speed (FAST\_READ)**

The FAST\_READ instruction is for quickly reading data out. The address is latched on rising edge of SCLK, and data of each bit shifts out on the falling edge of SCLK at a maximum frequency fR. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FAST\_READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing FAST\_READ instruction is: CS# goes low-> sending FAST\_READ instruction code-> 3-byte address on SI-> 1-dummy byte address on SI->data out on SO-> to end FAST\_READ operation can use CS# to high at any time during data out. (see Figure. 18)

While Program/Erase/Write Status Register cycle is in progress, FAST\_READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

## **(8) Parallel Mode (Highly recommended for production throughputs increasing)**

The parallel mode provides 8 bit inputs/outputs for increasing throughputs of factory production purpose. The parallel mode requires 55H command code, after writing the parallel mode command and then CS# going high, after that, the eLiteFlash™ Memory can be available to accept read/program/read status/read ID/RES/REMS command as the normal writing command procedure. The eLiteFlash™ Memory will be in parallel mode until VCC power-off.

- Only effective for Read Array for normal read(not FAST\_READ), Read Status, Read ID, Page Program, RES and REMS write data period. (refer to Figure 29~34)
- For normal write command (by SI), No effect
- Under parallel mode, the fastest access clock freq. will be changed to 1.5MHz(SCLK pin clock freq.)
- For parallel mode, the tAA will be change to 50ns.

### **(9) Sector Erase (SE)**

The Sector Erase (SE) instruction is for erasing the data of the chosen sector to be "1". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Sector Erase (SE). Any address of the sector (see table 3) is a valid address for Sector Erase (SE) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing SE instruction is: CS# goes low -> sending SE instruction code -> 3-byte address on SI -> CS# goes high. (see Figure 20)

The self-timed Sector Erase Cycle time (tSE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Sector Erase cycle is in progress. The WIP sets 1 during the tSE timing, and sets 0 when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the page is protected by BP2, BP1, BP0 bits, the Sector Erase (SE) instruction will not be executed on the page.

### **(10) Chip Erase (CE)**

The Chip Erase (CE) instruction is for erasing the data of the whole chip to be "1". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Chip Erase (CE). Any address of the sector (see table 3) is a valid address for Chip Erase (CE) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing CE instruction is: CS# goes low -> sending CE instruction code -> CS# goes high. (see Figure 21)

The self-timed Chip Erase Cycle time (tCE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Chip Erase cycle is in progress. The WIP sets 1 during the tBE timing, and sets 0 when Chip Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the chip is protected by BP2, BP1, BP0 bits, the Chip Erase (CE) instruction will not be executed. It will be only executed when BP2, BP1, BP0 all set to "0".

### **(11) Page Program (PP)**

The Page Program (PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Page Program (PP). If the eight least significant address bits (A7-A0) are not all 0, all transmitted data which goes beyond the end of the current page are programmed from the start address if the same page (from the address whose 8 least significant address bits (A7-A0) are all 0). The CS# must keep during the whole Page Program cycle. The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed. If more than 256 bytes are sent to the device, the data of the last 256-byte is programmed at the request page and previous data will be disregarded. If less than 256 bytes are sent to the device, the data is programmed at the request address of the page without effect on other address of the same page.

The sequence of issuing PP instruction is: CS# goes low -> sending PP instruction code -> 3-byte address on SI -> at least 1-byte on data on SI -> CS# goes high. (see Figure 19)

The self-timed Page Program Cycle time (tPP) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Page Program cycle is in progress. The WIP sets 1 during the tPP timing, and sets 0 when Page Program Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the page is protected by BP2, BP1, BP0 bits, the Page Program (PP) instruction will not be executed.

### **(12) Enter 4Kbit Mode (EN4K) and Exit 4Kbit Mode (EX4K)**

Enter and Exit 4kbit mode (EN4K & EX4K) (see Figure 27 & 28)

EN4K and EX4K will not be executed when the chip is in busy state. Enter 4kbit mode then the read and write command will be executed on this 4kbit. All read and write command sequence is the same as the normal array. The address of this 4k bits is: A20~A9=0 and A8~A0 customer defined.

Note 1: Chip erase and WRSR will not be executed in 4kbit mode. During Enter 4Kbit Mode, the following instructions can be accepted: WREN, WRDI, RDID, RDSR, FAST\_READ, READ, SE, PP, DP, RDP, RES, REMS.

Note 2: Chip erase can't erase this 4kbit

About the fail status:

Bit6 of the status register is used to state fail status, bit6=1 means program or erase have been failed. Any new write command will clear this bit.

### **(13) Deep Power-down (DP)**

The Deep Power-down (DP) instruction is for setting the device on the minimizing the power consumption (to entering the Deep Power-down mode), the standby current is reduced from ISB1 to ISB2). The Deep Power-down mode requires the Deep Power-down (DP) instruction to enter, during the Deep Power-down mode, the device is not active and all Write/Program/Erase instruction are ignored. When CS# goes high, it's only in standby mode not deep power-down mode. It's different from Standby mode.

The sequence of issuing DP instruction is: CS# goes low-> sending DP instruction code-> CS# goes high. (see Figure 22)

Once the DP instruction is set, all instruction will be ignored except the Release from Deep Power-down mode (RDP) and Read Electronic Signature (RES) instruction. (RES instruction to allow the ID been read out). When Power-down, the deep power-down mode automatically stops, and when power-up, the device automatically is in standby mode. For RDP instruction the CS# must go high exactly at the byte boundary (the latest eighth bit of instruction code been latched-in); otherwise, the instruction will not executed. As soon as Chip Select (CS#) goes high, a delay of tDP is required before entering the Deep Power-down mode and reducing the current to ISB2.

### **(14) Release from Deep Power-down (RDP), Read Electronic Signature (RES)**

The Release from Deep Power-down (RDP) instruction is terminated by driving Chip Select (CS#) High. When Chip Select (CS#) is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Stand-by Power mode is delayed by tRES2, and Chip Select (CS#) must remain High for at least tRES2(max), as specified in Table 6. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

RES instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as table of ID Definitions. This is not the same as RDID instruction. It is not recommended to use for new design. For new design, please use RDID instruction. Even in Deep power-down mode, the RDP, RES, and REMS are also allowed to be executed, only except the device is in progress of program/erase/write cycle; there's no effect on the current program/erase/write cycle in progress.

The sequence is shown as Figure 23,24,25.

The RES instruction is ended by CS# goes high after the ID been read out at least once. The ID outputs repeatedly if

continuously send the additional clock cycles on SCLK while CS# is at low. If the device was not previously in Deep Power-down mode, the device transition to standby mode is immediate. If the device was previously in Deep Power-down mode, there's a delay of tRES2 to transit to standby mode, and CS# must remain to high at least tRES2(max). Once in the standby mode, the device waits to be selected, so it can be receive, decode, and execute instruction.

The RDP instruction is for releasing from Deep Power Down Mode.

### (15) Read Electronic Manufacturer ID & Device ID (REMS)

The REMS instruction is an alternative to the Release from Power-down/Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The REMS instruction is very similar to the Release from Power-down/Device ID instruction. The instruction is initiated by driving the CS# pin low and shift the instruction code "90h" followed by two dummy bytes and one bytes address (A7~A0). After which, the Manufacturer ID for MXIC (C2h) and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in figure 25. The Device ID values are listed in Table of ID Definitions on page 20. If the one-byte address is initially set to 01h, then the device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

**Table of ID Definitions:**

|              |                 |             |                |
|--------------|-----------------|-------------|----------------|
| RDID Command | manufacturer ID | memory type | memory density |
|              | C2              | 20          | 15             |
| RES Command  | electronic ID   |             |                |
|              | 14              |             |                |
| REMS Command | manufacturer ID | device ID   |                |
|              | C2              | 14          |                |



## POWER-ON STATE

At Power-up and Power-down, the device must not be selected (that is Chip Select (CS#) must follow the voltage applied on VCC) until VCC reaches the correct value:

- VCC(min) at Power-up, and then for a further delay of  $t_{VSL}$
- VSS at Power-down

Usually a simple pull-up resistor on Chip Select (CS#) can be used to insure safe and proper Power-up and Power-down.

To avoid data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is included. The logic inside the device is held reset while VCC is less than the POR threshold value,  $V_{WI}$ —all operations are disabled, and the device does not respond to any instruction.

Moreover, the device ignores all Write Enable (WREN), Page Program (PP), Sector Erase (SE), Chip Erase (CE) and Write Status Register (WRSR) instructions until a time delay of  $t_{PUW}$  has elapsed after the moment that VCC rises above the  $V_{WI}$  threshold. However, the correct operation of the device is not guaranteed if, by this time, VCC is still below VCC(min). No Write Status Register, Program or Erase instructions should be sent until the later of:

- $t_{PUW}$  after VCC passed the  $V_{WI}$  threshold
- $t_{VSL}$  after VCC passed the VCC(min) level

These values are specified in Table 7.

If the delay,  $t_{VSL}$ , has elapsed, after VCC has risen above VCC(min), the device can be selected for READ instructions even if the  $t_{PUW}$  delay is not yet fully elapsed.

At Power-up, the device is in the following state:

- The device is in the Standby mode (not the Deep Power-down mode).
- The Write Enable Latch (WEL) bit is reset.

Normal precautions must be taken for supply rail decoupling, to stabilize the VCC feed. Each device in a system should have the VCC rail decoupled by a suitable capacitor close to the package pins. (Generally, this capacitor is of the order of 0.1 $\mu$ F).

At Power-down, when VCC drops from the operating voltage, to below the POR threshold value,  $V_{WI}$ , all operations are disabled and the device does not respond to any instruction. (The designer needs to be aware that if a Power-down occurs while a Write, Program or Erase cycle is in progress, some data corruption can result.)

## ELECTRICAL SPECIFICATIONS

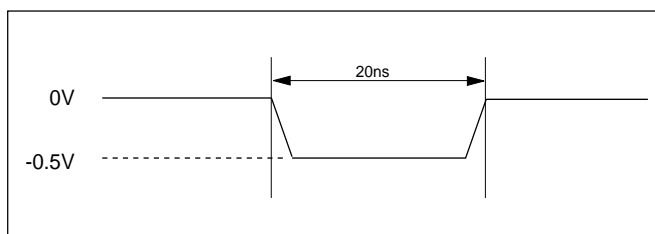
### ABSOLUTE MAXIMUM RATINGS

| RATING                        | VALUE  |
|-------------------------------|--|
| Ambient Operating Temperature | -40°C to 85°C for<br>Industrial grade<br>0°C to 70°C for<br>Commercial grade |
| Storage Temperature           | -55°C to 125°C   |
| Applied Input Voltage         | -0.5V to 4.6V  |
| Applied Output Voltage        | -0.5V to 4.6V  |
| VCC to Ground Potential       | -0.5V to 4.6V  |

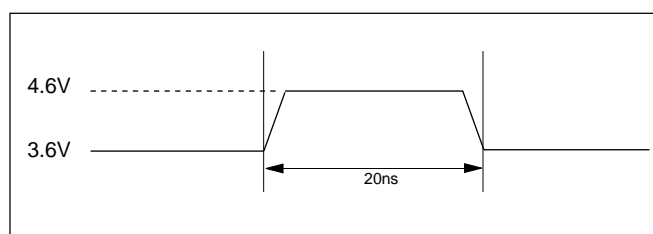
#### NOTICE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
2. Specifications contained within the following tables are subject to change.
3. During voltage transitions, all pins may overshoot to 4.6V or -0.5V for period up to 20ns.
4. All input and output pins may overshoot to VCC+0.5V while VCC+0.5V is smaller than or equal to 4.6V.

**Figure 4. Maximum Negative Overshoot Waveform**

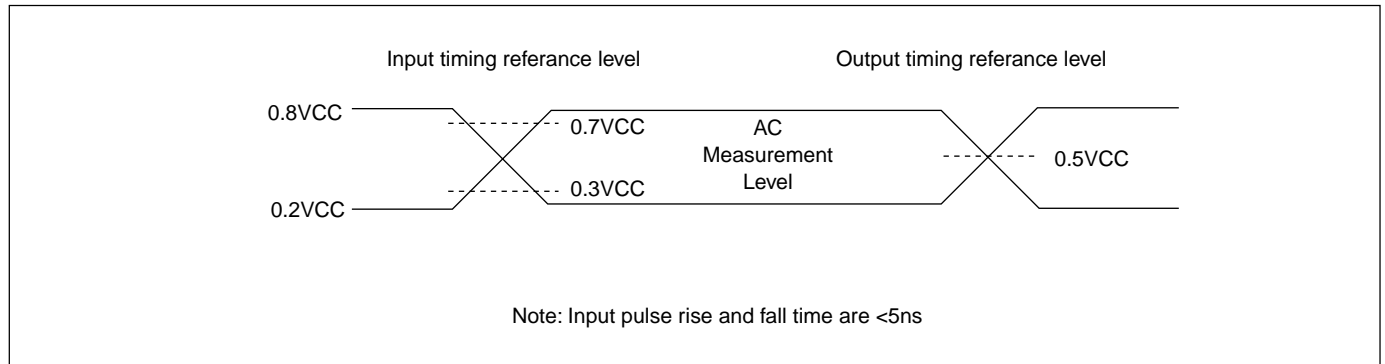
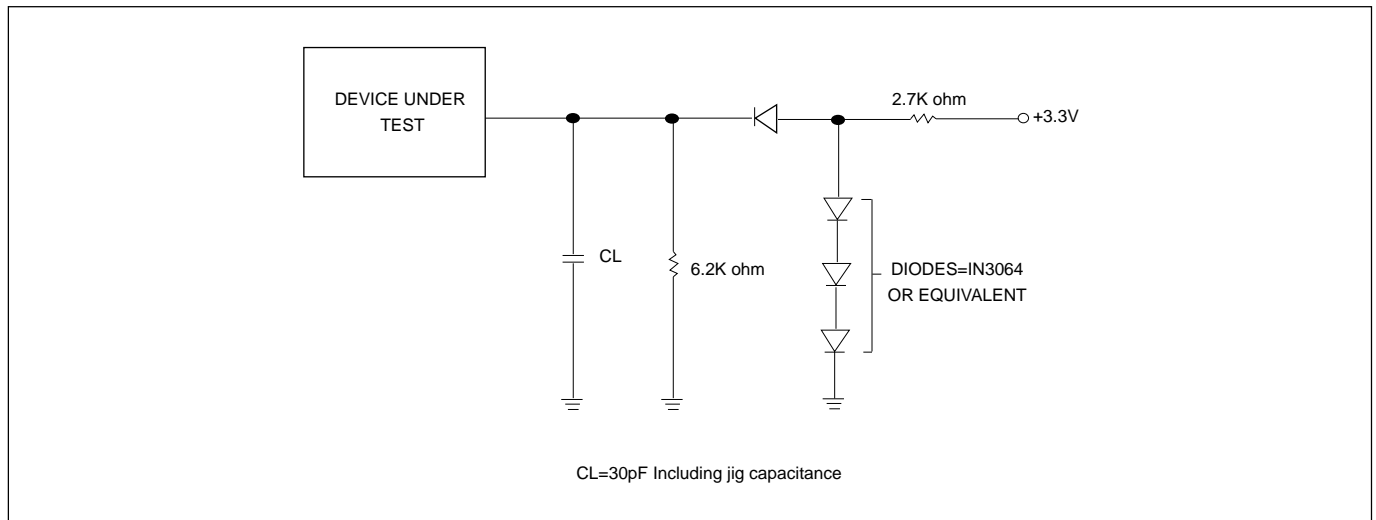


**Figure 5. Maximum Positive Overshoot Waveform**



### CAPACITANCE TA = 25°C, f = 1.0 MHz

| SYMBOL | PARAMETER          | MIN. | TYP | MAX. | UNIT | CONDITIONS |
|--------|--------------------|------|-----|------|------|------------|
| CIN    | Input Capacitance  |      |     | 10   | pF   | VIN = 0V   |
| COUT   | Output Capacitance |      |     | 10   | pF   | VOUT = 0V  |

**Figure 6. INPUT TEST WAVEFORMS AND MEASUREMENT LEVEL**

**Figure 7. OUTPUT LOADING**


**Table 5. DC CHARACTERISTICS (Temperature = -40°C to 85°C for Industrial grade, Temperature = 0°C to 70°C for Commercial grade, VCC = 2.7V ~ 3.6V)**

| SYMBOL | PARAMETER                                | NOTES | MIN.    | TYP | MAX.    | UNITS | TEST CONDITIONS                                |
|--------|--|-------|---------|-----|---------|-------|--|
| ILI    | Input Load Current                       | 1     |         |     | ± 2     | uA    | VCC = VCC Max<br>VIN = VCC or GND              |
| ILO    | Output Leakage Current                   | 1     |         |     | ± 2     | uA    | VCC = VCC Max<br>VIN = VCC or GND              |
| ISB1   | VCC Standby Current                      | 1     |         |     | 50      | uA    | VIN = VCC or GND<br>CS# = VCC                  |
| ISB2   | Deep Power-down Current                  |       |         | 1   | 10      | uA    | VIN = VCC or GND<br>CS# = VCC                  |
| ICC1   | VCC Read                                 | 1     |         |     | 30      | mA    | f=50MHz (serial)                               |
|        |  |       |         |     | 30      | mA    | f=1.5MHz (parallel)                            |
|        |  |       |         |     | 10      | mA    | f=20MHz (serial)                               |
|        |  |       |         |     | 20      | mA    | f=1.2MHz (parallel)                            |
| ICC2   | VCC Program Current (PP)                 | 1     |         |     | 30      | mA    | Program in Progress<br>CS# = VCC               |
| ICC3   | VCC Write Status Register (WRSR) Current |       |         |     | 30      | mA    | Program status register in progress<br>CS#=VCC |
| ICC4   | VCC Sector Erase Current (SE)            | 1     |         |     | 38      | mA    | Erase in Progress<br>CS#=VCC                   |
| ICC5   | VCC Chip Erase Current (CE)              | 1     |         |     | 38      | mA    | Erase in Progress<br>CS#=VCC                   |
| VHH    | Voltage for ACC Program Acceleration     | 1     | 11.5    |     | 12.5    | V     | VCC=2.7V~3.6V                                  |
| VIL    | Input Low Voltage                        |       | -0.5    |     | 0.3VCC  | V     |  |
| VIH    | Input High Voltage                       |       | 0.7VCC  |     | VCC+0.4 | V     |  |
| VOL    | Output Low Voltage                       |       |         |     | 0.4     | V     | IOL = 1.6mA                                    |
| VOH    | Output High Voltage                      |       | VCC-0.2 |     |         | V     | IOH = -100uA                                   |

**NOTES:**

1. Typical values at VCC = 3.3V, T = 25°C. These currents are valid for all product versions (package and speeds).
2. Typical value is calculated by simulation.

**Table 6. AC CHARACTERISTICS (Temperature = -40°C to 85°C for Industrial grade, Temperature = 0°C to 70°C for Commercial grade, VCC = 2.7V ~ 3.6V)**

| Symbol   | Alt. | Parameter   |                     | Min. | Typ. | Max. | Unit |
|----------|------|---|---------------------|------|------|------|------|
| fSCLK    | fC   | Clock Frequency for the following instructions:<br>FAST_READ, PP, SE, BE, DP, RES,REMS, RDP<br>WREN, WRDI, RDID, RDSR, WRSR, EN4K, EX4K | Serial              | D.C. |      | 50   | MHz  |
|          |      |   | Parallel            |      |      | 1.5  | MHz  |
| fRSCLK   | fR   | Clock Frequency for READ instructions   | Serial              | D.C. |      | 20   | MHz  |
|          |      |   | Parallel            |      |      | 1.2  | MHz  |
| tCH(1)   | tCLH | Clock High Time   | Serial              | 9    |      |      | ns   |
|          |      |   | Parallel            | 180  |      |      | ns   |
| tCL(1)   | tCLL | Clock Low Time  | Serial              | 9    |      |      | ns   |
|          |      |   | Parallel            | 180  |      |      | ns   |
| tCLCH(2) |      | Clock Rise Time (3) (peak to peak)  | Serial              | 0.1  |      |      | V/ns |
|          |      |   | Parallel            | 2    |      |      | V/ns |
| tCHCL(2) |      | Clock Fall Time (3) (peak to peak)  | Serial              | 0.1  |      |      | V/ns |
|          |      |   | Parallel            | 2    |      |      | V/ns |
| tSLCH    | tCSS | S Active Setup Time (relative to C)   |                     | 5    |      |      | ns   |
| tCHSL    | S    | Not Active Hold Time (relative to C)  |                     | 5    |      |      | ns   |
| tDVCH    | tDSU | Data In Setup Time  |                     | 2    |      |      | ns   |
| tCHDX    | tDH  | Data In Hold Time   |                     | 5    |      |      | ns   |
| tCHSH    |      | S Active Hold Time (relative to C)  |                     | 5    |      |      | ns   |
| tSHCH    |      | S Not Active Setup Time (relative to C)   |                     | 5    |      |      | ns   |
| tSHSL    | tCSH | S Deselect Time   |                     | 100  |      |      | ns   |
| tSHQZ(2) | tDIS | Output Disable Time   |                     |      |      | 8    | ns   |
| tCLQV    | tV   | Clock Low to Output Valid   |                     |      |      | 8    | ns   |
| tCLQX    | tHO  | Output Hold Time  |                     | 0    |      |      | ns   |
| tHLCH    |      | HOLD# Setup Time (relative to C)  |                     | 5    |      |      | ns   |
| tCHHH    |      | HOLD# Hold Time (relative to C)   |                     | 5    |      |      | ns   |
| tHHCH    |      | HOLD Setup Time (relative to C)   |                     | 5    |      |      | ns   |
| tCHHL    |      | HOLD Hold Time (relative to C)  |                     | 5    |      |      | ns   |
| tHHQX(2) | tLZ  | HOLD to Output Low-Z  |                     |      |      | 8    | ns   |
| tHLQZ(2) | tHZ  | HOLD# to Output High-Z  |                     |      |      | 8    | ns   |
| tWHS(4)  |      | Write Protect Setup Time  |                     | 20   |      |      | ns   |
| tSHWL(4) |      | Write Protect Hold Time   |                     | 100  |      |      | ns   |
| tDP(2)   |      | S High to Deep Power-down Mode  |                     |      |      | 3    | ms   |
| tRES1(2) |      | S High to Standby Mode without Electronic Signature Read  |                     |      |      | 30   | ms   |
| tRES2(2) |      | S High to Standby Mode with Electronic Signature Read   |                     |      |      | 30   | ms   |
| tW       |      | Write Status  | SRWD, BP2, BP1, BP0 |      | 90   | 500  | ms   |
|          |      | Register Cycle Time   | WIP, WEL            |      | 20   | 30   | ns   |
| tPP      |      | Page Program Cycle Time   |                     |      | 3    | 12   | ms   |
| tSE      |      | Sector Erase Cycle Time   |                     |      | 1    | 3    | s    |
| tCE      |      | Chip Erase Cycle Time   |                     |      | 32   | 64   | s    |

Note:

1. tCH + tCL must be greater than or equal to 1/ fC
2. Value guaranteed by characterization, not 100% tested in production.
3. Expressed as a slew-rate.
4. Only applicable as a constraint for a WRSR instruction when SRWD is set at 1.
5. Test condition is shown as Figure 3.

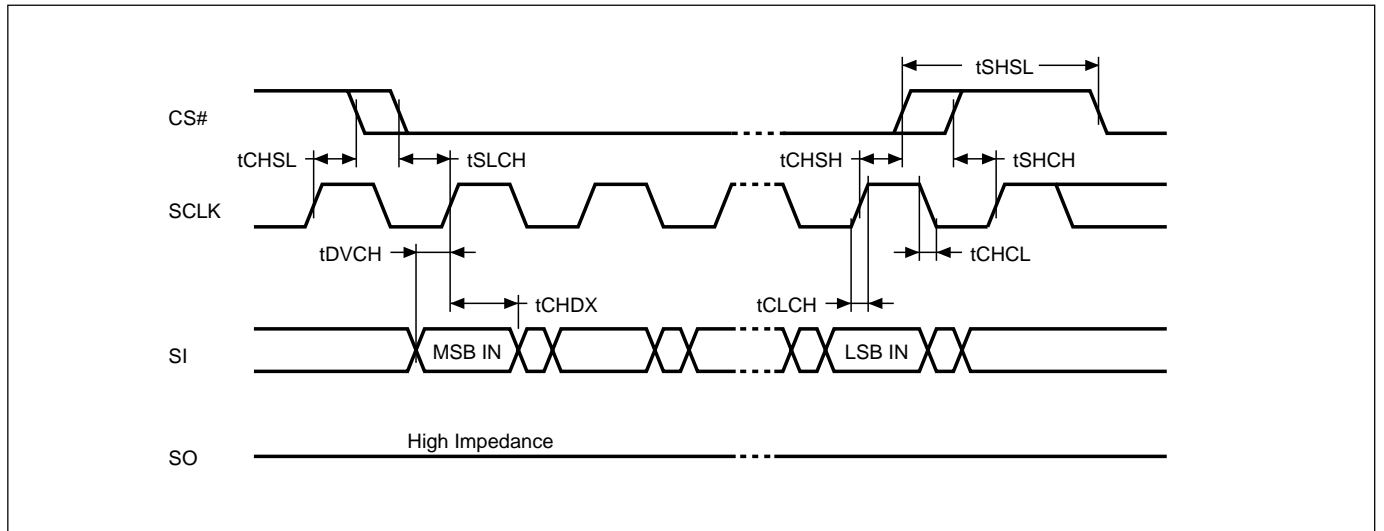
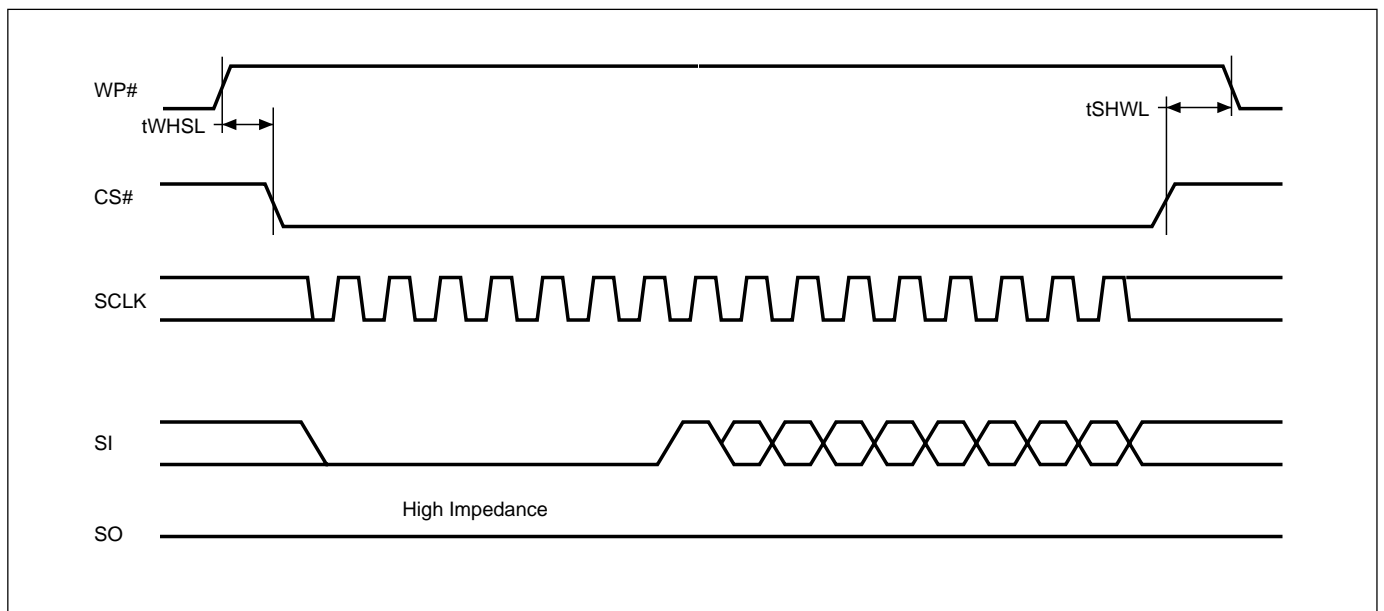
**Table 7. Power-Up Timing and VWI Threshold**

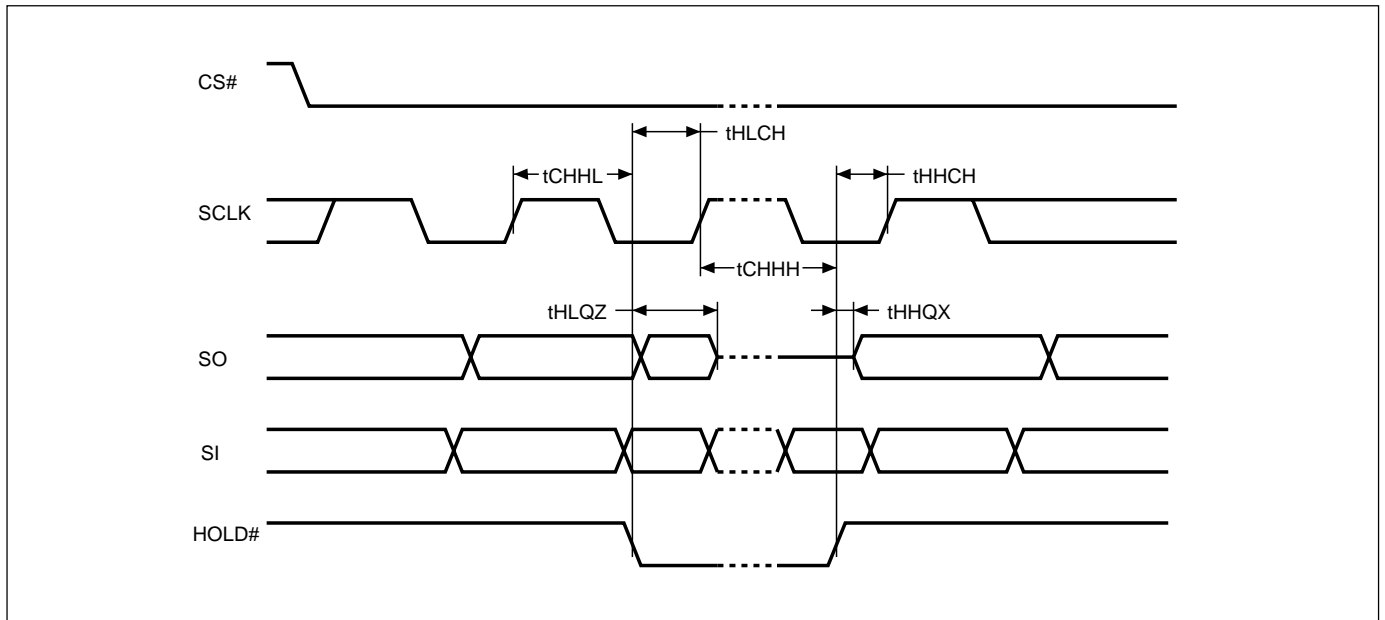
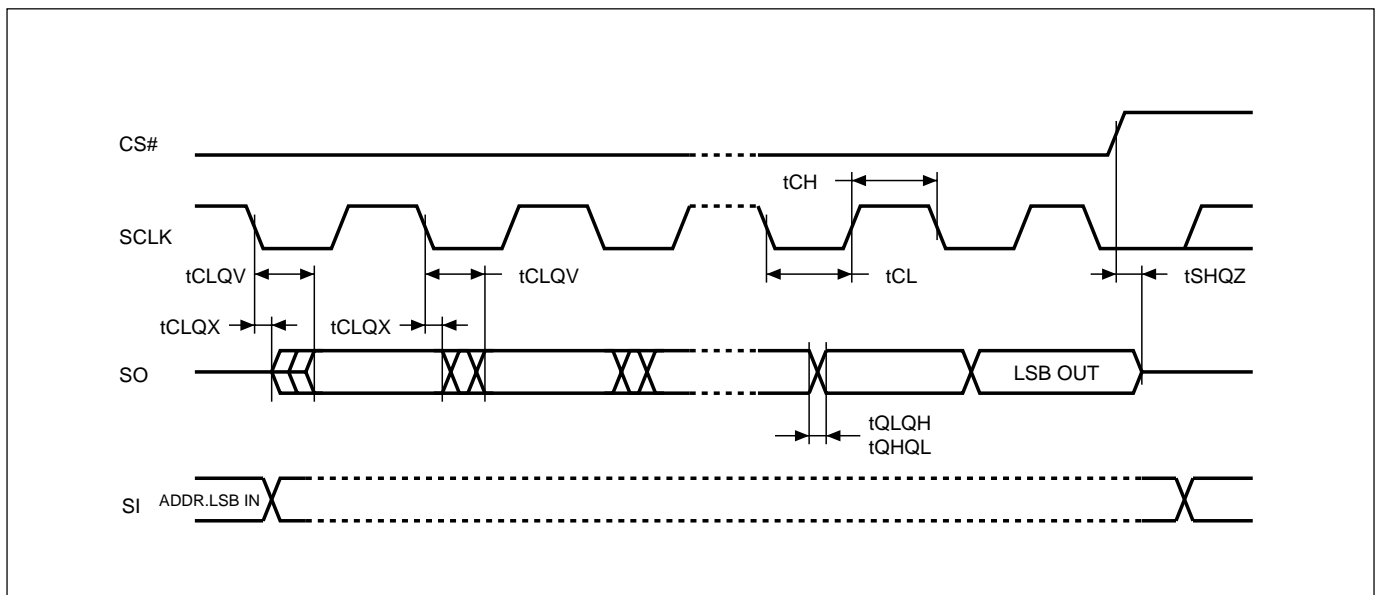
| Symbol  | Parameter                       | Min. | Max. | Unit |
|---------|---------------------------------|------|------|------|
| tVSL(1) | VCC(min) to S low               | 30   |      | us   |
| tPUW(1) | Time delay to Write instruction | 1    | 10   | ms   |
| VWI(1)  | Write Inhibit Voltage           | 1.5  | 2.5  | V    |

Note: 1. These parameters are characterized only.

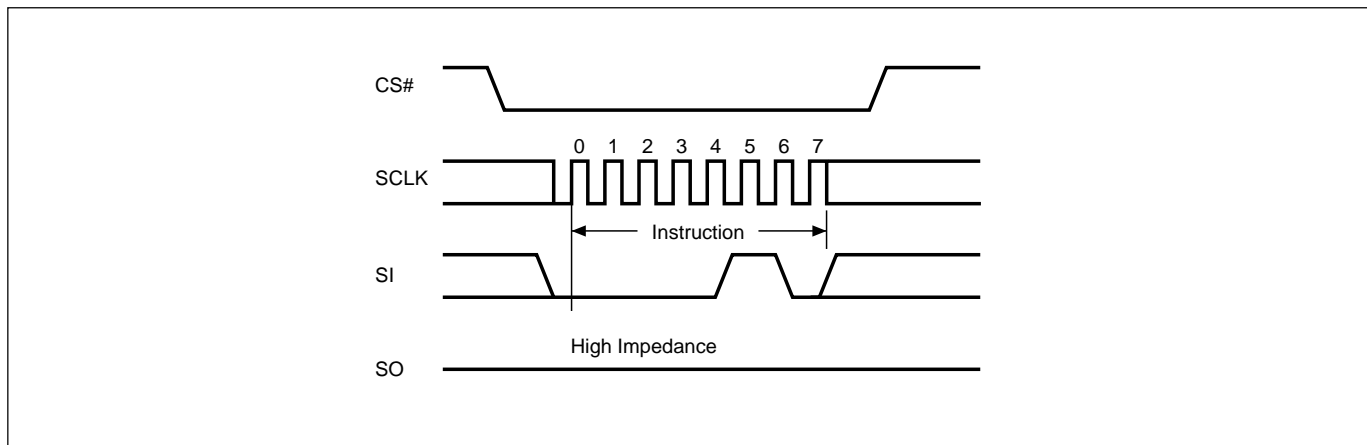
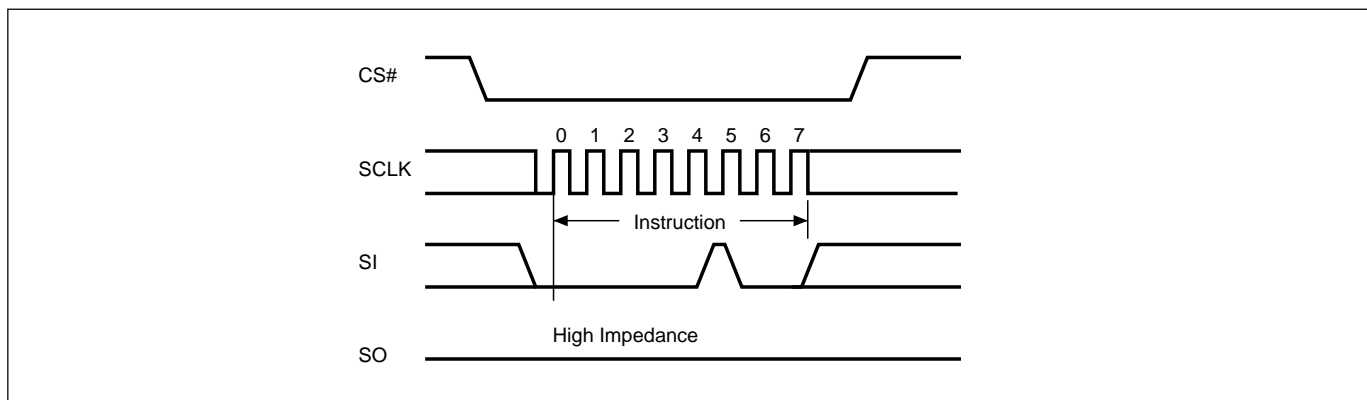
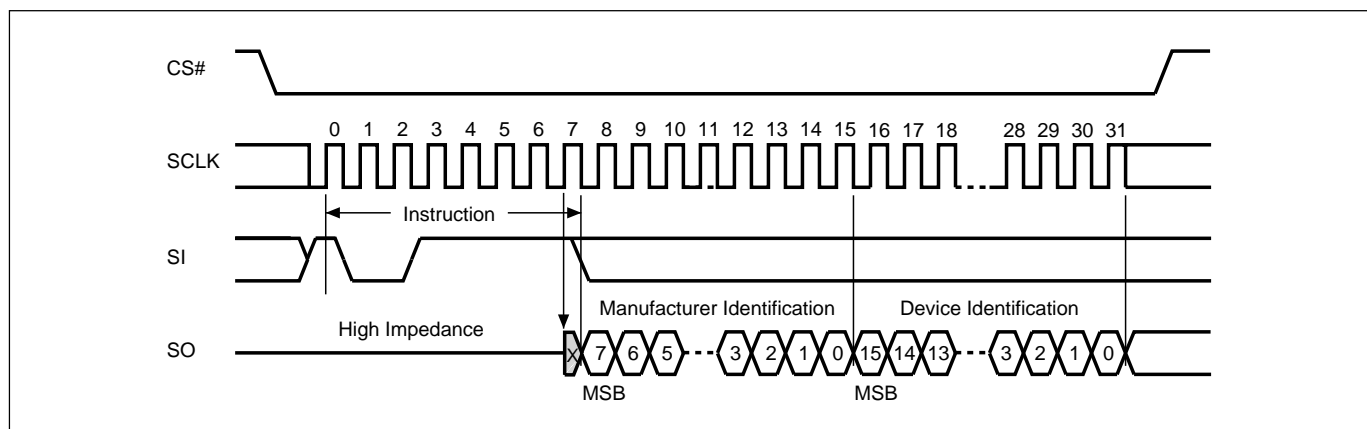
## INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

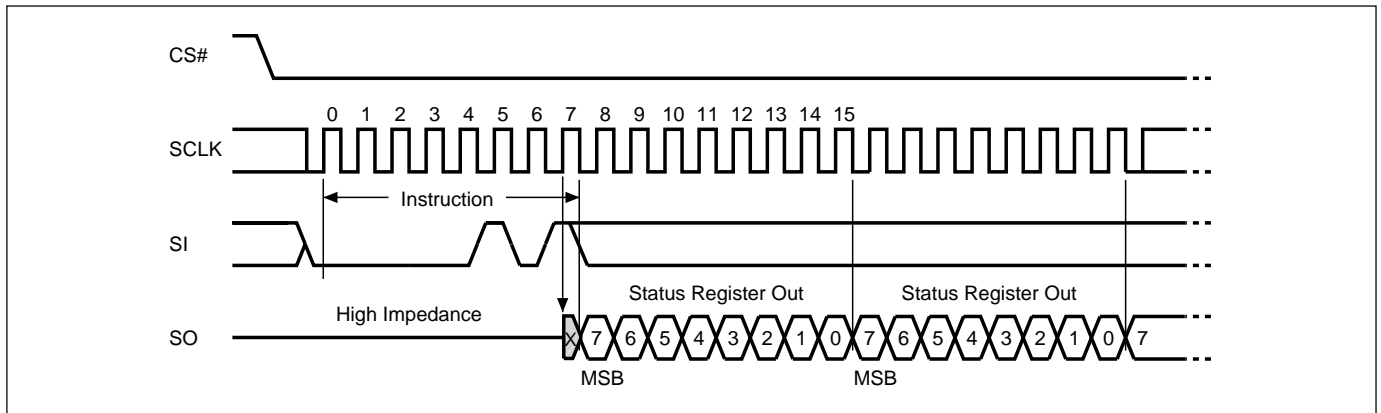
**Figure 8. Serial Input Timing**

**Figure 9. Write Protect Setup and Hold Timing during WRSR when SRWD=1**


**Figure 10. Hold Timing**

**Figure 11. Output Timing**


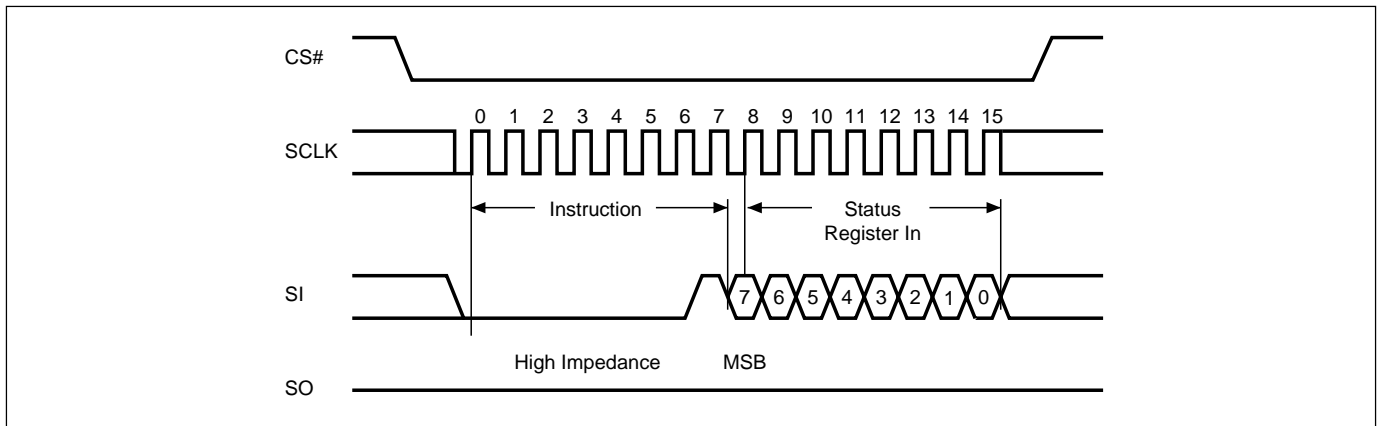
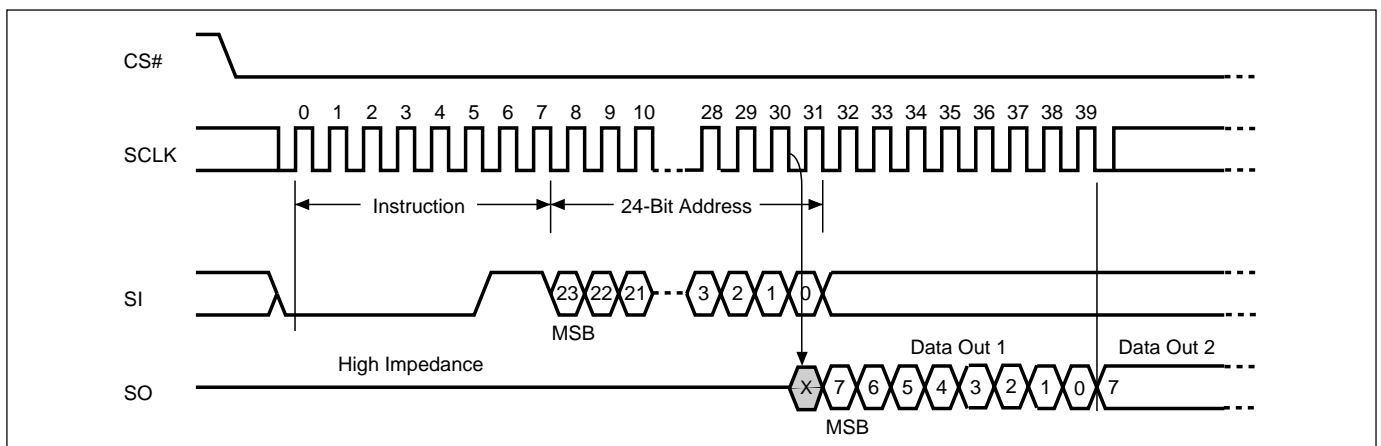


**Figure 12. Write Enable (WREN) Instruction Sequence**

**Figure 13. Write Disable (WRDI) Instruction Sequence**

**Figure 14. Read Identification (RDID) Instruction Sequence and Data-Out Sequence**


Notes: In serial RDID and RDSR mode, output pin SO will be enabled at 8th clock's rising edge. That means, MXIC's drip will enable output half a cycle in advance compare with other compatible vendor's spec.

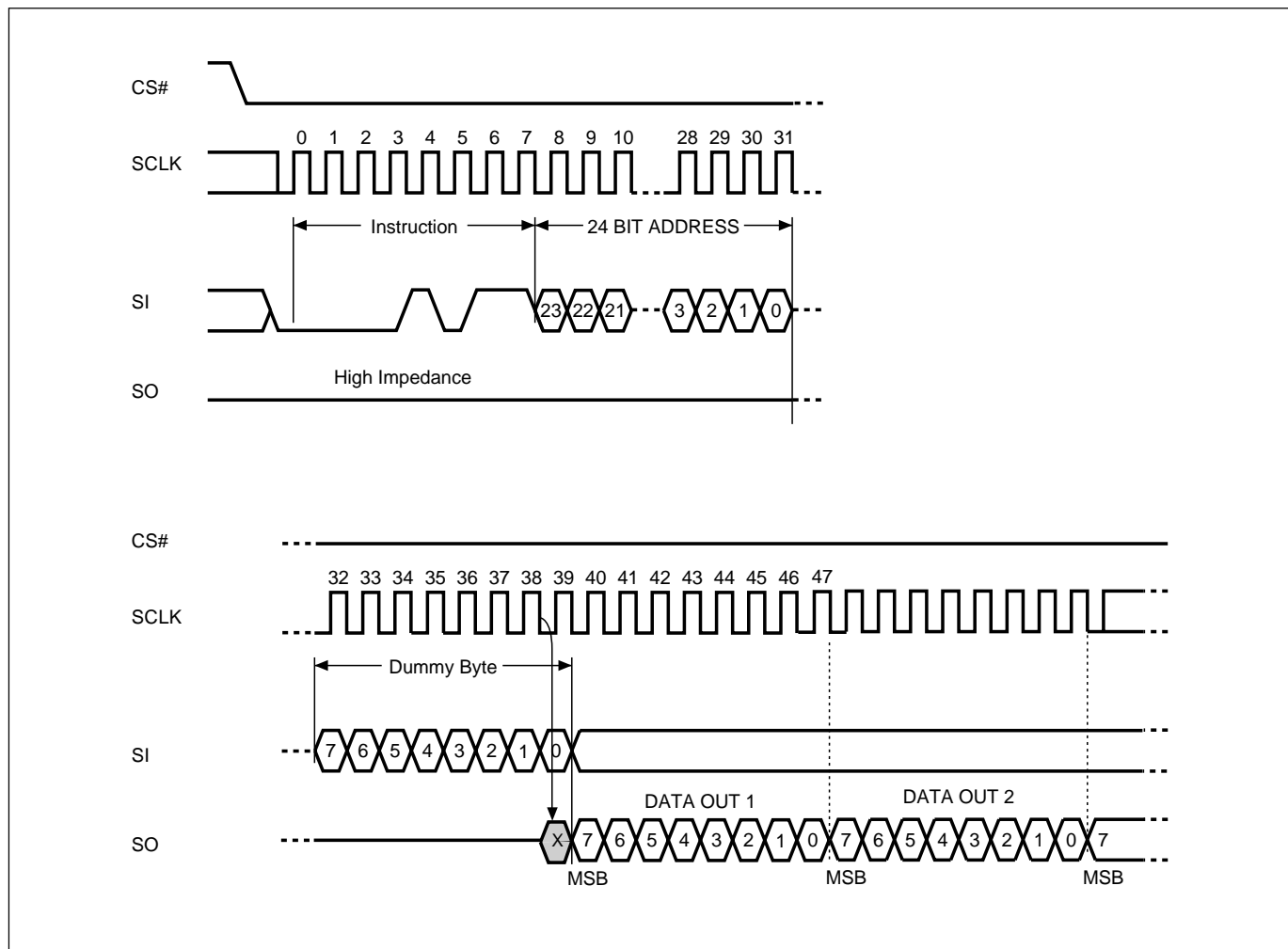
**Figure 15. Read Status Register (RDSR) Instruction Sequence and Data-Out Sequence**


Notes: In serial RDID and RDSR mode, output pin SO will be enabled at 8th clock's rising edge. That means, MXIC's drip will enable output half a cycle in advance compare with other compatible vendor's spec.

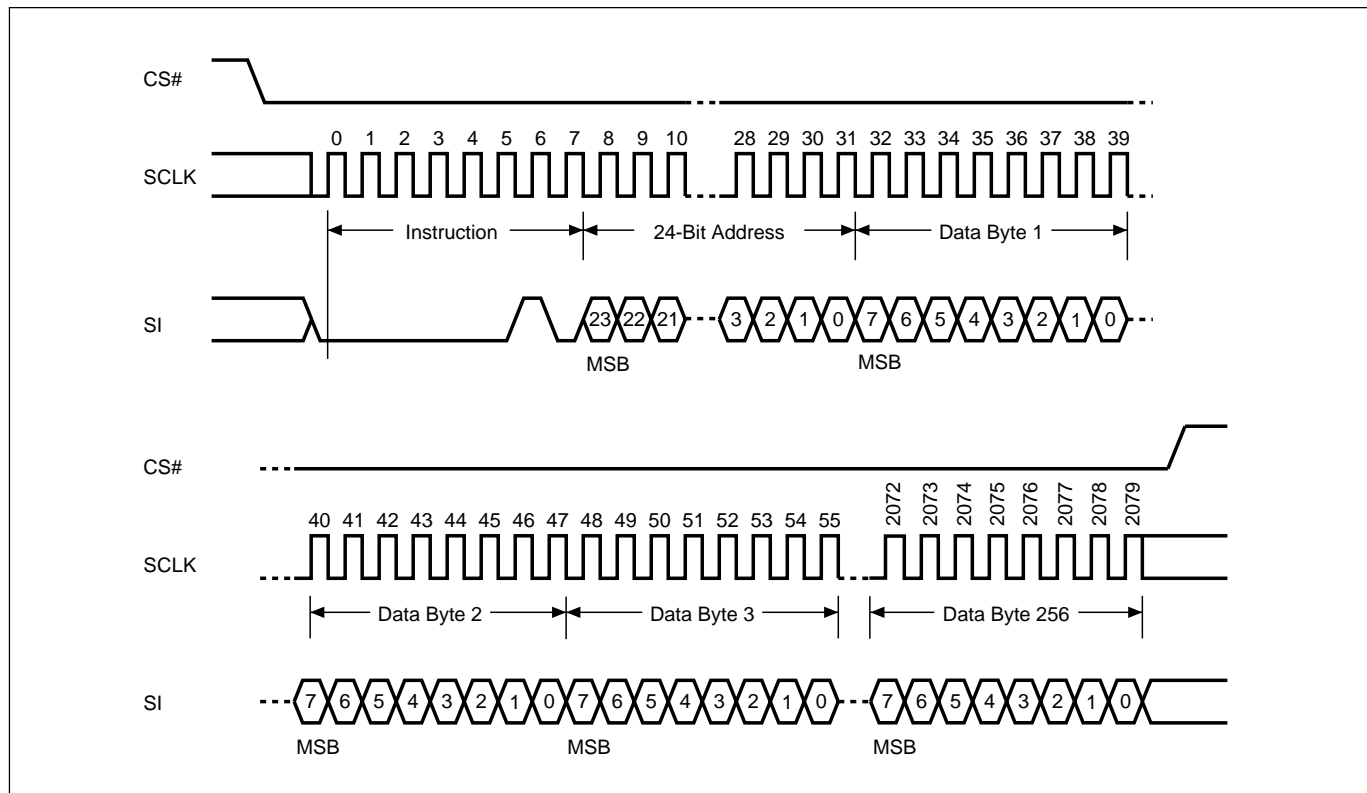
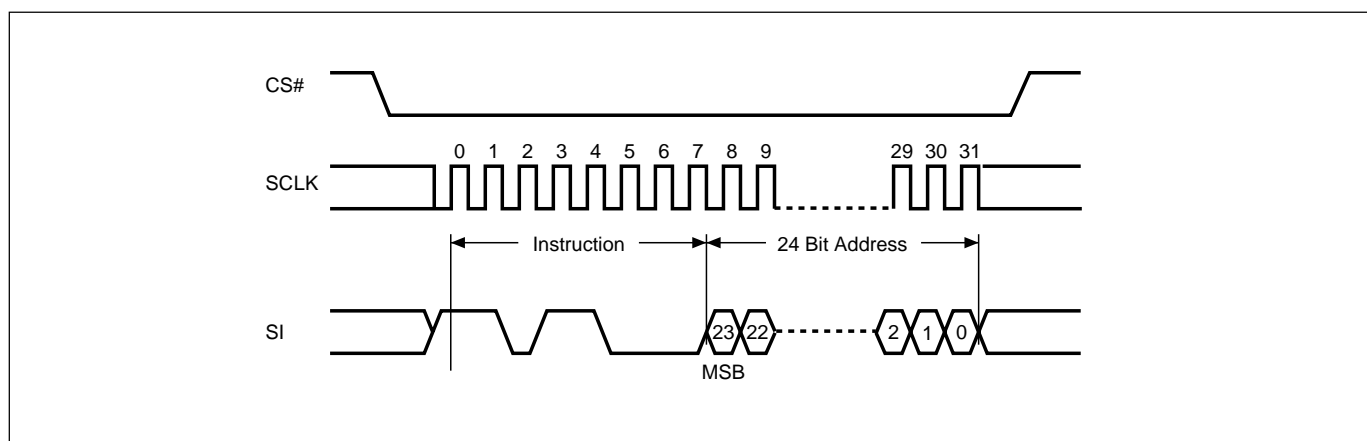
**Figure 16. Write Status Register (WRSR) Instruction Sequence**

**Figure 17. Read Data Bytes (READ) Instruction Sequence and Data-Out Sequence**


Notes: In READ mode, FAST\_READ mode, RES mode and REMS mode, MXIC IC will enable output an entire cycle in advance compare with other compatible vendor's spec. Detail condition please reference the waveform.

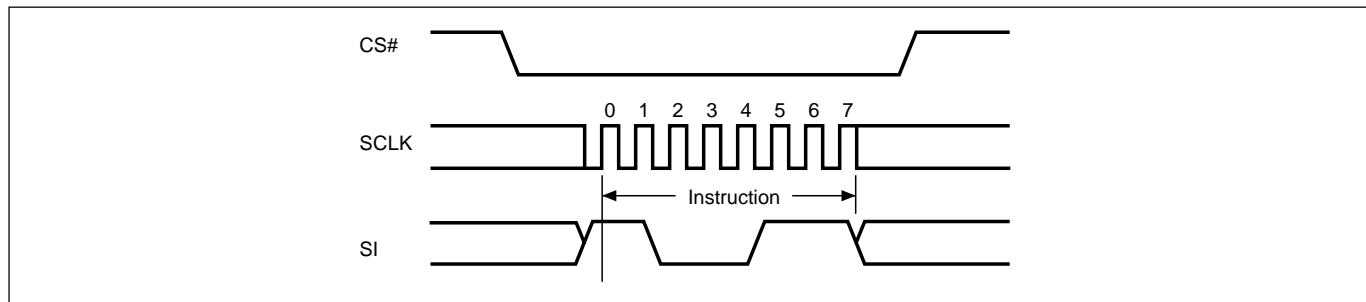
**Figure 18. Read Data Bytes at Higher Speed (FAST\_READ) Instruction Sequence and Data-Out Sequence**



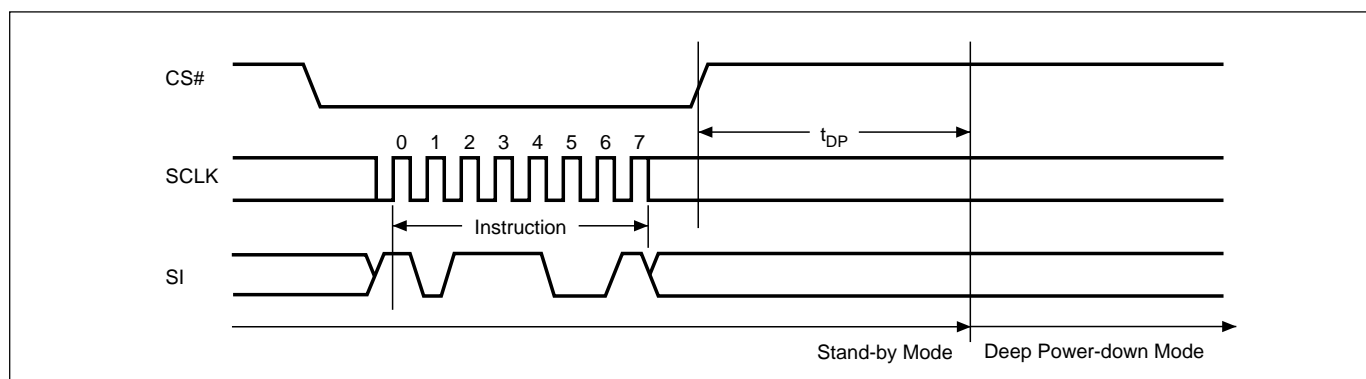
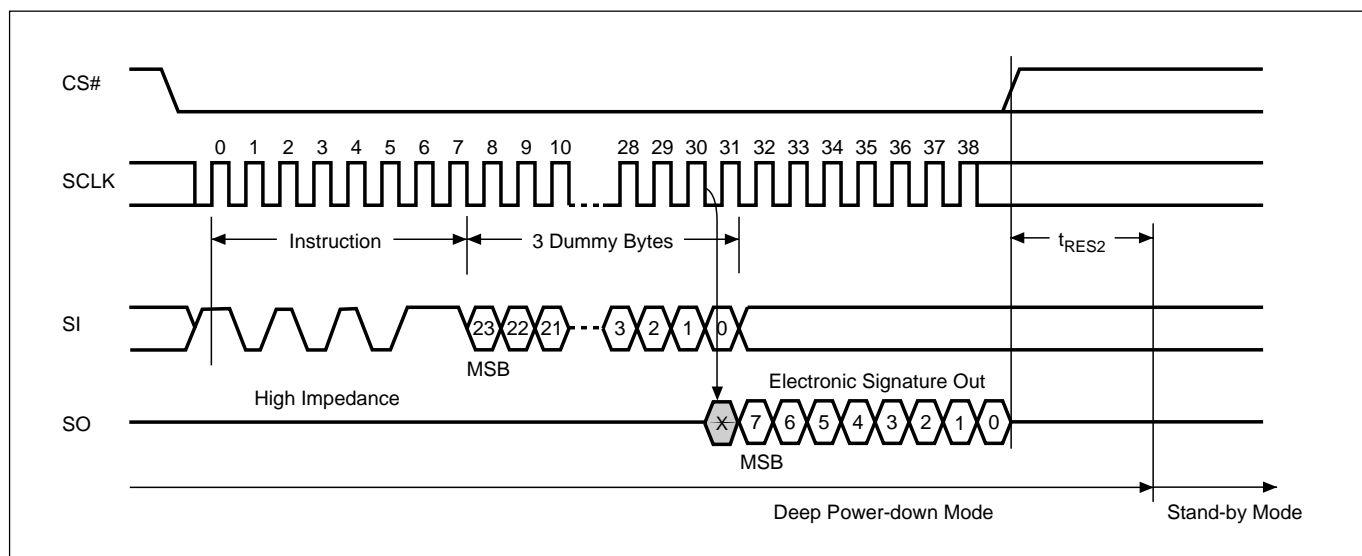
Notes: In READ mode, FAST\_READ mode, RES mode and REMS mode, MXIC IC will enable output an entire cycle in advance compare with other compatible vendor's spec. Detail condition please reference the waveform.

**Figure 19. Page Program (PP) Instruction Sequence**

**Figure 20. Sector Erase (SE) Instruction Sequence**


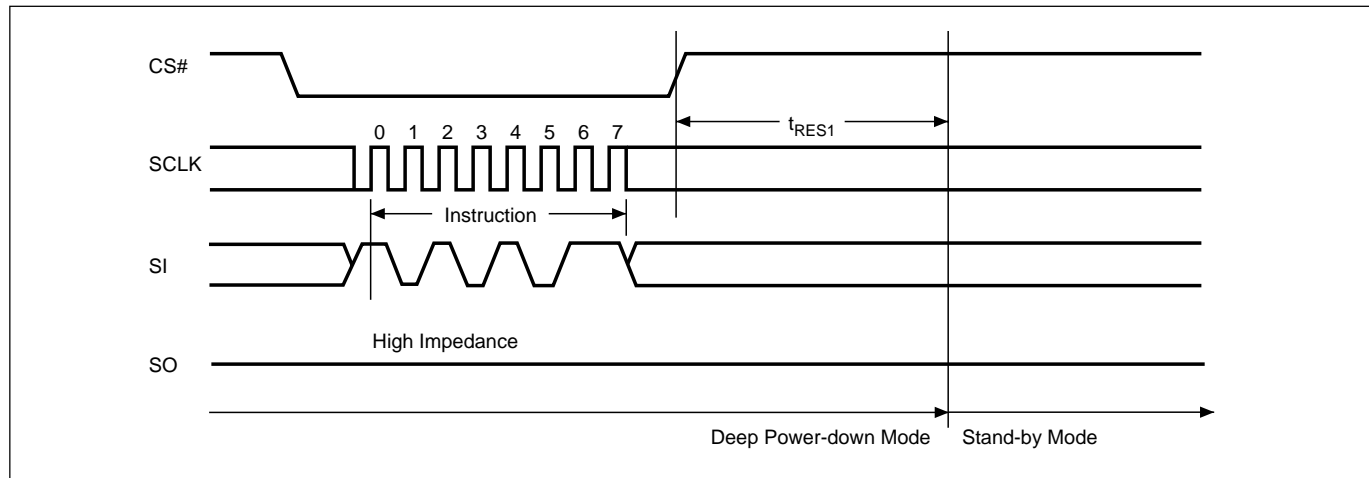
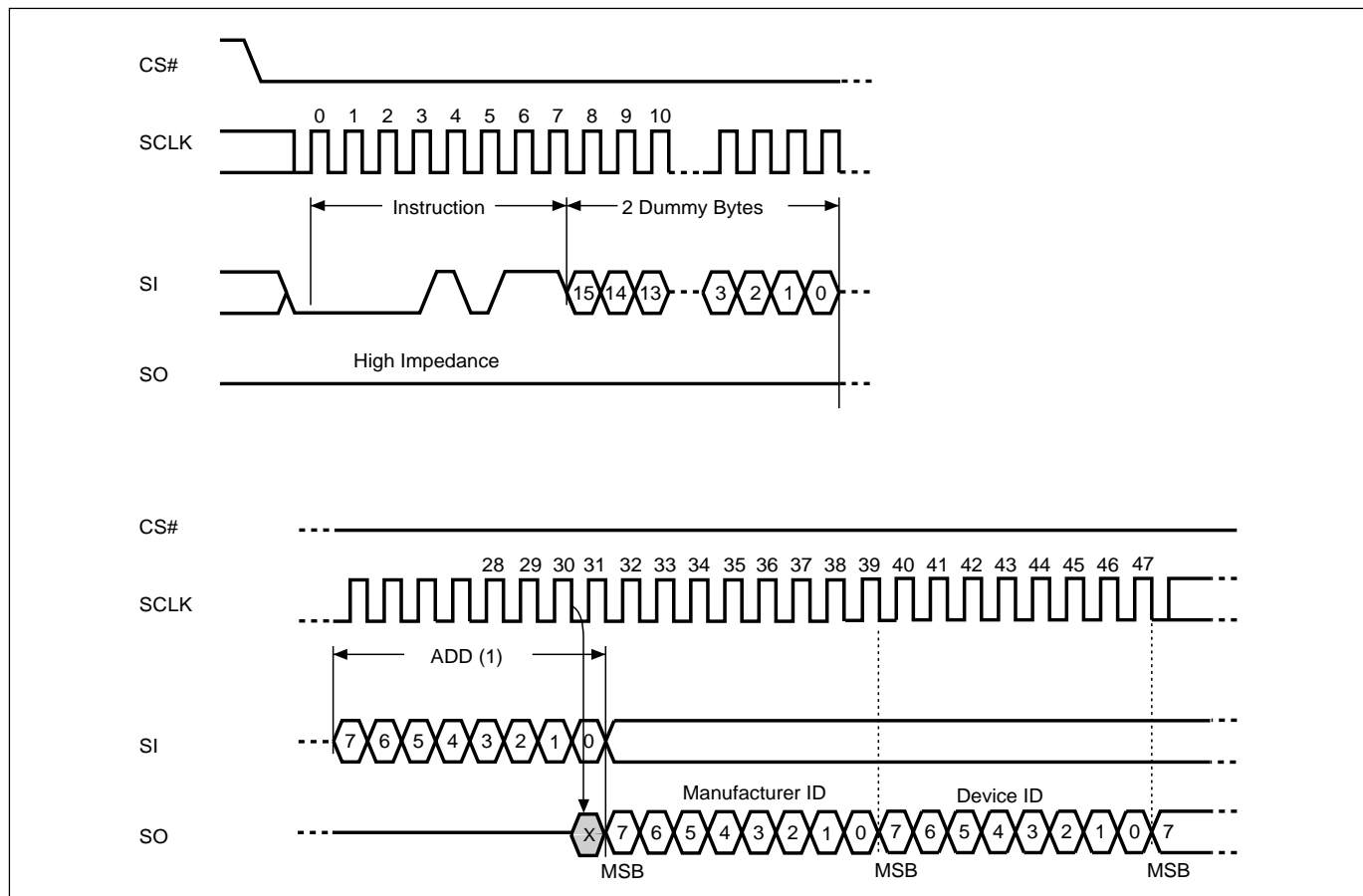
Note: SE instruction is 20(hex) or D8(hex).

**Figure 21. Chip Erase (CE) Instruction Sequence**


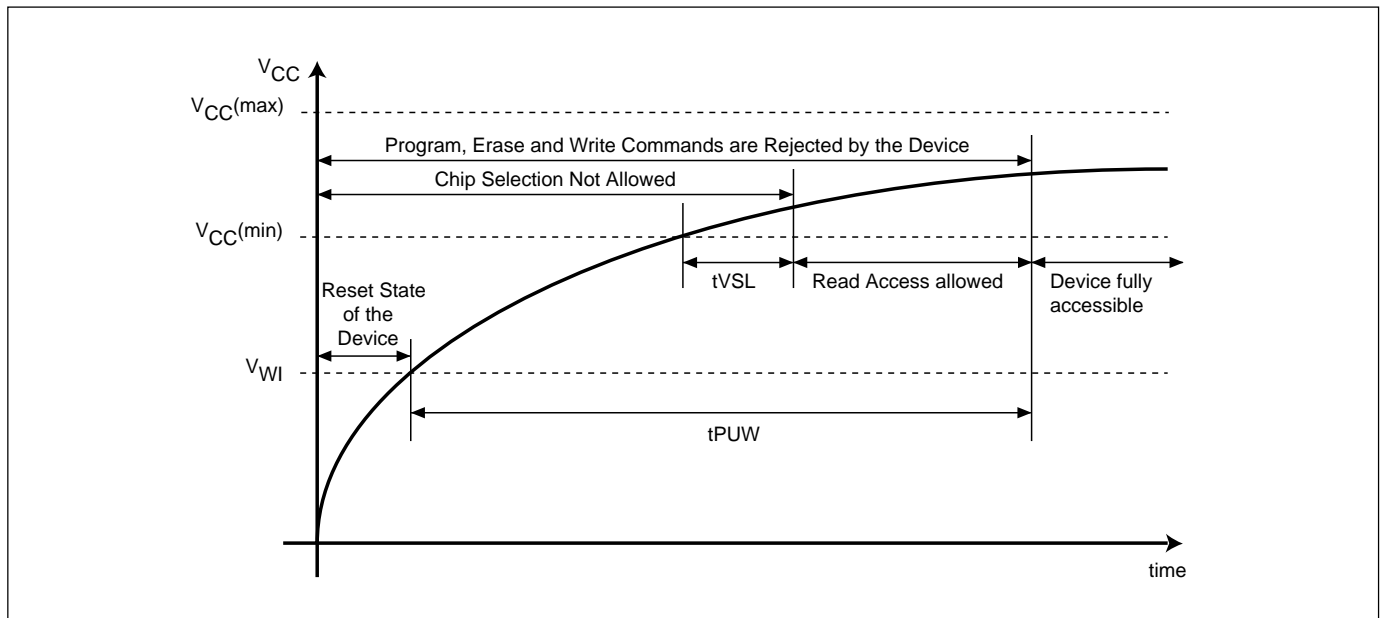
Note: CE instruction is 60(hex) or C7(hex).

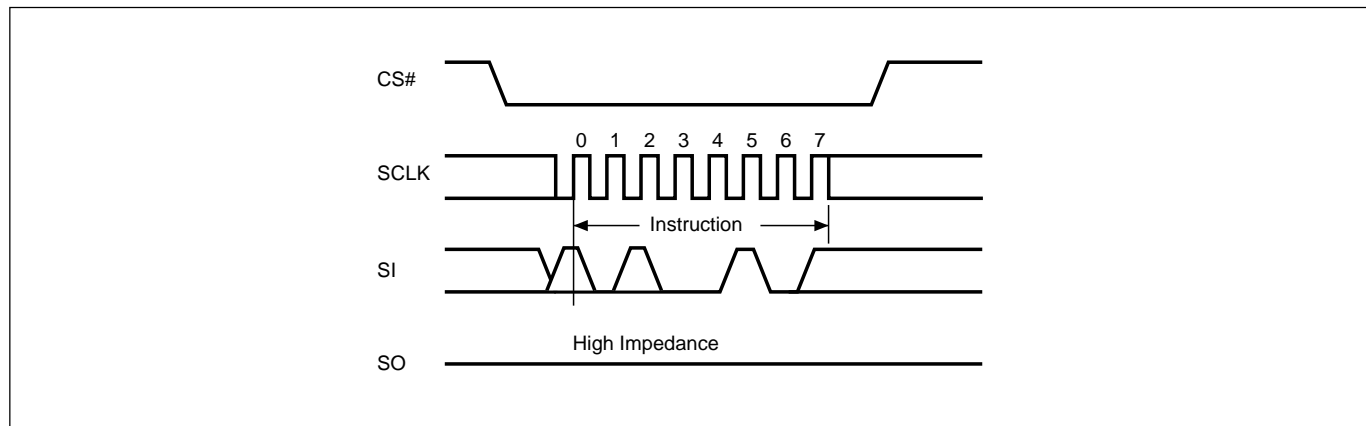
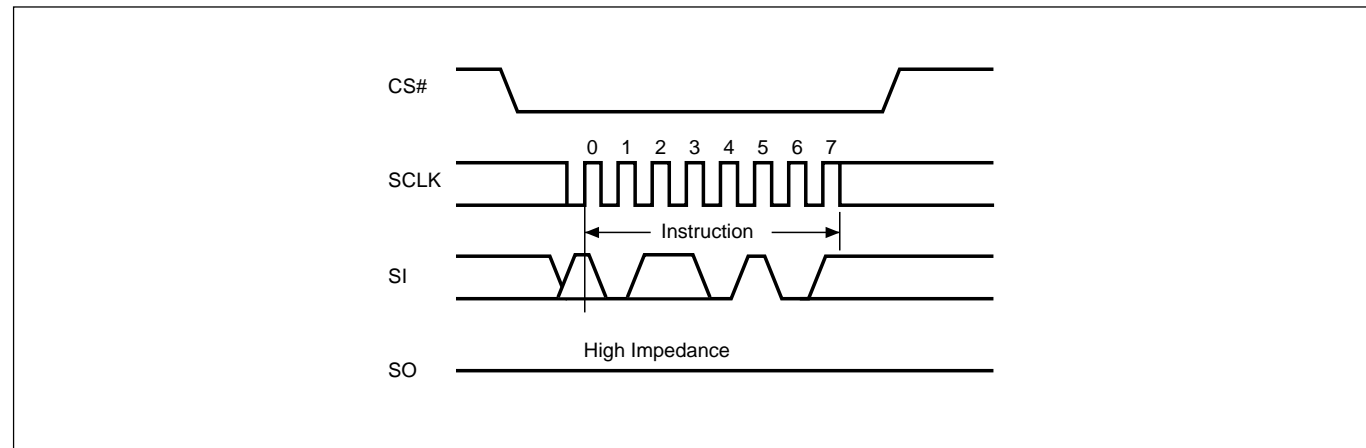
**Figure 22. Deep Power-down (DP) Instruction Sequence**

**Figure 23. Release from Deep Power-down and Read Electronic Signature (RES) Instruction Sequence and Data-Out Sequence**


Notes: In READ mode, FAST\_READ mode, RES mode and REMS mode, MXIC IC will enable output an entire cycle in advance compare with other compatible vendor's spec. Detail condition please reference the waveform.

**Figure 24. Release from Deep Power-down (RDP) Instruction Sequence**

**Figure 25. Read Electronic Manufacturer & Device ID (REMS) Instruction Sequence and Data-Out Sequence**

**Notes:**

- (1) ADD=00H will output the manufacturer's ID first and ADD=01H will output device ID first
- (2) In READ mode, FAST\_READ mode, RES mode and REMS mode, MXIC IC will enable output an entire cycle in advance compare with other compatible vendor's spec. Detail condition please reference the waveform.

**Figure 26. Power-up Timing**


**Figure 27. Enter 4Kbit Mode (EN4K) Instruction Sequence**

**Figure 28. Exit 4Kbit Mode (EX4K) Instruction Sequence**


**Note:**

Enter and Exit 4kbit mode (EN4K & EX4K)

EN4K and EX4K will not be executed when the chip is in busy state. Enter 4kbit mode then the read and write command will be executed on this 4kbit. All read and write command sequence is the same as the normal array. The address of this 4k bits is: A20~A9=0 and A8~A0 customer defined.

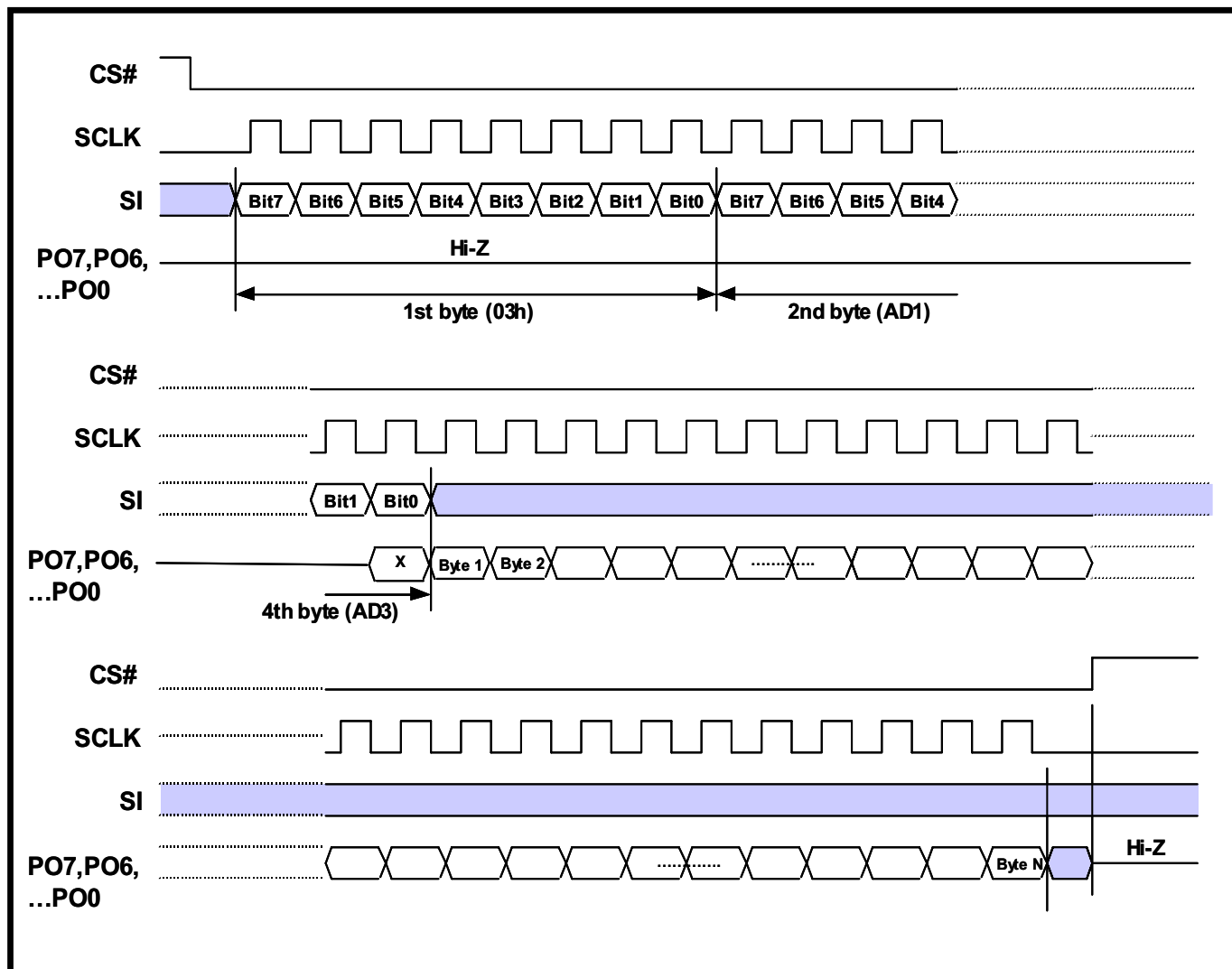
Note 1: Chip erase and WRSR will not be executed in 4kbit mode

Note 2: Chip erase can't erase this 4kbit

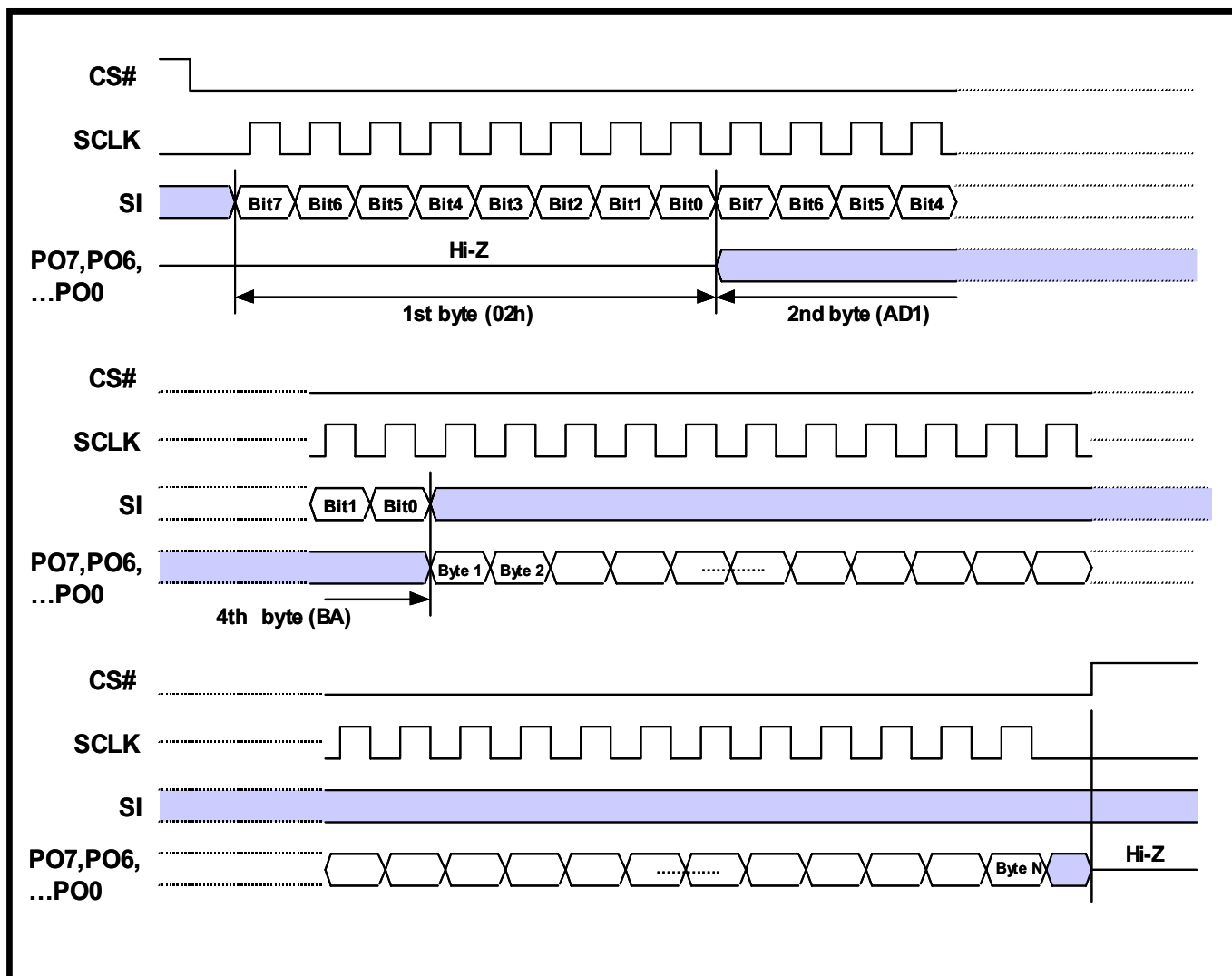
**About the fail status:**

Bit6 of the status register is used to state fail status, bit6=1 means program or erase have been failed. Any new write command will clear this bit.

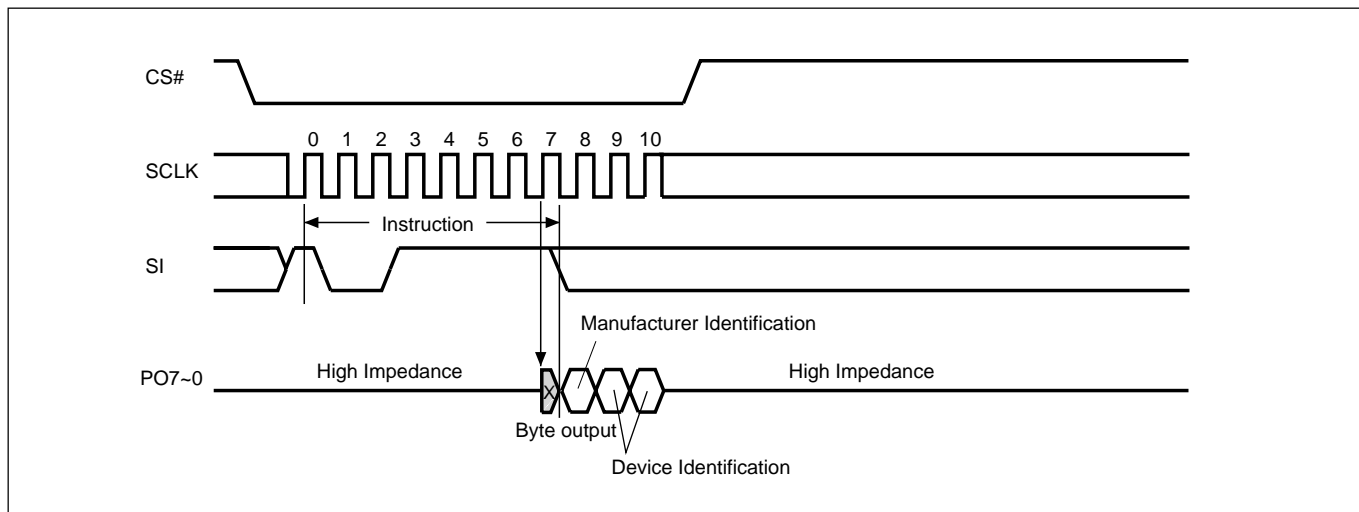


**Figure 29. READ ARRAY WAVEFORM (Parallel)**

**NOTES:**

1. 1st Byte='03h'
2. 2nd Byte=Address 1(AD1), AD23=BIT7, AD22=BIT6, AD21=BIT5, AD20=BIT4,....AD16=BIT0.
3. 3rd Byte=Address 2(AD2), AD15=BIT7, AD14=BIT6, AD13=BIT5, AD12=BIT4,....AD8=BIT0.
4. 4th Byte=Address 3(AD3), AD7=BIT7, AD6=BIT6, ....AD0=BIT0.
5. From Byte 5, SO Would Output Array Data.
6. Under parallel mode, the fastest access clock freq. will be changed to 1.2MHz(SCLK pin clock freq.).
7. To read array in parallel mode requires a parallel mode command (55H) before the read command.  
Once in the parallel mode, eLiteFlash™ Memory will not exit parallel mode until power-off.
8. In READ mode, RES mode and REMS mode, MXIC IC will enable output an entire cycle in advance compare with other compatible vendor's spec.

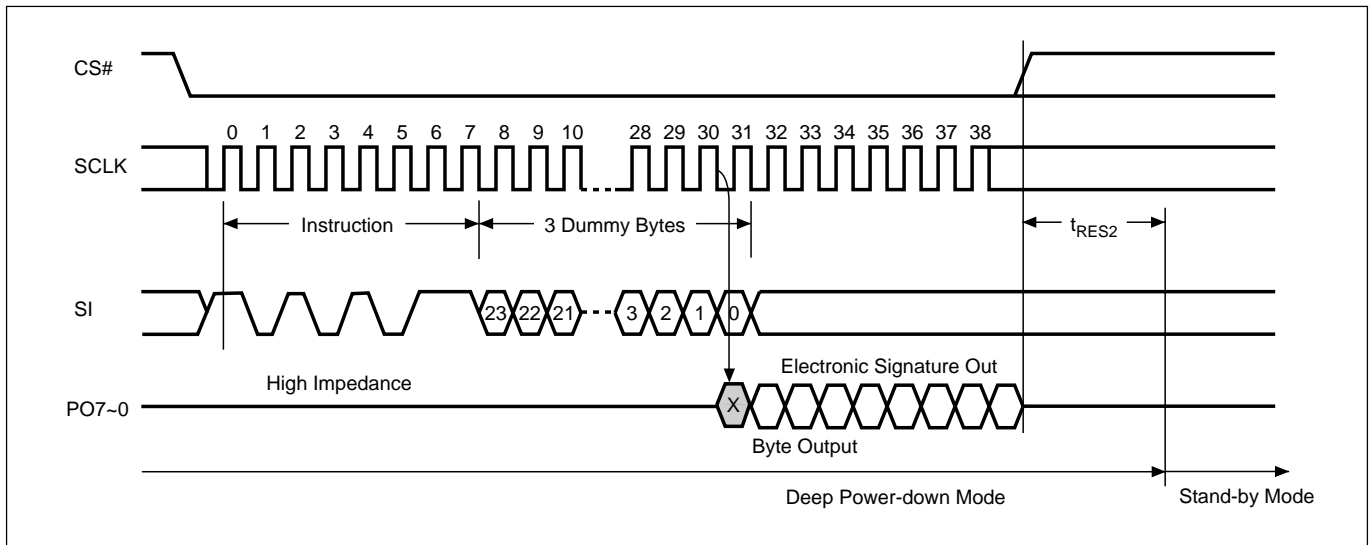
**Figure 30. AUTO PAGE PROGRAM TIMING WAVEFORM (Parallel)**

**NOTES:**

1. 1st Byte='02h'
2. 2nd Byte=Address 1(AD1), AD23=BIT7, AD22=BIT6, AD21=BIT5, AD20=BIT4,....AD16=BIT0.
3. 3rd Byte=Address 2(AD2), AD15=BIT7, AD14=BIT6, AD13=BIT5, AD12=BIT4,....AD8=BIT0.
4. 4th Byte=Address 3(AD3), AD7=BIT7, AD6=BIT6, ....AD0=BIT0.
5. 5th byte: 1st write data byte.
6. Under parallel mode, the fastest access clock freq. will be changed to 1.2MHz(SCLK pin clock freq.).
7. To program in parallel mode requires a parallel mode command (55H) before the program command.  
Once in the parallel mode, eLiteFlash™ Memory will not exit parallel mode until power-off.

**Figure 31. Read Identification (RDID) Instruction Sequence and Data-Out Sequence (Parallel)**

**NOTES:**

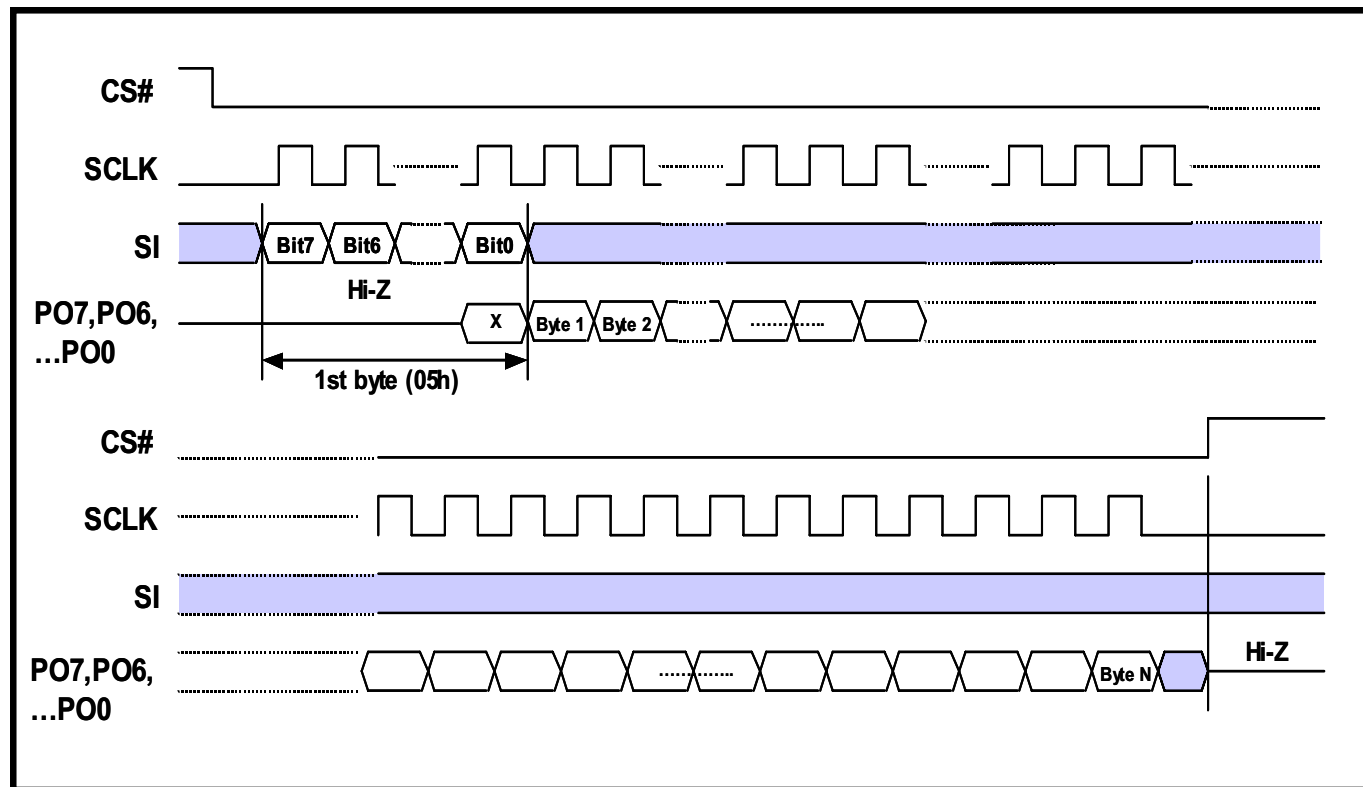
- Under parallel mode, the fastest access clock freq. will be changed to 1.2MHz(SCLK pin clock freq.)  
To read identification in parallel mode, which requires a parallel mode command (55H) before the read identification command.  
Once in the parallel mode, eLiteFlash™ Memory will not exit parallel mode until power-off.
- Only 1~3 bytes would be output for manufacturer and Device ID. It's same for serial RDID mode.
- In serial RDID and RDSR mode, output pin SO will be enabled at 8th clock's rising edge. That means, MXIC's drip will enable output half a cycle in advance compare with other compatible vendor's spec.

**Figure 32. Release from Deep Power-down and Read Electronic Signature (RES) Instruction Sequence and Data-Out Sequence (Parallel)**



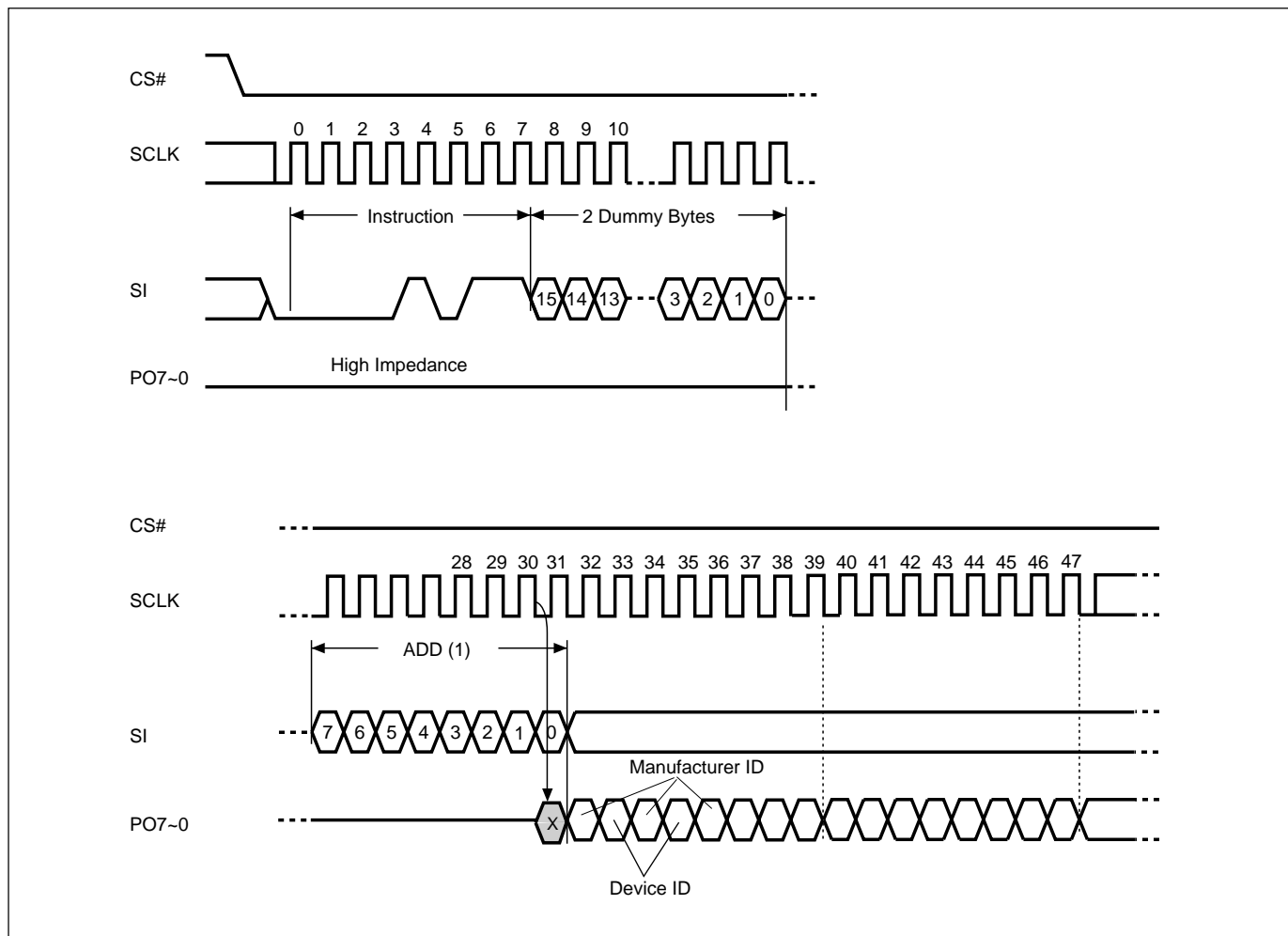
**NOTES:**

1. Under parallel mode, the fastest access clock freq. will be changed to 1.2MHz(SCLK pin clock freq.)  
To release from deep power-down mode and read ID in parallel mode, which requires a parallel mode command (55H) before the read status register command.  
Once in the parallel mode, eLiteFlash™ Memory will not exit parallel mode until power-off.
2. In READ mode, RES mode and REMS mode, MXIC IC will enable output an entire cycle in advance compare with other compatible vendor's spec.

**Figure 33. READ STATUS REGISTER TIMING WAVEFORM (Parallel)**

**NOTES:**

1. 1st Byte='05h'
2. BIT7 status register write disable signal. BIT7=1, means SR write disable.
3. BIT6=0 ==> Program/erase is correct.
4. BIT4, 3, 2 defines the level of protected block. (BIT 5 is not used)
5. BIT1 write enable latch
6. BIT0=0 ==> Device is in ready state
7. Under parallel mode, the fastest access clock freq. will be changed to 1.2MHz(SCLK pin clock freq.).  
To read status register in parallel mode requires a parallel mode command (55H) before the read status register command.  
Once in the parallel mode, eLiteFlash™ Memory will not exit parallel mode until power-off.
8. In serial RDID and RDSR mode, output pin SO will be enabled at 8th clock's rising edge. That means, MXIC's drip will enable output half a cycle in advance compare with other compatible vendor's spec.

**Figure 34. Read Electronic Manufacturer & Device ID (REMS) Instruction Sequence and Data-Out Sequence (Parallel)**



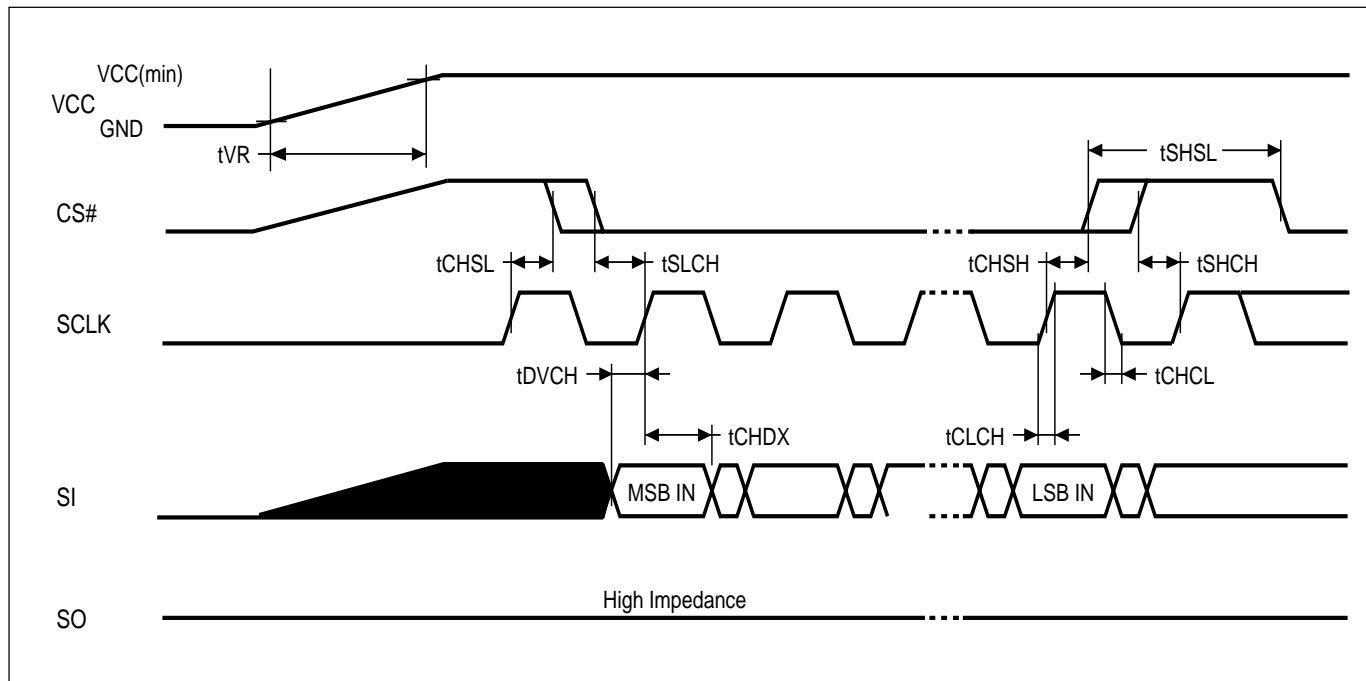
**NOTES:**

- (1) ADD=00H will output the manufacturer's ID first and ADD=01H will output device ID first
- (2) Under parallel mode, the fastest access clock freq. will be changed to 1.2MHz(SCLK pin clock freq.)  
To read ID in parallel mode, which requires a parallel mode command (55H) before the read ID command.  
Once in the parallel mode, eLiteFlash™ Memory will not exit parallel mode until power-off.
- (3) In READ mode, RES mode and REMS mode, MXIC IC will enable output an entire cycle in advance compare with other compatible vendor's spec.

## RECOMMENDED OPERATING CONDITIONS

### At Device Power-Up

AC timing illustrated in Figure A is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.



**Figure A. AC Timing at Device Power-Up**

| Symbol | Parameter     | Notes | Min. | Max.   | Unit |
|--------|---------------|-------|------|--------|------|
| tVR    | VCC Rise Time | 1     | 0.5  | 500000 | us/V |

#### Notes :

1. Sampled, not 100% tested.
2. For AC spec tCHSL, tSLCH, tDVCH, tCHDX, tSHSL, tCHSH, tSHCH, tCHCL, tCLCH in the figure, please refer to "AC CHARACTERISTICS" table.

**ERASE AND PROGRAMMING PERFORMANCE**

| PARAMETER                               |                | Min. | TYP. (1) | Max. (2) | UNIT   | Comments                          |
|---|----------------|------|----------|----------|--------|-----------------------------------|
| Chip Erase Time                         |                |      | 32       | 64       | s      |                                   |
| Chip Erase Time<br>(with ACC=12V)       |                |      | 25       | 52       | s      | Note (4)                          |
| Sector erase Time                       |                |      | 1        | 3        | s      | Note (4)                          |
| Sector erase Time<br>(with ACC=12V)     |                |      | 0.8      | 2.4      | s      | Note (4)                          |
| Additional 4Kb Erase Time               |                |      | 25       | 50       | mS     | Note (4)                          |
| Page Programming Time                   |                |      | 3        | 12       | mS     | Excludes system level overhead(3) |
| Page Programming Time<br>(with ACC=12V) |                |      | 2.4      | 9.6      | mS     |                                   |
| Erase/Program<br>Cycle                  | Main Array     | 10K  |          |          | cycles |                                   |
|   | Additional 4Kb | 100K |          |          | cycles |                                   |

Note:

1. Typical program and erase time assumes the following conditions: 25°C, 3.0V, and all bits are programmed by checker-board pattern.
2. Under worst conditions of 70°C and 3.0V. Maximum values are up to including 10K program/erase cycles.
3. System-level overhead is the time required to execute the command sequences for the page program command.
4. Excludes 00H programming prior to erasure. (In the pre-programming step of the embedded erase algorithm, all bits are programmed to 00H before erasure)

**LATCH-UP CHARACTERISTICS**

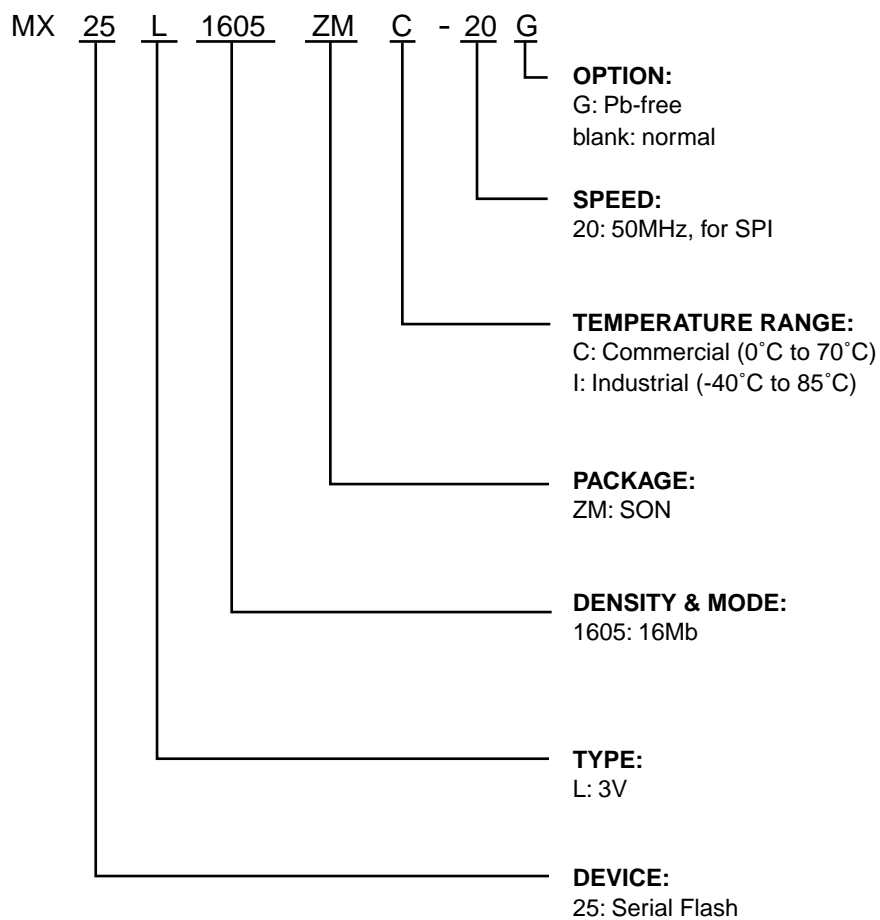
|   | MIN.   | MAX.       |
|---|--------|------------|
| Input Voltage with respect to GND on ACC                                      | -1.0V  | 12.5V      |
| Input Voltage with respect to GND on all power pins, SI, CS#                  | -1.0V  | 2 VCCmax   |
| Input Voltage with respect to GND on SO                                       | -1.0V  | VCC + 1.0V |
| Current   | -100mA | +100mA     |
| Includes all pins except VCC. Test conditions: VCC = 3.0V, one pin at a time. |        |            |

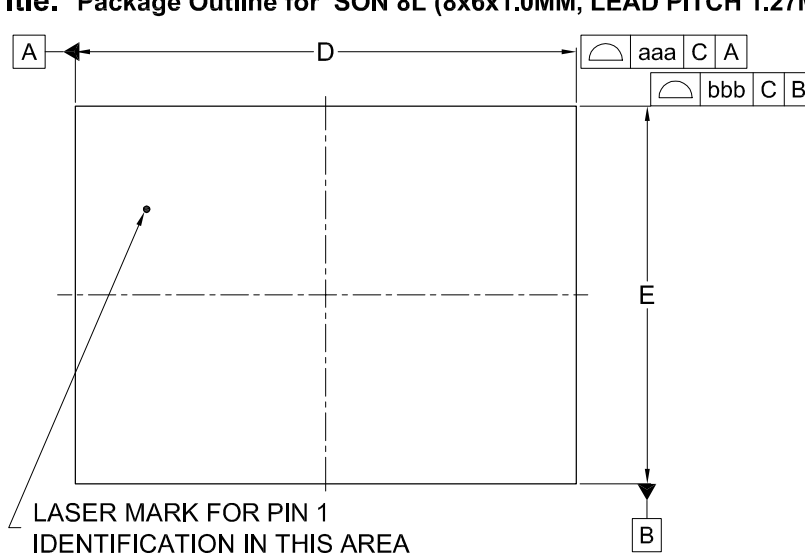
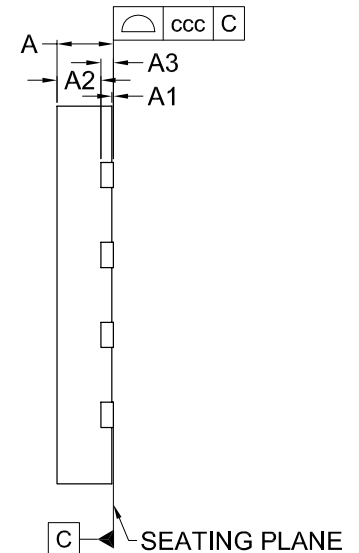
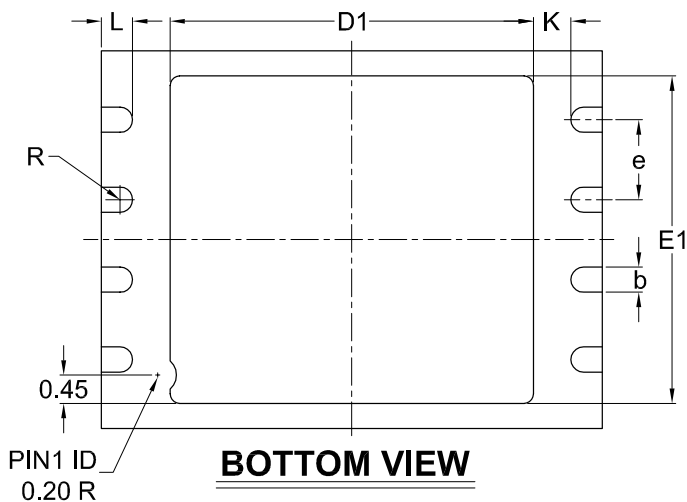


**ORDERING INFORMATION**

| PART NO.         | ACCESS<br>TIME(ns) | OPERATING<br>CURRENT(mA) | STANDBY<br>CURRENT(uA) | Temperature | PACKAGE    | Remark  |
|------------------|--------------------|--------------------------|------------------------|-------------|------------|---------|
| MX25L1605ZMC-20G | 20                 | 30                       | 50                     | 0~70°C      | 8-land SON | Pb-free |
| MX25L1605ZMI-20G | 20                 | 30                       | 50                     | -40~85°C    | 8-land SON | Pb-free |

### PART NAME DESCRIPTION



**PACKAGE INFORMATION**
**Title: Package Outline for SON 8L (8x6x1.0MM, LEAD PITCH 1.27MM)**

**TOP VIEW**

**SIDE VIEW**

**BOTTOM VIEW**

Dimensions (inch dimensions are derived from the original mm dimensions)

\*1 : The exposed pad size must not violate the minimum metal separation requirement (K).

| SYMBOL |      | A     | A1    | A2    | A3    | b     | D     | D1    | E     | E1    | L     | e    | R     | K     | aaa   | bbb   | ccc   |
|--------|------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|------|-------|-------|-------|-------|-------|
| UNIT   |      |       |       |       |       |       |       |       |       |       |       |      |       |       |       |       |       |
| mm     | Min. | ---   | ---   | ---   | ---   | 0.35  | 7.90  | 0.00  | 5.90  | 0.00  | 0.45  | ---  | 0.165 | 0.20  | ---   | ---   | ---   |
|        | Nom. | ---   | ---   | 0.65  | 0.20  | 0.40  | 8.00  | *1    | 6.00  | *1    | 0.50  | 1.27 | ---   | ---   | 0.10  | 0.10  | 0.05  |
|        | Max. | 1.00  | 0.05  | 0.70  | ---   | 0.48  | 8.10  |       | 6.10  |       | 0.60  | ---  | ---   | ---   | ---   | ---   | ---   |
| Inch   | Min. | ---   | ---   | ---   | ---   | 0.014 | 0.311 | 0.000 | 0.232 | 0.000 | 0.018 | ---  | 0.006 | 0.008 | ---   | ---   | ---   |
|        | Nom. | ---   | ---   | 0.026 | 0.008 | 0.016 | 0.315 | *1    | 0.236 | *1    | 0.020 | 0.05 | ---   | ---   | 0.004 | 0.004 | 0.002 |
|        | Max. | 0.039 | 0.002 | 0.028 | ---   | 0.019 | 0.319 |       | 0.240 |       | 0.024 | ---  | ---   | ---   | ---   | ---   | ---   |

| DWG.NO.   | REVISION | REFERENCE |      |  | ISSUE DATE |
|-----------|----------|-----------|------|--|------------|
|           |          | JEDEC     | EIAJ |  |            |
| 6110-3301 | 6        | MO-220    |      |  | 05-30-'05  |



**MX25L1605ZM**

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