

**64M-BIT [4Mx16] CMOS SINGLE VOLTAGE
1.8V ONLY FLASH MEMORY****FEATURES**

- **Architecture**
 - Bit Organization: 4,194,304 x 16
 - Multiple 4Mb partitions
 - RWW (Read While Write) or RWE (Read While Erase)
 - Sector Erase (Sector structure : 4Kword x 8 (parameter sectors), 32Kword x 127 (main sectors))
 - Top/Bottom Boot
- **Single power supply operation**
 - VCC=1.65V to 1.95V only operation for read, erase and program operation
 - V_{pp} =12 V fast production programming (12us/word, typical)
 - 1.7V~2.24V for I/O Option (V_{CCQ})
- **High performance**
 - Fast access time : 70/85 ns
 - 14ns Synchronous Burst Mode
 - 25ns Page Mode Read
 - 4-, 8-, 16-, and continuous Word Burst Modes
 - Burst and Page Modes in both parameter and main partitions
 - 12us/word @ 1.8V programming
 - Burst suspend feature
 - Enhanced factory programming @3.1 us/word (typ.)
- **Low power consumption**
 - 7mA typical read current @40/54MHz 4-Word syn. read
 - 6mA maximum active read current, f=13MHz (CMOS input)
 - 21mA program erase current maximum (V_{pp} =0.9~1.95V)
 - 5uA typical standby current
- **Software Control**
 - Detection of program and erase operation completion.
 - Command User Interface (CUI)
 - Status Register (SR)
 - Word program suspend to read
 - Sector erase suspend to program or read
 - Common Flash Interface (CFI)
- **Security Feature**
 - Include parameter sectors and main sectors to be lock/unlock
 - 128-bit Protection Register
 - 64-bit Unique Device Identifier
 - 64-bit User-Programmable
 - Hardware write protection if $V_{pp} < V_{PPLK}$
- **Reliability and Package type**
 - Operating temperature :- 40°C~85°C
 - 100,000 minimum erase/program cycles
 - Latch-up protected to 100mA from -1V to VCC+1V
 - 56-ball CSP (8mm x 10mm)

GENERAL DESCRIPTION

The MX28F640W18T/B is a 64-mega bit Flash memory organized as 4M words of 16 bits. The 1M word of data is arranged in eight 4Kword parameter sectors, and 127 32Kword main sectors which are individually erasable. MXIC's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The MX28F640W18T/B is packaged in 56-ball CSP. It is designed to be reprogrammed and erased in system or in standard EPROM programmers.

The standard MX28F640W18T/B offers initial access speed as fast as 70ns, allowing operation of high-speed microprocessors without wait states.

MXIC's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The MX28F640W18T/B uses a command register to manage this functionality. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

MXIC Flash technology reliably stores memory contents even after 100,000 erase and program cycles. The MXIC cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and program operations produces reliable cycling. The MX28F640W18T/B uses a 1.65V~1.95V VCC supply to perform the High Reliability Erase and auto Program/Erase algorithms.

The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamps on address and data pin from -1V to VCC + 1V.

The dedicated VPP pin gives complete data protection when $VPP < VPPLK$.

A Command User Interface (CUI) serves as the interface between the system processor and internal operation of the device. A valid command sequence written to the CUI initiates device automation. An internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for erase, full chip erase, word write and sector lock/unlock configuration operations.

A sector erase operation erases one of the device's 32K-word sectors typically within 0.7s, 4K-word sectors typically within 0.3s independent of other sectors. Each sector can be independently erased minimum 100,000 times. Sector erase suspend mode allows system software to suspend sector erase to read or write data from any other sector.

Writing memory data is performed in word increments of the device's 32K-word sectors typically within 0.4s and 4K-word sectors typically within 0.05s. Word program suspend mode enables the system to read data or execute code from any other memory array location.

MX28F640W18T/B features with individual sectors locking by using a combination of bits one hundred thirty-five sector lock-bits and \overline{WP} , to lock and unlock sectors.

The status register indicates when the WSM's sector erase, word program or lock configuration operation is done.

The access time is 70/85ns (tELQV) over the operating temperature range (-40°C to +80°C) and VCC supply voltage range of 1.65V~1.95V.

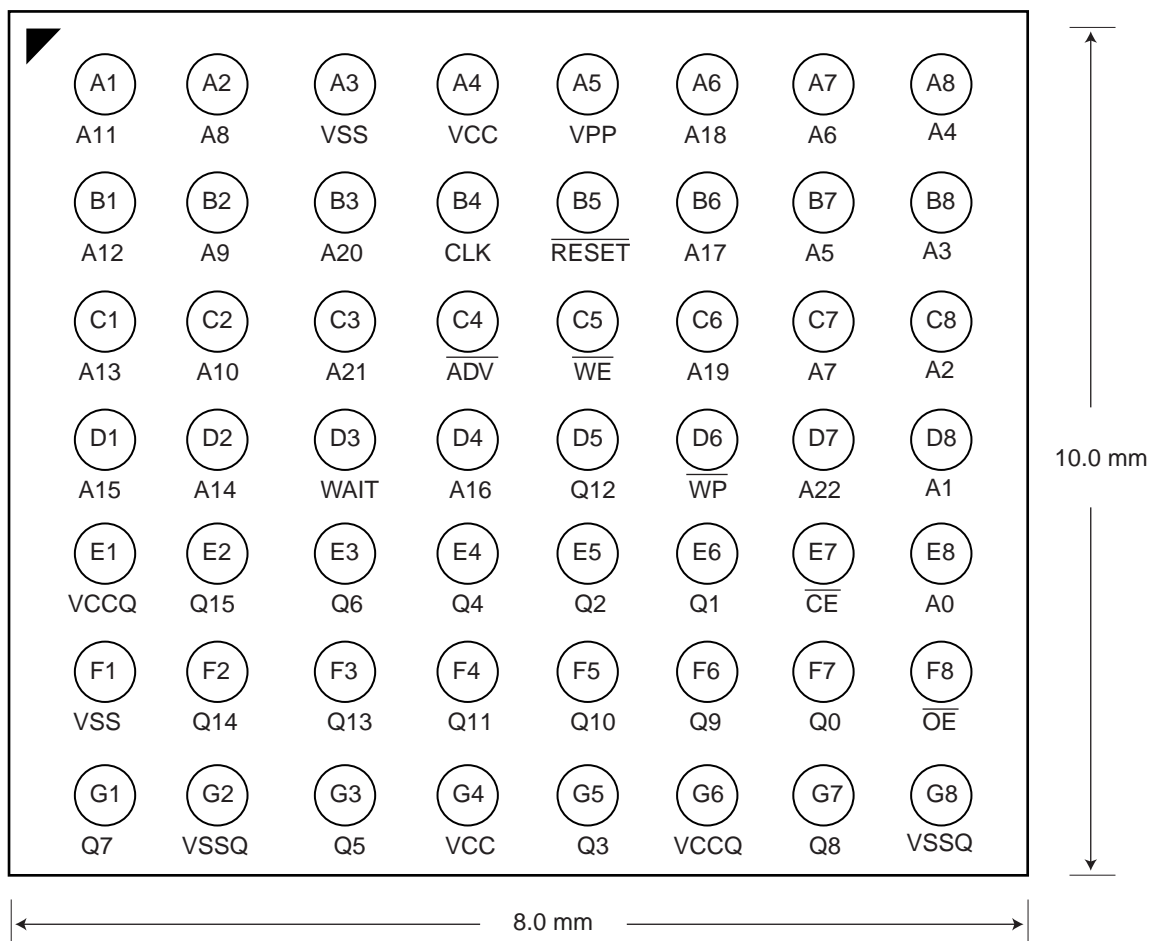
MX28F640W18T/B's power saving mode feature substantially reduces active current when the device is in static mode (addresses not switching). In this mode, the typical ICCS current is 5uA (CMOS) at 3.0V VCC Max.

As \overline{CE} and \overline{RESET} are at VCC, ICC CMOS standby mode is enabled. When \overline{RESET} is at GND, the reset mode is enabled which minimize power consumption and provide data write protection.

A reset time (tPHQV) is required from \overline{RESET} switching high until outputs are valid. Similarly, the device has a wake time (tPHEL) from \overline{RESET} -high until writes to the CUI are recognized. With \overline{RESET} at GND, the WSM is reset and the status register is cleared.

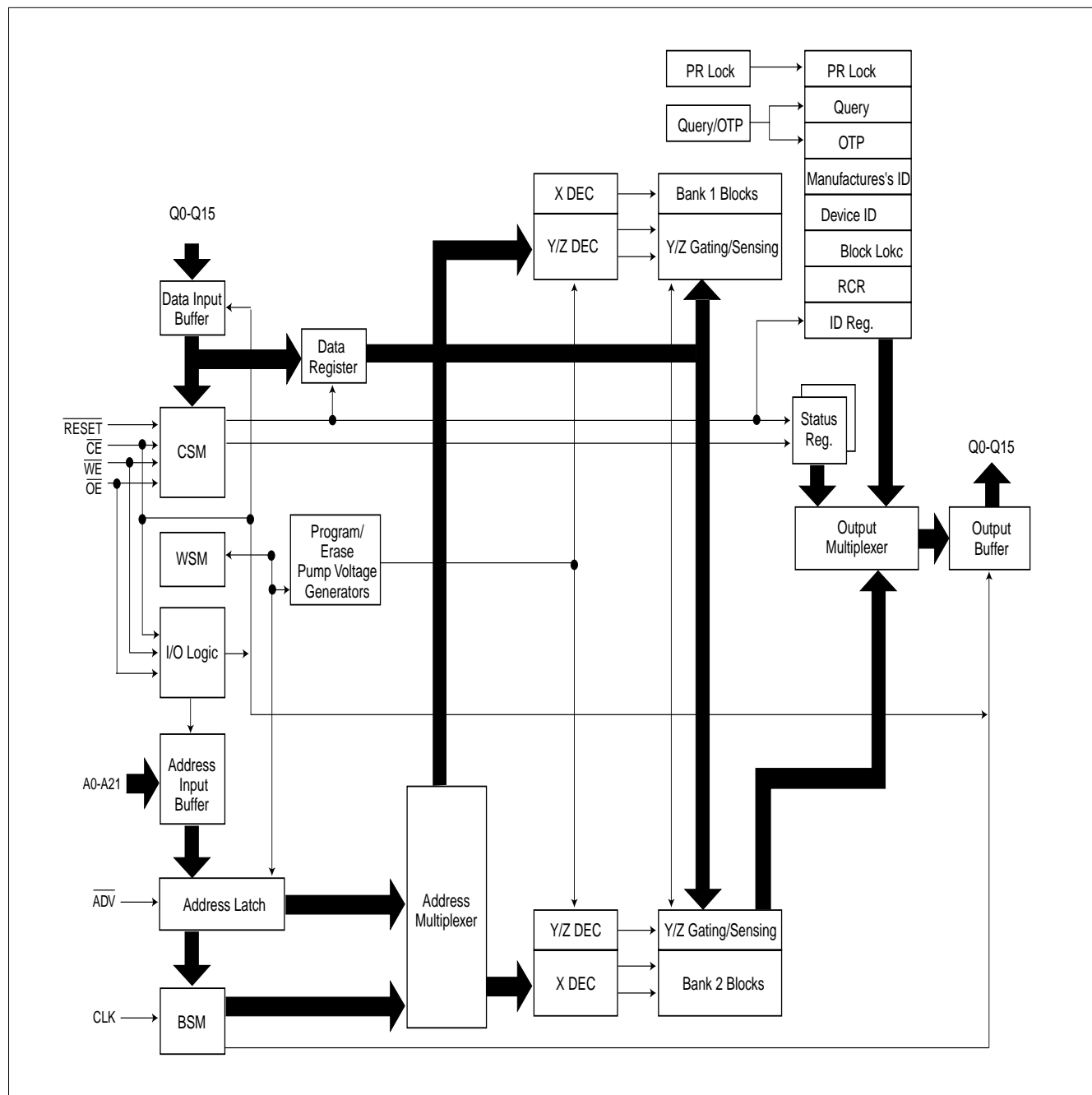
PIN CONFIGURATIONS

56 Ball CSP (8.0mm x 10.0mm) Top View, Ball Down for MX28F640W18T/BXA
(Ball Pitch=0.75mm, Ball Width=0.35mm)



Pin Description

Symbol	Type	Description and Function
A0-A22	input	Address inputs for memory address. Data pin float to high-impedance when the chip is deselected or outputs are disable. Addresses are internally latched during a write or erase cycle.
Q0-Q15	input/output	Data inputs/outputs: Inputs array data on the second \overline{CE} and \overline{WE} cycle during a program command. Data is internally latched. Outputs array and configuration data. The data pin float to tri-state when the chip is de-selected.
ADV	input	ADDRESS VALID: ADV indicates valid address presence on address presence on address inputs. During synchronous read operation, all addresses are latch on \overline{ADV} 's rising edge or CLK's rising (or falling) edge, whichever occurs first.
\overline{CE}	input	Activates the device's control logic, input buffers, and sense amplifiers. \overline{CE} high de-selects the memory device and reduce power consumption to standby level. \overline{CE} is active low.
CLK	input	CLOCK: CLK synchronizes the device to the system bus frequency in synchronous-read configuration and increments an internal burst address generator. During synchronous read operations, addresses are latched on ADV's rising edge or clk's rising (or falling) edge, whichever occurs first.
\overline{RESET}	input	Reset Deep Power Down: when \overline{RESET} =VIL, the device is in reset/deep power down mode, which drives the outputs to High Z, resets the WSM and minimizes current level. When \overline{RESET} =VIH, the device is normal operation. When \overline{RESET} transition the device defaults to the read array mode.
WAIT	output	WAIT: Indicates data valid in synchronous read modes. It is High-Z until Configuration Register bit 10 (CR.10 WT) is written, which determines its polarity when asserted. With \overline{CE} at VIL, WAIT's active output is VOL or VOH. WAIT is High-Z if \overline{CE} is VIH. WAIT is not gated by \overline{OE} .
\overline{WE}	input	Write Enable: to control write to CUI and array sector. \overline{WE} =VIL becomes active. The data and address is latched \overline{WE} on the rising edge of the second \overline{WE} pulse.
VPP	input/supply	Program/Erase Power Supply: (0.9V~1.95V or 11.4V~12.6V) Lower VPP<VPPLK, to protect any contents against Program and Erase Command. Set VPP=VCC for in-system Read, Program and Erase Operation. Raise VPP to 12V±5% for faster program and erase in a production environment.
\overline{OE}	input	Output enable: gates the device's outputs during a real cycle.
WP	input	Write protect: when WP is VIL, the boot sectors cannot be written or erased. When WP is VIH, locked boot sectors cannot be written or erase. \overline{WP} is not affected parameter and main sectors.
VCC	supply	Device power supply: (1.65V~1.95V).
VCCQ	supply	I/O Power Supply: supplies for input/output buffers.
VSS	supply	Ground voltage: all the GND pin shall not be connected.
VSSQ	supply	Output Ground: provides ground to all outputs which are driven by VCCQ. This signal may be tied directly to VSS.
DU		Don't Use: Do not use this pin. This pin should not be connected to any power supplies, signals or other pins and must be floated.

BLOCK DIAGRAM




MX28F640W18T/B

MACRONIX INTERNATIONAL Co., LTD.

HEADQUARTERS:

TEL: +886-3-578-6688

FAX: +886-3-563-2888

EUROPE OFFICE:

TEL: +32-2-456-8020

FAX: +32-2-456-8021

JAPAN OFFICE:

TEL: +81-44-246-9100

FAX: +81-44-246-9105

SINGAPORE OFFICE:

TEL: +65-348-8385

FAX: +65-348-8096

TAIPEI OFFICE:

TEL: +886-2-2509-3300

FAX: +886-2-2509-2200

MACRONIX AMERICA, INC.

TEL: +1-408-453-8088

FAX: +1-408-453-8488

CHICAGO OFFICE:

TEL: +1-847-963-1900

FAX: +1-847-963-1909

[http : //www.macronix.com](http://www.macronix.com)