



MX29F022/022NT/B

2M-BIT[256K x 8]CMOS FLASH MEMORY

FEATURES

- 262,144x 8 only
- Fast access time: 55/70/90/120ns
- Low power consumption
 - 30mA maximum active current
 - 1uA typical standby current@5MHz
- Programming and erasing voltage $5V \pm 10\%$
- Command register architecture
 - Byte Programming (7us typical)
 - Sector Erase (16K-Byte x1, 8K-Byte x 2, 32K-Byte x1, and 64K-Byte x 3)
- Auto Erase (chip & sector) and Auto Program
 - Automatically erase any combination of sectors or the whole chip with Erase Suspend capability.
 - Automatically programs and verifies data at specified address
- Erase Suspend/Erase Resume
 - Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation.
- Status Reply
 - Data polling & Toggle bit for detection of program and erase cycle completion.
- Chip protect/unprotect for 5V only system or 5V/12V system
- 100,000 minimum erase/program cycles
- Latch-up protected to 100mA from -1 to VCC+1V
- Boot Code Sector Architecture
 - T = Top Boot Sector
 - B = Bottom Boot Sector
- Hardware $\overline{\text{RESET}}$ pin
 - Resets internal state machine to read mode
- Low VCC write inhibit is equal to or less than 3.2V
- Package type:
 - 32-pin PDIP
 - 32-pin PLCC
 - 32-pin TSOP (Type 1)
- 20 years data retention

GENERAL DESCRIPTION

The MX29F022T/B is a 2-mega bit Flash memory organized as 256K bytes of 8 bits only. MXIC's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The MX29F022T/B is packaged in 32-pin PDIP, PLCC and 32-pin TSOP(I). It is designed to be reprogrammed and erased in-system or in-standard EPROM programmers.

The standard MX29F022T/B offers access time as fast as 55ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the MX29F022T/B has separate chip enable ($\overline{\text{CE}}$) and output enable ($\overline{\text{OE}}$) controls.

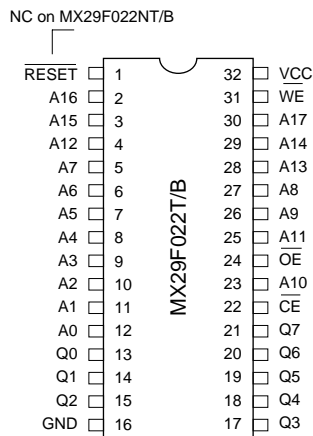
MXIC's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The MX29F022T/B uses a command register to manage this functionality. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

MXIC's Flash technology reliably stores memory contents even after 100,000 erase and program cycles. The MXIC cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The MX29F022T/B uses a $5.0V \pm 10\%$ VCC supply to perform the High Reliability Erase and auto Program/Erase algorithms.

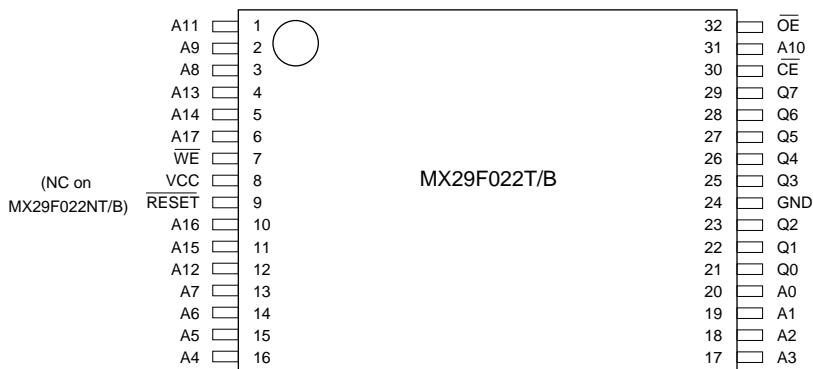
The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamps on address and data pin from -1V to VCC + 1V.

PIN CONFIGURATIONS

32 PDIP

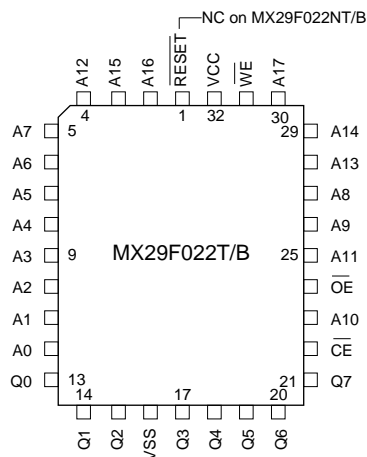


32 TSOP (TYPE 1)



(NORMAL TYPE)

32 PLCC



SECTOR STRUCTURE

A 17 ~ A 0

3 F F F F H

3 B F F F H

3 9 F F F H

3 7 F F F H

2 F F F F H

1 F F F F H

0 F F F F H

0 0 0 0 0 H

16 K - B Y T E (B O O T S E C T O R)
8 K - B Y T E
8 K - B Y T E
32 K - B Y T E
64 K - B Y T E
64 K - B Y T E
64 K - B Y T E

MX29F022T Sector Architecture

A 17 ~ A 0

3 F F F F H

2 F F F F H

1 F F F F H

0 F F F F H

0 7 F F F H

0 5 F F F H

0 3 F F F H

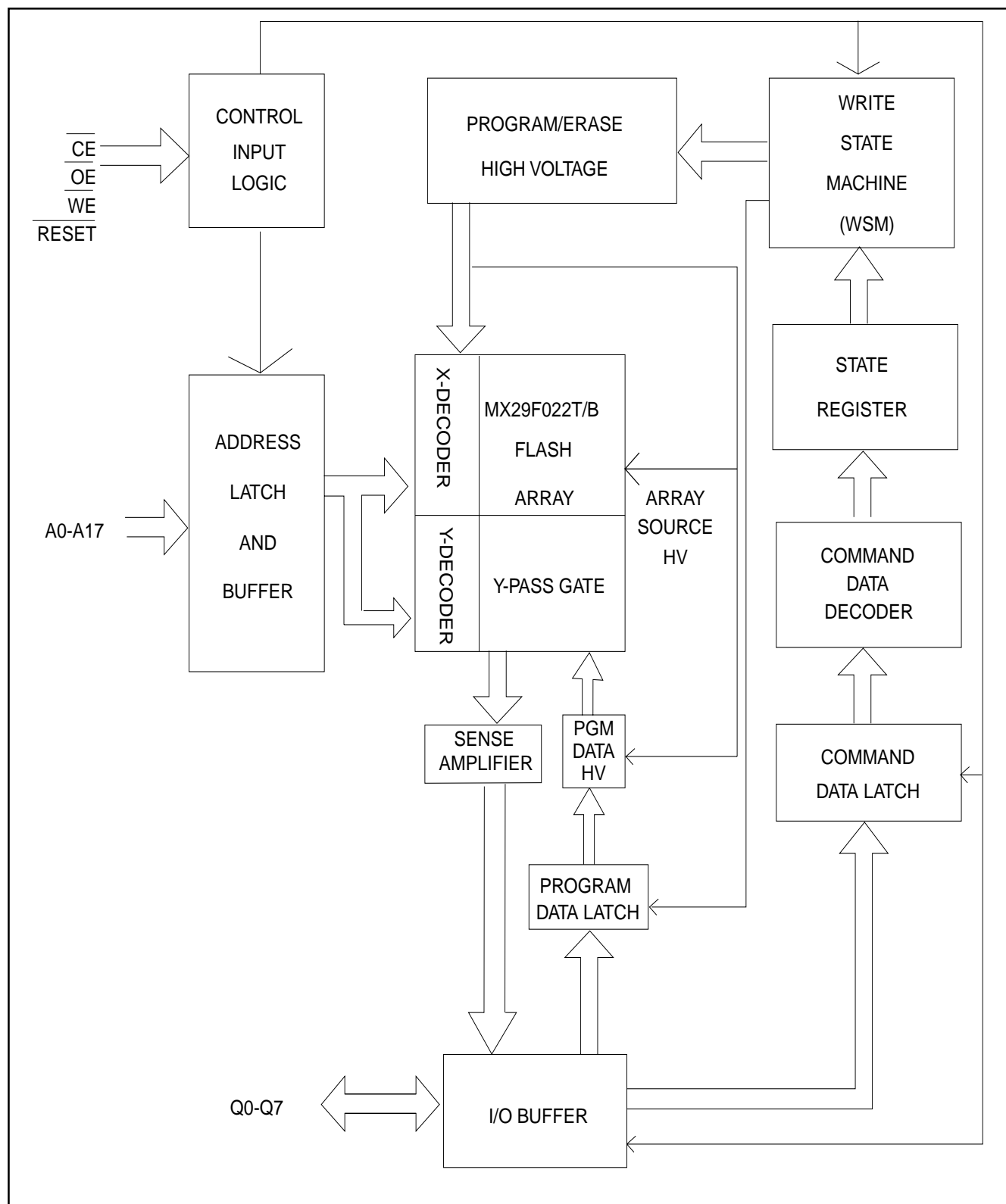
0 0 0 0 0 H

64 K - B Y T E
64 K - B Y T E
64 K - B Y T E
32 K - B Y T E
8 K - B Y T E
8 K - B Y T E
16 K - B Y T E (B O O T S E C T O R)

MX29F022B Sector Architecture

PIN DESCRIPTION:

SYMBOL	PIN NAME
A0~A17	Address Input
Q0~Q7	Data Input/Output
CE	Chip Enable Input
WE	Write Enable Input
RESET	Hardware Reset Pin/Sector Protect Unlock
OE	Output Enable Input
VCC	Power Supply Pin (+5V)
GND	Ground Pin

BLOCK DIAGRAM


AUTOMATIC PROGRAMMING

The MX29F022T/B is byte programmable using the Automatic Programming algorithm. The Automatic Programming algorithm does not require the system to time out or verify the data programmed. The typical chip programming time of the MX29F022T/B at room temperature is less than 2 seconds.

AUTOMATIC CHIP ERASE

The entire chip is bulk erased using 10ms erase pulses according to MXIC's High Reliability Chip Erase algorithm. Typical erasure at room temperature is accomplished in less than two second. The device is erased using the Automatic Erase algorithm. The Automatic Erase algorithm automatically programs the entire array prior to electrical erase. The timing and verification of electrical erase are internally controlled within the device.

AUTOMATIC SECTOR ERASE

The MX29F022T/B is sector(s) erasable using MXIC's Auto Sector Erase algorithm. Sector erase modes allow sectors of the array to be erased in one erase cycle. The Automatic Sector Erase algorithm automatically programs the specified sector(s) prior to electrical erase. The timing and verification of electrical erase are internally controlled by the device.

AUTOMATIC PROGRAMMING ALGORITHM

MXIC's Automatic Programming algorithm requires the user to only write a program set-up commands (include 2 unlock write cycle and A0H) include 2 unlock write cycle and A0H and a program command (program data and address). The device automatically times the programming pulse width, verifies the program verification, and counts the number of sequences. A status bit similar to \overline{DATA} polling and a status bit toggling between consecutive read cycles, provides feedback to the user as to the status of the programming operation.

AUTOMATIC ERASE ALGORITHM

MXIC's Automatic Erase algorithm requires the user to write commands to the command register using standard microprocessor write timings. The device will automatically pre-program and verify the entire array. Then the device automatically times the erase pulse width, verifies the erase, and counts the number of sequences. A status bit similar to \overline{DATA} polling and status bit toggling between consecutive read cycles provides feedback to the user as to the status of the programming operation.

Commands are written to the command register using standard microprocessor write timings. Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. During a system write cycle addresses are latched on the falling edge, and data are latched on the rising edge of \overline{WE} .

MXIC's Flash technology combines years of EPROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The MX29F022T/B electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

During a program cycle, the state-machine will control the program sequences and command register will not respond to any command set. During a Sector Erase cycle, the command register will only respond to Erase Suspend command. After Erase Suspend is completed, the device stays in read mode. After the state machine has completed its task, it will allow the command register to respond to its full command set.

TABLE 1. SOFTWARE COMMAND DEFINITIONS

Command	Bus Cycle	First Bus Cycle		Second Bus Cycle		Third Bus Cycle		Fourth Bus Cycle		Fifth Bus Cycle		Sixth Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Reset	1	XXXH	F0H										
Read	1	RA	RD										
Read Silicon ID	4	555H	AAH	2AAH	55H	555H	90H	ADI	DDI				
Chip Protect Verify	4	555H	AAH	2AAH	55H	555H	90H	(SA) X02H	00H 01H				
Program	4	555H	AAH	2AAH	55H	555H	A0H	PA	PD				
Chip Erase	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H
Sector Erase	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	SA	30H
Sector Erase Suspend	1	XXXH	B0H										
Sector Erase Resume	1	XXXH	30H										
Unlock for chip protect/unprotect	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	20H

Note:

- ADI = Address of Device identifier; A1=0, A0 =0 for manufacture code, A1=0, A0 =1 for device code (Refer to Table 3).
DDI = Data of Device identifier : C2H for manufacture code, 36H/37H for device code.
X = X can be VIL or VIH
RA=Address of memory location to be read.
RD=Data to be read at location RA.
- PA = Address of memory location to be programmed.
PD = Data to be programmed at location PA.
SA = Address to the sector to be erased.
- The system should generate the following address patterns: 555H or 2AAH to Address A0~A10.
Address bit A11~A17=X=Don't care for all address commands except for Program Address (PA) and Sector Address (SA). Write Sequence may be initiated with A11~A17 in either state.
- For Chip Protect Verify operation: If read out data is 01H, it means the chip has been protected. If read out data is 00H, it means the chip is still not being protected.

TABLE 2. MX29F022T/B BUS OPERATION

Pins Mode	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	A0	A1	A6	A9	Q0~Q7
Read Silicon ID Manufacturer Code(1)	L	L	H	L	L	X	$V_{\text{ID}}(2)$	C2H
Read Silicon ID Device Code(1)	L	L	H	H	L	X	$V_{\text{ID}}(2)$	36H/37H
Read	L	L	H	A0	A1	A6	A9	D_{OUT}
Standby	H	X	X	X	X	X	X	HIGH Z
Output Disable	L	H	H	X	X	X	X	HIGH Z
Write	L	H	L	A0	A1	A6	A9	$D_{\text{IN}}(3)$
Chip Protect with 12V system (6)	L	$V_{\text{ID}}(2)$	L	X	X	L	$V_{\text{ID}}(2)$	X
Chip Unprotect with 12V system (6)	L	$V_{\text{ID}}(2)$	L	X	X	H	$V_{\text{ID}}(2)$	X
Verify chip Protect with 12V system	L	L	H	X	H	X	$V_{\text{ID}}(2)$	Code (5)
Chip Protect without 12V system (6)	L	H	L	X	X	L	H	X
Chip Unprotect without 12V system (6)	L	H	L	X	X	H	H	X
Verify Chip Protect/Unprotect without 12V system (7)	L	L	H	X	H	X	H	Code(5)
Reset	X	X	X	X	X	X	X	HIGH Z

NOTES:

1. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 1.
2. VID is the Silicon-ID-Read high voltage, 11.5V to 12.5V.
3. Refer to Table 1 for valid Data-In during a write operation.
4. X can be VIL or VIH.
5. Code=00H means unprotected.
Code=01H means protected.
6. Refer to chip protect/unprotect algorithm and waveform.
Must issue "unlock for chip protect/unprotect" command before "chip protect/unprotect without 12V system" command.
7. The "verify chip protect/unprotect without 12V system" is only following "chip protect/unprotect without 12V system" command.

READ/RESET COMMAND

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the command register contents are altered.

If program-fail or erase-fail happen, the write of F0H will reset the device to abort the operation. A valid command must then be written to place the device in the desired state.

SILICON-ID-READ COMMAND

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto address lines is not generally desired system design practice.

The MX29F022T/B contains a Silicon-ID-Read operation to supplement traditional PROM programming methodology. The operation is initiated by writing the read silicon ID command sequence into the command register. Following the command write, a read cycle with A1=VIL, A0=VIL retrieves the manufacturer code of C2H. A read cycle with A1=VIL, A0=VIH returns the device code of 36H for MX29F022T, 37H for MX29F022B.

SET-UP AUTOMATIC CHIP/SECTOR ERASE COMMANDS

Chip erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command 80H. Two more "unlock" write cycles are then followed by the chip erase command 10H.

The Automatic Chip Erase does not require the device to be entirely pre-programmed prior to executing the Automatic Chip Erase. Upon executing the Automatic Chip Erase, the device will automatically program and verify the entire memory for an all-zero data pattern. When the device is automatically verified to contain an all-zero pattern, a self-timed chip erase and verification begin. The erase and verification operations are completed when the data on Q7 is "1" at which time the device returns to the Read mode. The system is not required to provide any control or timing during these operations.

When using the Automatic Chip Erase algorithm, note that the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase verify command is required).

If the Erase operation was unsuccessful, the data on Q5 is "1" (see Table 4), indicating the erase operation of exceed internal timing limit.

The automatic erase begins on the rising edge of the last WE pulse in the command sequence and terminates when the data on Q7 is "1" and the data on Q6 stops toggling for two consecutive read cycles, at which time the device returns to the Read mode.

TABLE 3. EXPANDED SILICON ID CODE

Pins	A0	A1	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Code(Hex)
Manufacture code	VIL	VIL	1	1	0	0	0	0	1	0	C2H
Device code for MX29F022T	VIH	VIL	0	0	1	1	0	1	1	0	36H
Device code for MX29F022B	VIH	VIL	0	0	1	1	0	1	1	1	37H
Chip Protection Verification	X	VIH	0	0	0	0	0	0	0	1	01H (Protected)
	X	VIH	0	0	0	0	0	0	0	0	00H (Unprotected)

SET-UP AUTOMATIC SECTOR ERASE COMMANDS

The Automatic Sector Erase does not require the device to be entirely pre-programmed prior to executing the Automatic Set-up Sector Erase command and Automatic Sector Erase command. Upon executing the Automatic Sector Erase command, the device will automatically program and verify the sector(s) memory for an all-zero data pattern. The system does not require to provide any control or timing during these operations.

When the sector(s) is automatically verified to contain an all-zero pattern, a self-timed sector erase and verification begin. The erase and verification operations are complete when the data on Q7 is "1" and the data on Q6 stops toggling for two consecutive read cycles, at which time the device returns to the Read mode. The system does not required to provide any control or timing during these operations.

When using the Automatic Sector Erase algorithm, note that the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase verification command is required). Sector erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the set-up command-80H. Two more "unlock" write cycles are then followed by the sector erase command-30H. The sector address is latched on the falling edge of \overline{WE} , while the command(data) is latched on the rising edge of \overline{WE} . Sector addresses selected are loaded into internal register on the sixth falling edge of \overline{WE} . Each successive sector load cycle started by the falling edge of \overline{WE} must begin within 30 μ s from the rising edge of the preceding \overline{WE} . Otherwise, the loading period ends and internal auto sector erase cycle starts. (Monitor Q3 to determine if the sector erase timer window is still open, see section Q3, Sector Erase Timer.) Any command other than Sector Erase (30H) or Erase Suspend (B0H) during the time-out period resets the device to read mode.

ERASE SUSPEND

This command is only valid while the state machine is executing Automatic Sector Erase operation, and therefore will only be responded during Automatic/Sector Erase operation. Writing the Erase Suspend command during the Sector Erase time-out immediately terminates the time-out period and suspends the erase op-

eration. After this command has been executed, the command register will initiate erase suspend mode. The state machine will return to read mode automatically after suspend is ready. At this time, state machine only allows the command register to respond to the Read Memory Array, Erase Resume and Program commands. The system can determine the status of the program operation using the Q7 or Q6 status bits, just as in the standard program operation. After an erase-suspended program operation is complete, the system can once again read array data within non-suspended sectors.

TABLE 4. WRITE OPERATION STATUS

	Status		Q7	Q6	Q5	Q3	Q2
			Note1		Note2		
In Progress	Byte Program in Auto Program Algorithm		$\overline{Q7}$	Toggle	0	N/A	No Toggle
	Auto Erase Algorithm		0	Toggle	0	1	Toggle
	Erase Suspended Mode	Erase Suspend Read (Erase Suspended Sector)	1	No Toggle	0	N/A	Toggle
		Erase Suspend Read (Non-Erase Suspended Sector)	Data	Data	Data	Data	Data
		Erase Suspend Program	$\overline{Q7}$	Toggle	0	N/A	N/A
Exceeded Time Limits	Byte Program in Auto Program Algorithm		$\overline{Q7}$	Toggle	1	N/A	No Toggle
	Auto Erase Algorithm		0	Toggle	1	1	Toggle
	Erase Suspend Program		$\overline{Q7}$	Toggle	1	N/A	N/A

Note:

1. Q7 and Q2 require a valid address when reading status information. Refer to the appropriate subsection for further details.
2. Q5 switches to '1' when an Auto Program or Auto Erase operation has exceeded the maximum timing limits. See "Q5 : Exceeded Timing Limits" for more information.

ERASE RESUME

This command will cause the command register to clear the suspend state and return back to Sector Erase mode but only if an Erase Suspend command was previously issued. Erase Resume will not have any effect in all other conditions. Another Erase Suspend command can be written after the chip has resumed erasing.

SET-UP AUTOMATIC PROGRAM COMMANDS

To initiate Automatic Program mode, A three-cycle command sequence is required. There are two "unlock" write cycles. These are followed by writing the Automatic Program command A0H.

Once the Automatic Program command is initiated, the next \overline{WE} pulse causes a transition to an active programming operation. Addresses are latched on the falling edge, and data are internally latched on the rising edge of the \overline{WE} pulse. The rising edge of \overline{WE} also begins the programming operation. The system does not require to provide further controls or timings. The device will automatically provide an adequate internally generated program pulse and verify margin.

If the program operation was unsuccessful, the data on Q5 is "1", indicating the program operation of internally exceed timing limit. The automatic programming operation is complete when the data read on Q6 stops toggling for two consecutive read cycles and the data on Q7 and Q6 are equivalent to data written to these two bits, at which time the device returns to the Read mode (no program verify command is required).

WRITE OPERATION STATUS DATA POLLING-Q7

The MX29F022T/B also features \overline{Data} Polling as a method to indicate to the host system that the Automatic Program or Erase algorithms are either in progress or completed.

While the Automatic Programming algorithm is in operation, an attempt to read the device will produce the complement data of the data last written to Q7. Upon completion of the Automatic Program Algorithm an attempt to read the device will produce the true data last written to Q7. The Data Polling feature is valid after the

rising edge of the second \overline{WE} pulse of the two write pulse sequences.

While the Automatic Erase algorithm is in operation, Q7 will read "0" until the erase operation is complete. Upon completion of the erase operation, the data on Q7 will read "1". The Data Polling feature is valid after the rising edge of the second \overline{WE} pulse of two write pulse sequences.

The Data Polling feature is active during Automatic Program/Erase algorithm or sector erase time-out. (see section Q3 Sector Erase Timer)

Q6 : Toggle BIT I

The MX29F022T/B features a "Toggle Bit" as a method to indicate to the host system that the Auto Program/Erase algorithms are either in progress or complete.

During an Automatic Program or Erase algorithm operation, successive read cycles to any address cause Q6 to toggle. The system may use either OE or CE to control the read cycles. When the operation is complete, Q6 stops toggling.

After an erase command sequence is written, if the chip is protected, Q6 toggles and returns to reading array data.

The system can use Q6 and Q2 together to determine whether a sector is actively erasing or is erase suspended. When the device is actively erasing (that is, the Automatic Erase algorithm is in progress), Q6 toggling. When the device enters the Erase Suspend mode, Q6 stops toggling. However, the system must also use Q2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use Q7 (see the subsection on Q7 : Data Polling).

If a program address falls within a protected sector, Q6 toggles for approximately 2 μ s after the program command sequence is written, then returns to reading array data.

Q6 also toggles during the erase-suspend-program mode, and stops toggling once the Automatic Program algorithm is complete.

The Write Operation Status table shows the outputs for Toggle Bit I on Q6. Refer to the toggle bit algorithm.

Q2:Toggle Bit II

The "Toggle Bit II" on Q2, when used with Q6, indicates whether a particular sector is actively erasing (that is, the Automatic Erase algorithm is in process), or whether that sector is erase-suspended. Toggle Bit I is valid after the rising edge of the final WE pulse in the command sequence.

Q2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE or CE to control the read cycles.) But Q2 cannot distinguish whether the sector is actively erasing or is erase-suspended. Q6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sectors and mode information. Refer to Table 4 to compare outputs for Q2 and Q6.

Reading Toggle Bits Q6/ Q2

Refer to the toggle bit algorithm for the following discussion. Whenever the system initially begins reading toggle bit status, it must read Q7-Q0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on Q7-Q0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of Q5 is high (see the section on Q5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as Q5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that system initially determines that the toggle bit is toggling and Q5 has not gone high. The system may continue to monitor the toggle bit and Q5 through successive read cycles, determining the

status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of the toggle bit algorithm flow chart).

Q5

Exceeded Timing Limits

Q5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions Q5 will produce a "1". This time-out condition indicates that the program or erase cycle was not successfully completed. Data Polling and Toggle Bit are the only operating functions not of the device under this condition.

If this time-out condition occurs during sector erase operation, it specifies that a particular sector is bad and it may not be reused. However, other sectors are still functional and may be used for the program or erase operation. The device must be reset to use other sectors. Write the Reset command sequence to the device, and then execute program or erase command sequence. This allows the system to continue to use the other active sectors in the device.

If this time-out condition occurs during the chip erase operation, it specifies that the entire chip is bad or combination of sectors are bad.

If this time-out condition occurs during the byte programming operation, it specifies that the entire sector containing that byte is bad and this sector may not be reused, (other sectors are still functional and can be reused).

The time-out condition may also appear if a user tries to program a non blank location without erasing. In this case the device locks out and never completes the Automatic Algorithm operation. Hence, the system never reads a valid data on Q7 bit and Q6 never stops toggling. Once the Device has exceeded timing limits, the Q5 bit will indicate a "1". Please note that this is not a device failure condition since the device was incorrectly used.

Q3**Sector Erase Timer**

After the completion of the initial sector erase command sequence the sector erase time-out will begin. Q3 will remain low until the time-out is complete. Data Polling and Toggle Bit are valid after the initial sector erase command sequence.

If $\overline{\text{Data Polling}}$ or the Toggle Bit indicates the device has been written with a valid erase command, Q3 may be used to determine if the sector erase timer window is still open. If Q3 is high ("1") the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by $\overline{\text{Data Polling}}$ or Toggle Bit. If Q3 is low ("0"), the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of Q3 prior to and following each subsequent sector erase command. If Q3 were high on the second status check, the command may not have been accepted.

DATA PROTECTION

The MX29F022T/B is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transition. During power up the device automatically resets the state machine in the Read mode. In addition, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from VCC power-up and power-down transition or system noise.

WRITE PULSE "GLITCH" PROTECTION

Noise pulses of less than 5ns (typical) on $\overline{\text{CE}}$ or $\overline{\text{WE}}$ will not initiate a write cycle.

LOGICAL INHIBIT

Writing is inhibited by holding any one of $\overline{\text{OE}} = \text{VIL}$, $\overline{\text{CE}} = \text{VIH}$ or $\overline{\text{WE}} = \text{VIH}$. To initiate a write cycle $\overline{\text{CE}}$ and $\overline{\text{WE}}$ must be a logical zero while $\overline{\text{OE}}$ is a logical one.

POWER SUPPLY DECOUPLING

In order to reduce power switching effect, each device should have a 0.1uF ceramic capacitor connected between its VCC and GND.

CHIP PROTECTION WITH 12V SYSTEM

The MX29F022T/B features hardware chip protection, which will disable both program and erase operations. To activate this mode, the programming equipment must force VID on address pin A9 and control pin $\overline{\text{OE}}$, (suggest VID = 12V) A6 = VIL and $\overline{\text{CE}} = \text{VIL}$. (see Table 2) Programming of the protection circuitry begins on the falling edge of the $\overline{\text{WE}}$ pulse and is terminated on the rising edge. Please refer to chip protect algorithm and waveform.

To verify programming of the protection circuitry, the programming equipment must force VID on address pin A9 (with $\overline{\text{CE}}$ and $\overline{\text{OE}}$ at VIL and $\overline{\text{WE}}$ at VIH. When A1=1, it will produce a logical "1" code at device output Q0 for the protected status. Otherwise the device will produce 00H for the unprotected status. In this mode, the addresses, except for A1, are in "don't care" state. Address locations with A1 = VIL are reserved to read manufacturer and device codes. (Read Silicon ID)

It is also possible to determine if the chip is protected in the system by writing a Read Silicon ID command. Performing a read operation with A1=VIH, it will produce a logical "1" at Q0 for the protected status.

CHIP UNPROTECT WITH 12V SYSTEM

The MX29F022T/B also features the chip unprotect mode, so that all sectors are unprotected after chip unprotect is completed to incorporate any changes in the code.

To activate this mode, the programming equipment must force VID on control pin $\overline{\text{OE}}$ and address pin A9. The $\overline{\text{CE}}$ pins must be set at VIL. Pins A6 must be set to VIH. (see Table 2) Refer to chip unprotect algorithm and waveform for the chip unprotect algorithm. The unprotection mechanism begins on the falling edge of the $\overline{\text{WE}}$ pulse and is terminated on the rising edge.

It is also possible to determine if the chip is unprotected in the system by writing the Read Silicon ID command.

Performing a read operation with A1=VIH, it will produce 00H at data outputs (Q0-Q7) for an unprotected chip. It is noted that all sectors are unprotected after the chip unprotect algorithm is complete.

CHIP PROTECTION WITHOUT 12V SYSTEM

The MX29F022T/B also feature a hardware chip protection method in a system without 12V power supply. The programming equipment do not need to supply 12 volts to protect all sectors. The details are shown in chip protect algorithm and waveform.

CHIP UNPROTECT WITHOUT 12V SYSTEM

The MX29F022T/B also feature a hardware chip unprotection method in a system without 12V power supply. The programming equipment do not need to supply 12 volts to unprotect all sectors. The details are shown in chip unprotect algorithm and waveform.

POWER-UP SEQUENCE

The MX29F022T/B powers up in the Read only mode. In addition, the memory contents may only be altered after successful completion of a two-step command sequence. Vpp and Vcc power up sequence is not required.

ABSOLUTE MAXIMUM RATINGS

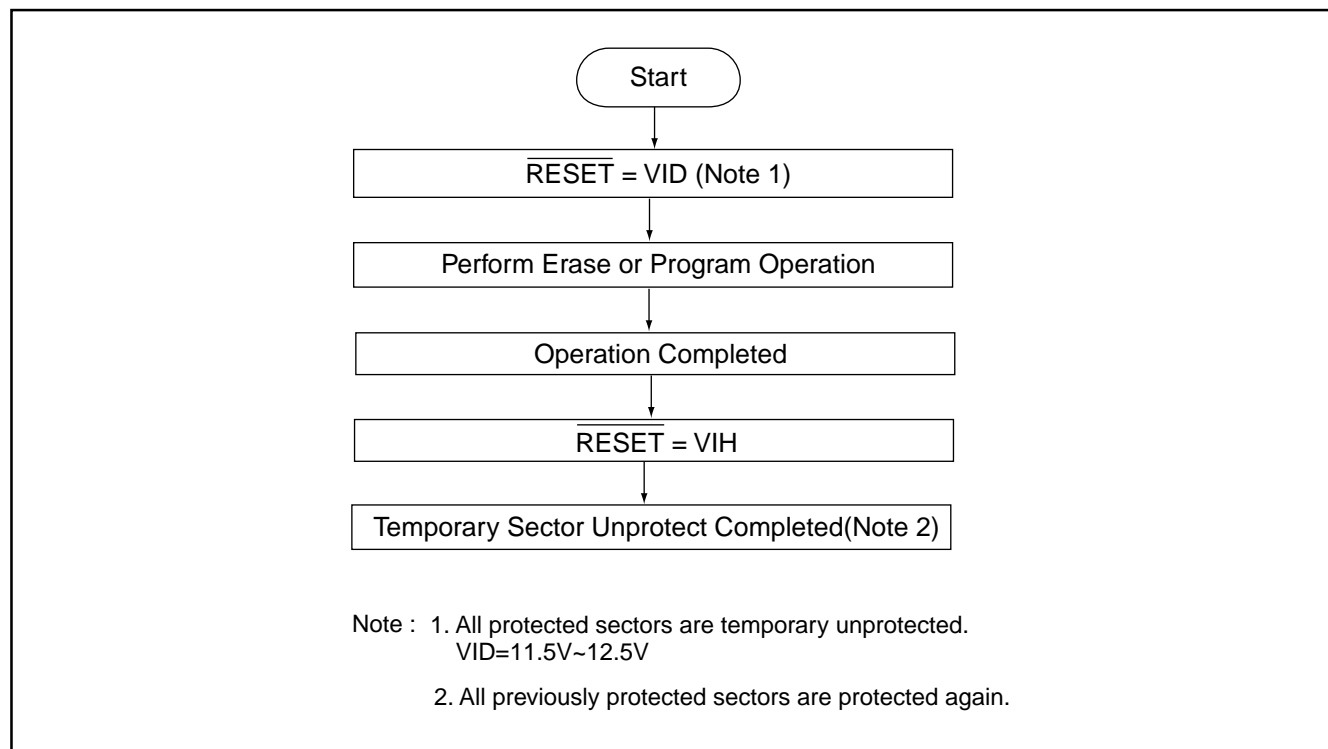
RATING	VALUE
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 125°C
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to 7.0V
VCC to Ground Potential	-0.5V to 7.0V
A9	-0.5V to 13.5V

NOTICE:

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

NOTICE:

Specifications contained within the following tables are subject to change.

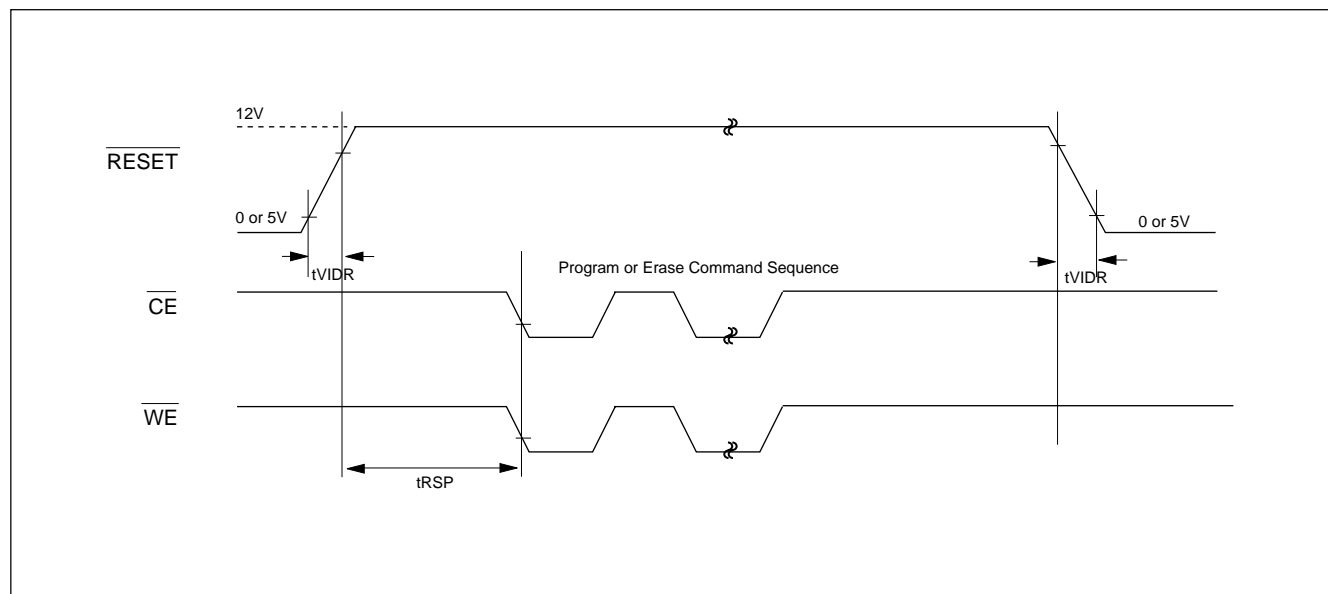
TEMPORARY SECTOR UNPROTECT OPERATION (only for 29F022T/B)

TEMPORARY SECTOR UNPROTECT

Parameter Std.	Description	Test Setup	All Speed Options	Unit
tVIDR	VID Rise and Fall Time (See Note)	Min	500	ns
tRSP	RESET Setup Time for Temporary Sector Unprotect	Min	4	us

Note:
Not 100% tested

TEMPORARY SECTOR UNPROTECT TIMING DIAGRAM (only for 29F022T/B)

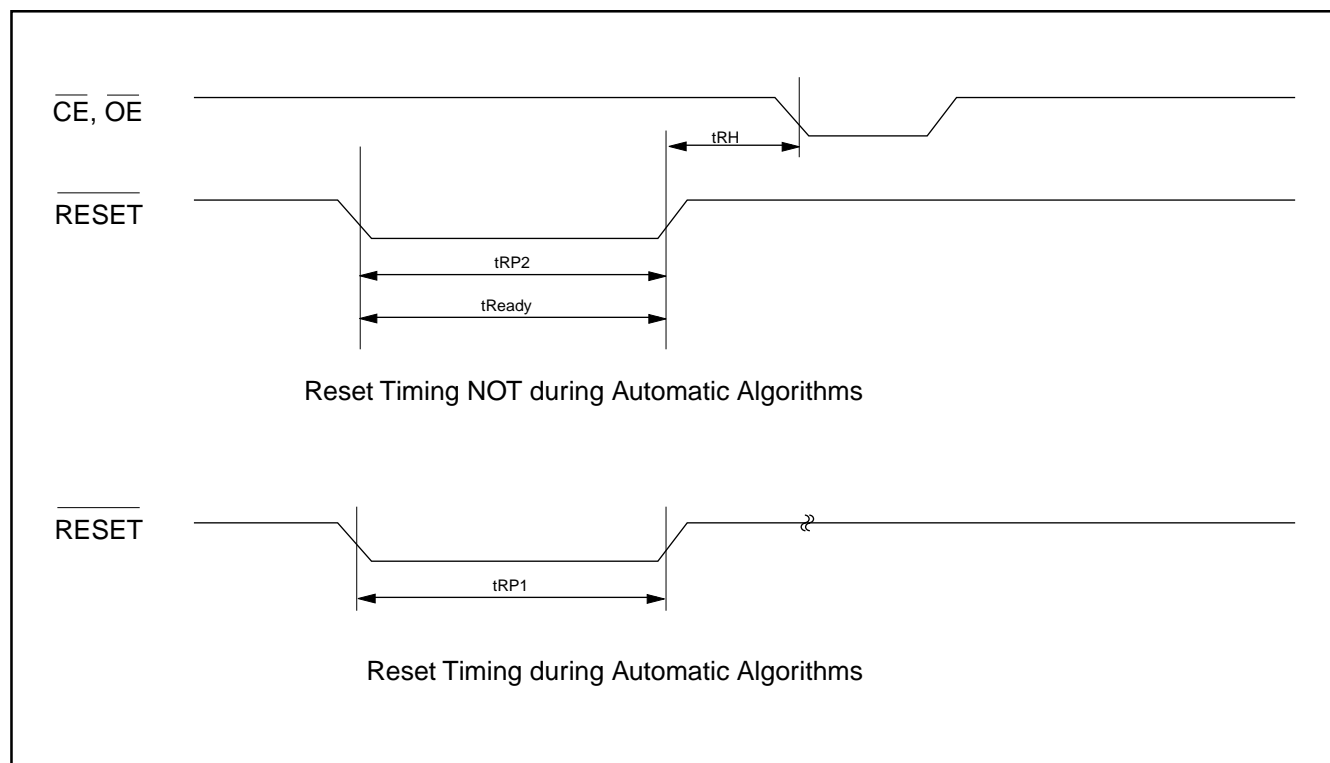


AC CHARACTERISTICS

Parameter Std	Description	Test Setup	All Speed Options	Unit
tREADY	RESET PIN Low (Not During Automatic Algorithms) to Read or Write (See Note)	MAX	500	ns
tRP1	RESET Pulse Width (During Automatic Algorithms)	MIN	10	us
tRP2	RESET Pulse Width (NOT During Automatic Algorithms)	MIN	500	ns
tRH	RESET High Time Before Read(See Note)	MIN	0	ns

Note:
Not 100% tested

RESET TIMING WAVEFORM (only for 29F002T/B)



CAPACITANCE TA = 25°C, f = 1.0 MHz

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
CIN1	Input Capacitance			8	pF	VIN = 0V
CIN2	Control Pin Capacitance			12	pF	VIN = 0V
COUT	Output Capacitance			12	pF	VOUT = 0V

READ OPERATION
DC CHARACTERISTICS TA = 0°C TO 70°C, VCC = 5V ± 10% (VCC=5V ± 5% for 29F022/022N-55)

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
ILI	Input Leakage Current			1	mA	VIN = GND to VCC
ILO	Output Leakage Current			10	mA	VOUT = GND to VCC
ISB1	Standby VCC current			1	mA	$\overline{CE} = V_{IH}$
ISB2			1	5	uA	$\overline{CE} = V_{CC} + 0.3V$
ICC1	Operating VCC current			30	mA	IOUT = 0mA, f=5MHz
ICC2				50	mA	IOUT = 0mA, f=10MHz
VIL	Input Low Voltage	-0.3(NOTE1)		0.8	V	
VIH	Input High Voltage	2.0		VCC + 0.3	V	
VOL	Output Low Voltage			0.45	V	IOL = 2.1mA
VOH1	Output High Voltage(TTL)	2.4			V	IOH = -2mA
VOH2	Output High Voltage(CMOS)	VCC-0.4			V	IOH = -100uA, VCC=VCC MIN

NOTES:

- VIL min. = -1.0V for pulse width is equal to or less than 50 ns.
VIL min. = -2.0V for pulse width is equal to or less than 20 ns.
- VIH max. = VCC + 1.5V for pulse width is equal to or less than 20 ns
If VIH is over the specified maximum value, read operation cannot be guaranteed.

AC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ±10%(VCC = 5V ±5% for 29F022T/B-55)

SYMBOL	PARAMETER	<u>29F022T/B-55</u>		<u>29F022T/B-70</u>		UNIT	CONDITIONS
		MIN.	MAX.	MIN.	MAX.		
tACC	Address to Output Delay		55		70	ns	$\overline{CE}=\overline{OE}=VIL$
tCE	\overline{CE} to Output Delay		55		70	ns	$\overline{OE}=VIL$
tOE	\overline{OE} to Output Delay		25		30	ns	$\overline{CE}=VIL$
tDF	\overline{OE} High to Output Float (Note1)	0	20	0	20	ns	$\overline{CE}=VIL$
tOH	Address to Output hold	0		0		ns	$\overline{CE}=\overline{OE}=VIL$

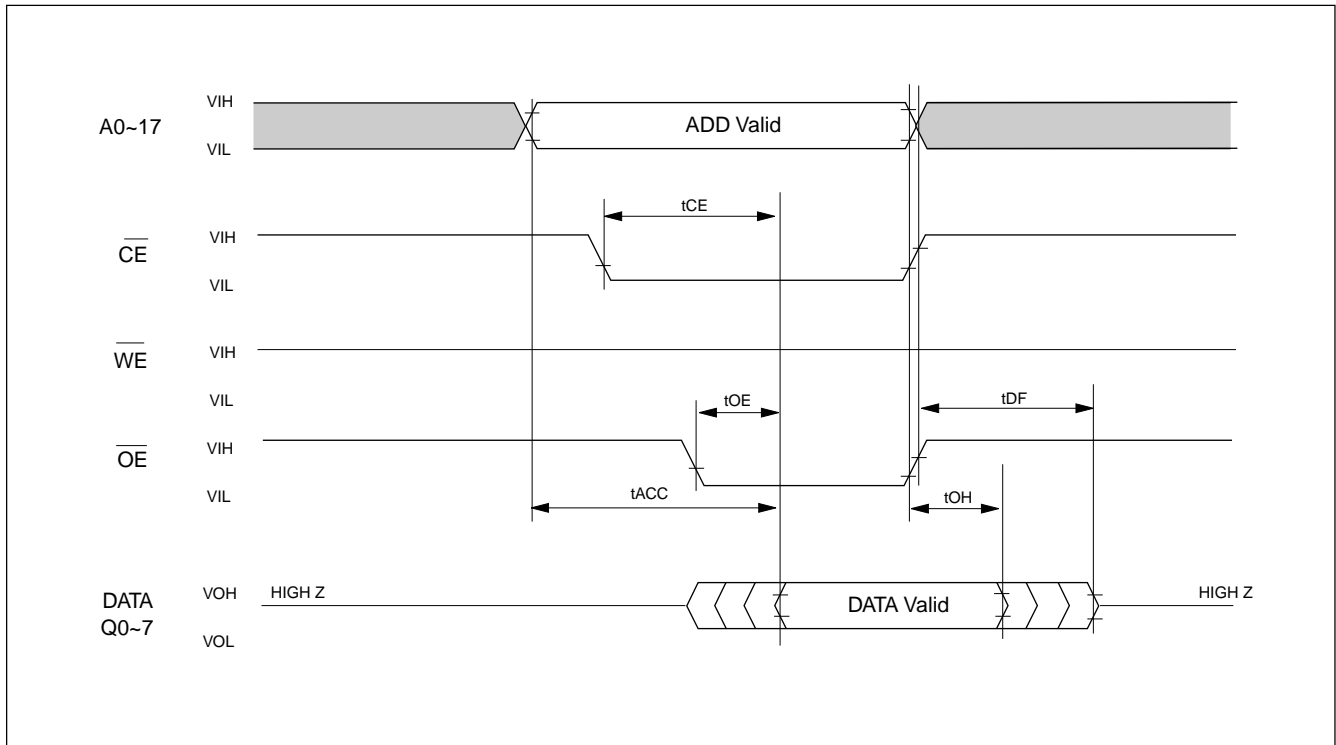
SYMBOL	PARAMETER	<u>29F022T/B-90</u>		<u>29F022T/B-120</u>		UNIT	CONDITIONS
		MIN.	MAX.	MIN.	MAX.		
tACC	Address to Output Delay		90		120	ns	$\overline{CE}=\overline{OE}=VIL$
tCE	\overline{CE} to Output Delay		90		120	ns	$\overline{OE}=VIL$
tOE	\overline{OE} to Output Delay		40		50	ns	$\overline{CE}=VIL$
tDF	\overline{OE} High to Output Float (Note1)	0	30	0	30	ns	$\overline{CE}=VIL$
tOH	Address to Output hold	0		0		ns	$\overline{CE}=\overline{OE}=VIL$

TEST CONDITIONS:

- Input pulse levels: 0.45V/2.4V for 70ns max.
: 0V/3V for 55ns speed grade.
- Input rise and fall times: ≤ 10 ns for 70ns max.
: ≤ 5 ns for 55ns speed grade.
- Output load: 1 TTL gate + 100pF(Including scope and jig) for 70ns max.
: 1 TTL gate + 50pF(Including scope and jig) for 55ns speed grade.
- Reference levels for measuring timing : 0.8V/2.0V or 70ns max.
: 1.5V/1.5V for 55ns speed grade.

NOTE:

1.tDF is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

READ TIMING WAVEFORMS


COMMAND PROGRAMMING/DATA PROGRAMMING/ERASE OPERATION**DC CHARACTERISTICS** TA = 0°C to 70°C, VCC = 5V ± 10%(VCC = 5V ± 5% for 29F022/022N-55)

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
ICC1 (Read)	Operating VCC Current			30	mA	IOUT=0mA, f=5MHz
ICC2				50	mA	IOUT=0mA, F=10MHz
ICC3 (Program)				50	mA	In Programming
ICC4 (Erase)				50	mA	In Erase
ICCES	VCC Erase Suspend Current		2		mA	\overline{CE} =VIH, Erase Suspended

NOTES:

1. VIL min. = -0.6V for pulse width is equal to or less than 20ns.
2. If VIH is over the specified maximum value, programming operation cannot be guaranteed.
3. ICCES is specified with the device de-selected. If the device is read during erase suspend mode, current draw is the sum of ICCES and ICC1 or ICC2.
4. All current are in RMS unless otherwise noted.

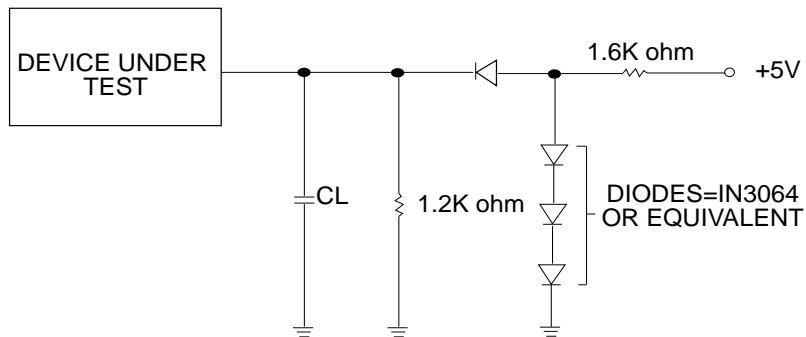
AC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 10%(VCC=5V±5% for 29F022T/B-55)

		29F022T/B-55(Note2)		29F022T/B-70		29F022T/B-90		29F022T/B-12		
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNIT
tOES	\overline{OE} setup time	0		0		0		0		ns
tCWC	Command programming cycle	70		70		90		120		ns
tCEP	\overline{WE} programming pulse width	45		45		45		50		ns
tCEPH1	\overline{WE} programming pulse width High	20		20		20		20		ns
tCEPH2	\overline{WE} programming pulse width High	20		20		20		20		ns
tAS	Address setup time	0		0		0		0		ns
tAH	Address hold time	45		45		45		50		ns
tDS	Data setup time	20		30		45		50		ns
tDH	Data hold time	0		0		0		0		ns
tCESC	\overline{CE} setup time before command write	0		0		0		0		ns
tDF	Output disable time (Note 1)		20		30		40		40	ns
tAETC	Total erase time in auto chip erase	3(TYP.)	24	3(TYP.)	24	3(TYP.)	24	3(TYP.)	24	s
tAETB	Total erase time in auto sector erase	1(TYP.)	8	1(TYP.)	8	1(TYP.)	8	1(TYP.)	8	s
tAVT	Total programming time in auto verify (Byte Program time)	7(TYP.)	210	7(TYP.)	210	7(TYP.)	210	7(TYP.)	210	us
tBAL	Sector address load time	100		100		100		100		us
tCH	\overline{CE} Hold Time	0		0		0		0		us
tCS	\overline{CE} setup to \overline{WE} going low	0		0		0		0		us
tVLHT	Voltage Transition Time	4		4		4		4		us
tOESP	\overline{OE} Setup Time to \overline{WE} Active	4		4		4		4		us
tWPP1	Write pulse width for chip protect	10		10		10		10		us
tWPP2	Write pulse width for chip unprotect	12		12		12		12		ms

NOTES:

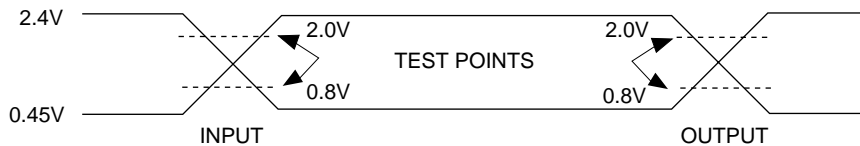
- 1.tDF defined as the time at which the output achieves the open circuit condition and data is no longer driven.
- 2.Under condition of VCC=5V±5%,CL=50pF, VIH/VIL=3.0V/0V, VOH/VOL=1.5V/1.5V,IOL=2mA,IOH=-2mA.

SWITCHING TEST CIRCUITS



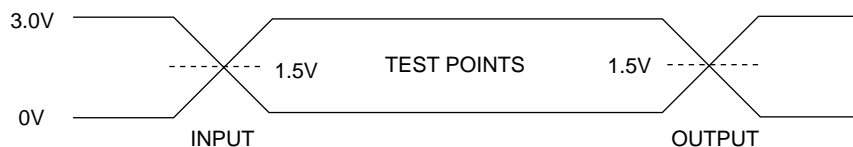
CL=100pF Including jig capacitance for 29F022/022N-70,
29F022/022N-90,29F022/022N-12
CL=50pF Including jig capacitance for 29F022/022N-55

SWITCHING TEST WAVEFORMS(I) for MX29F022/022N-70/90/120

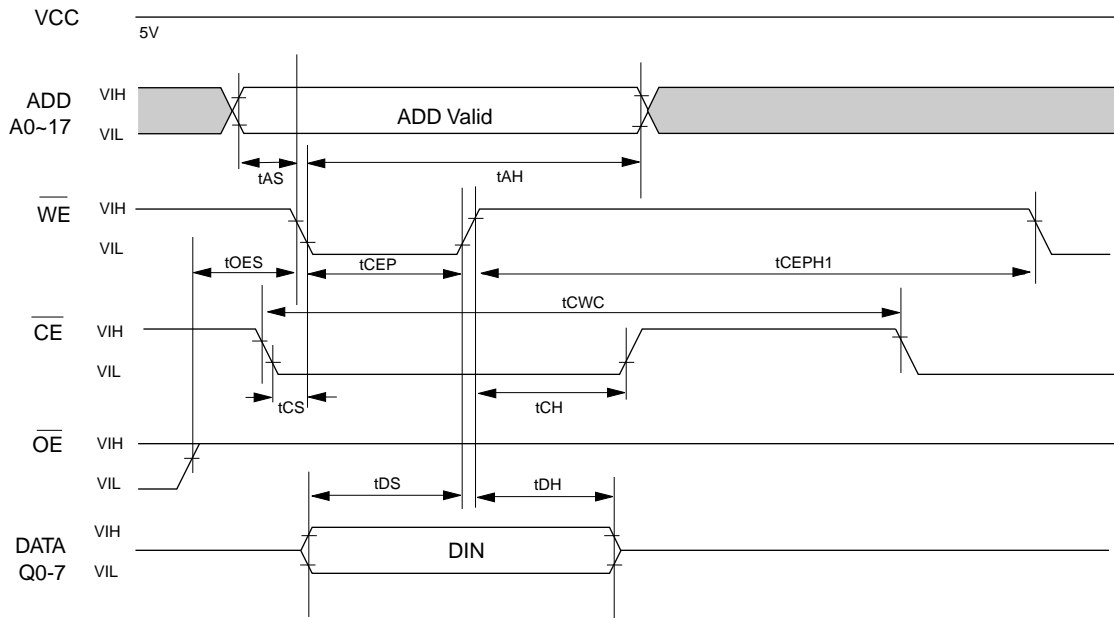


AC TESTING: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0".
Input pulse rise and fall times are <20ns.

SWITCHING TEST WAVEFORMS(I) for MX29F022/022N-55



AC TESTING: Inputs are driven at 3.0V for a logic "1" and 0V for a logic "0".
Input pulse rise and fall times are < 5ns.

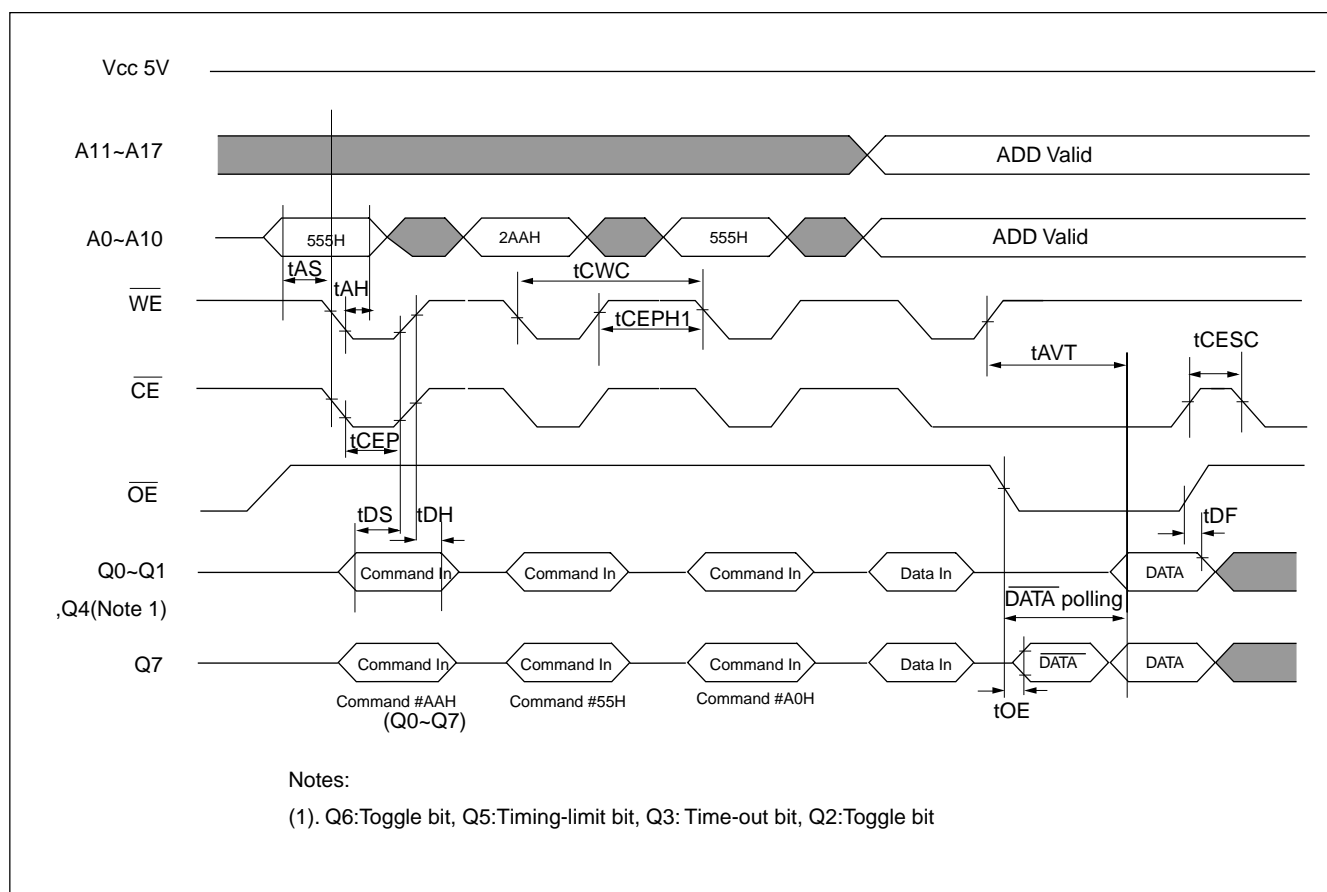
COMMAND WRITE TIMING WAVEFORM


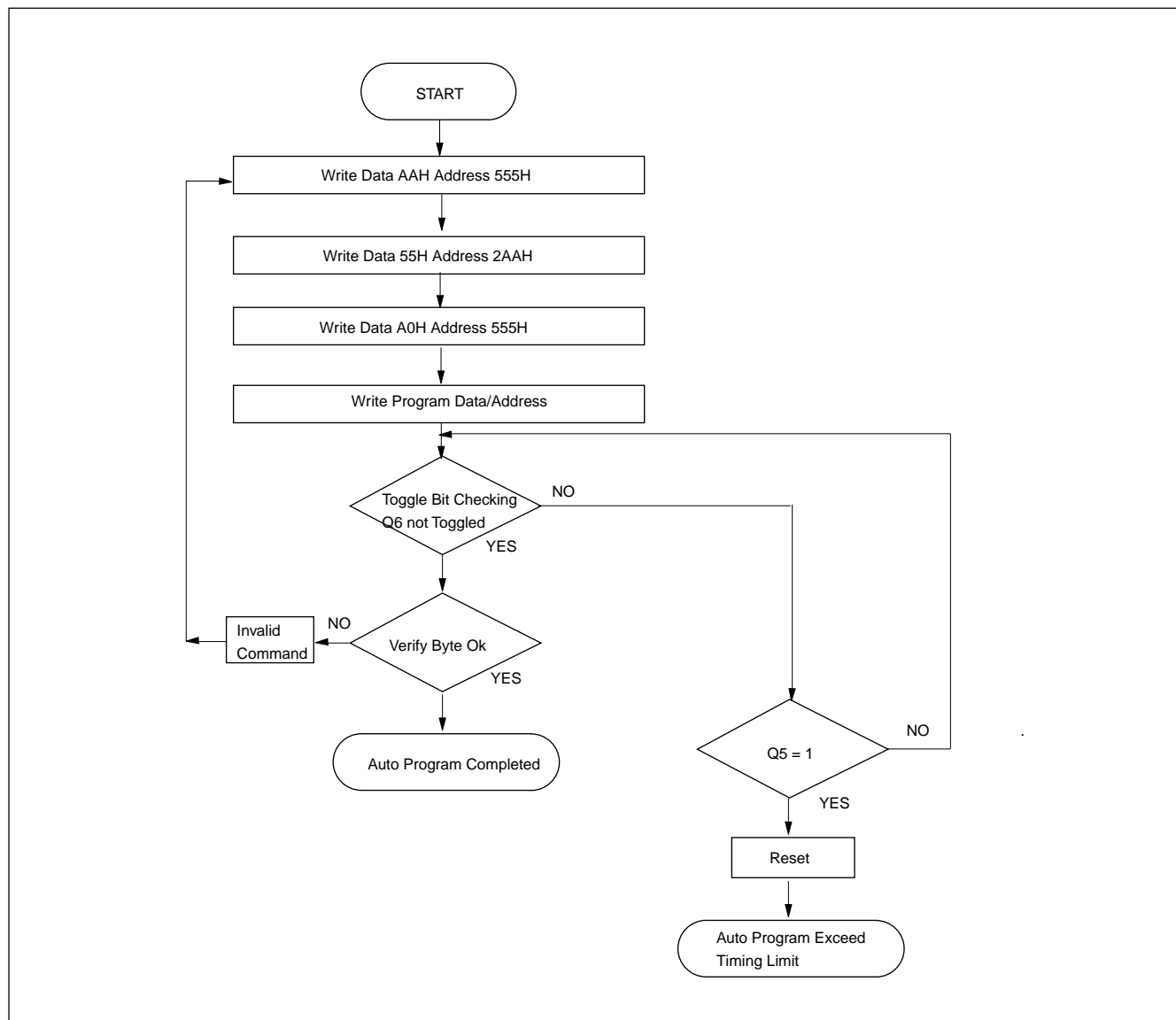
AUTOMATIC PROGRAMMING TIMING WAVEFORM

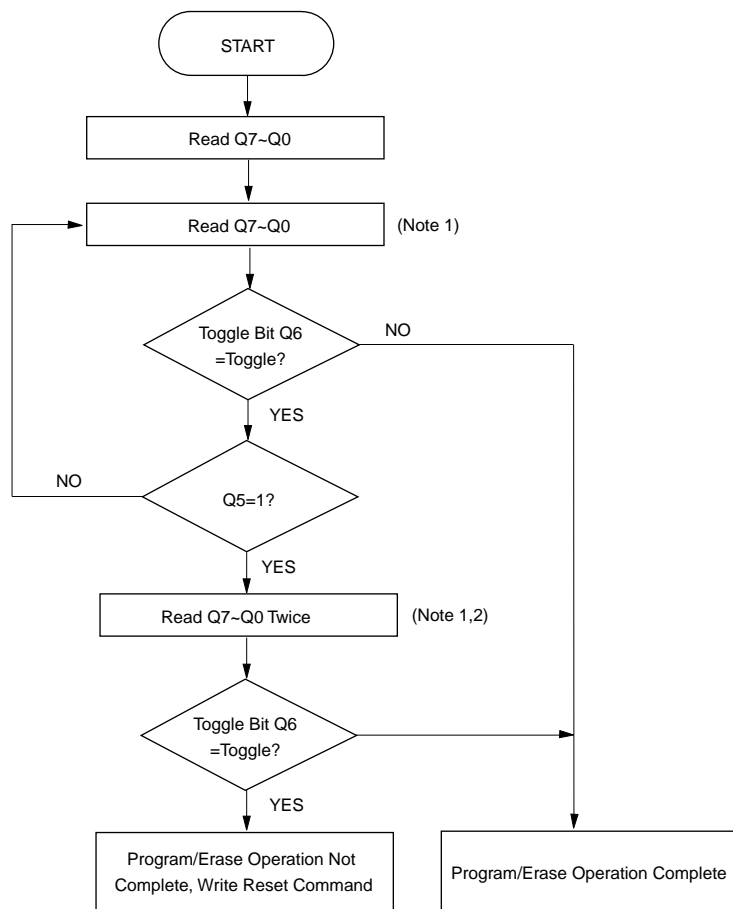
One byte data is programmed. Verifying in fast algorithm and additional programming by external control are not required because these operations are executed automatically by internal control circuit. Programming completion can be verified by DATA

polling and toggle bit checking after automatic verification starts. Device outputs DATA during programming and DATA after programming on Q7.(Q6 is for toggle bit; see toggle bit, DATA polling, timing waveform)

AUTOMATIC PROGRAMMING TIMING WAVEFORM



AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART


TOGGLE BIT ALGORITHM

Notes:

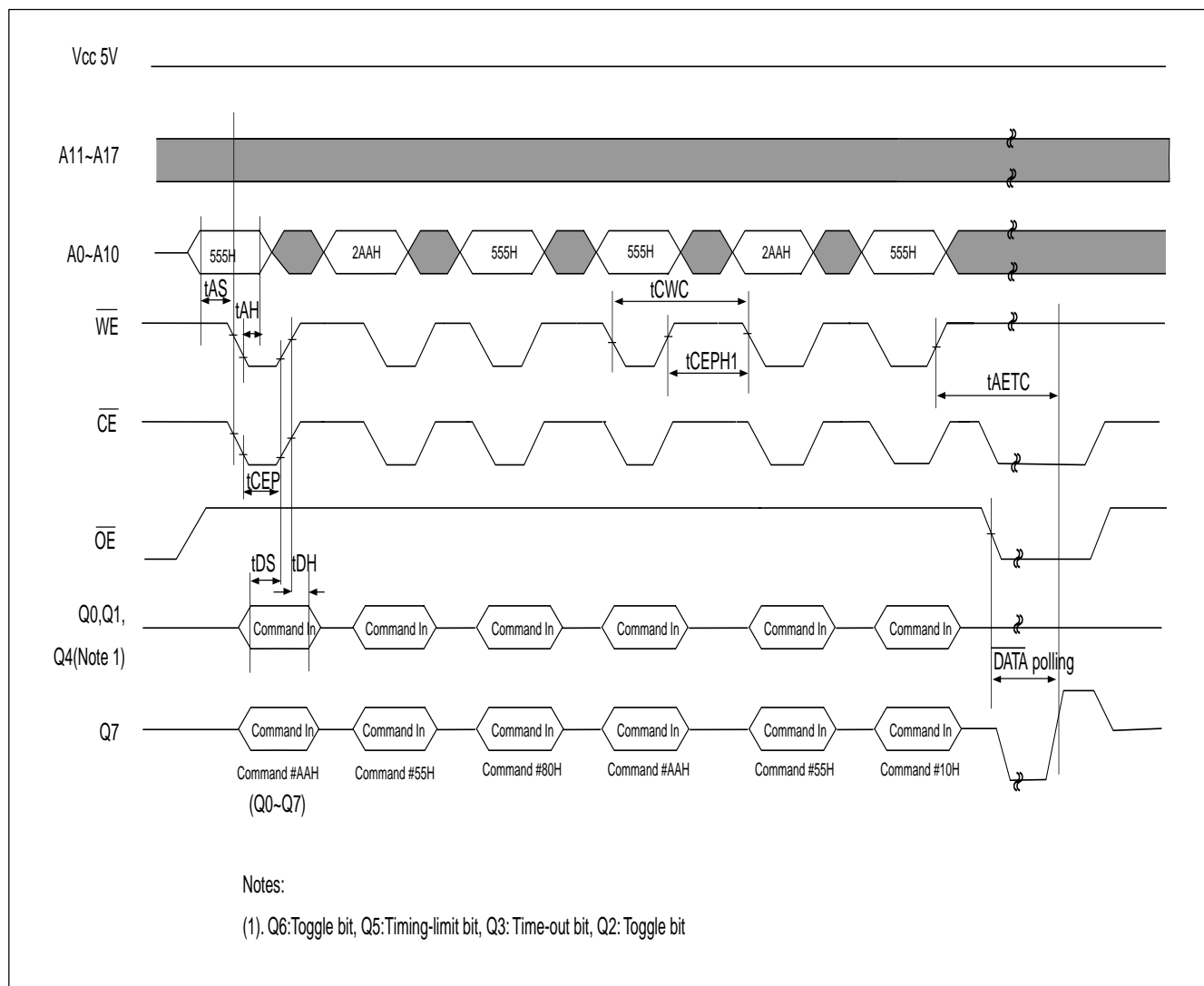
1. Read toggle bit Q6 twice to determine whether or not it is toggle. See text.
2. Recheck toggle bit Q6 because it may stop toggling as Q5 changes to "1". See text.

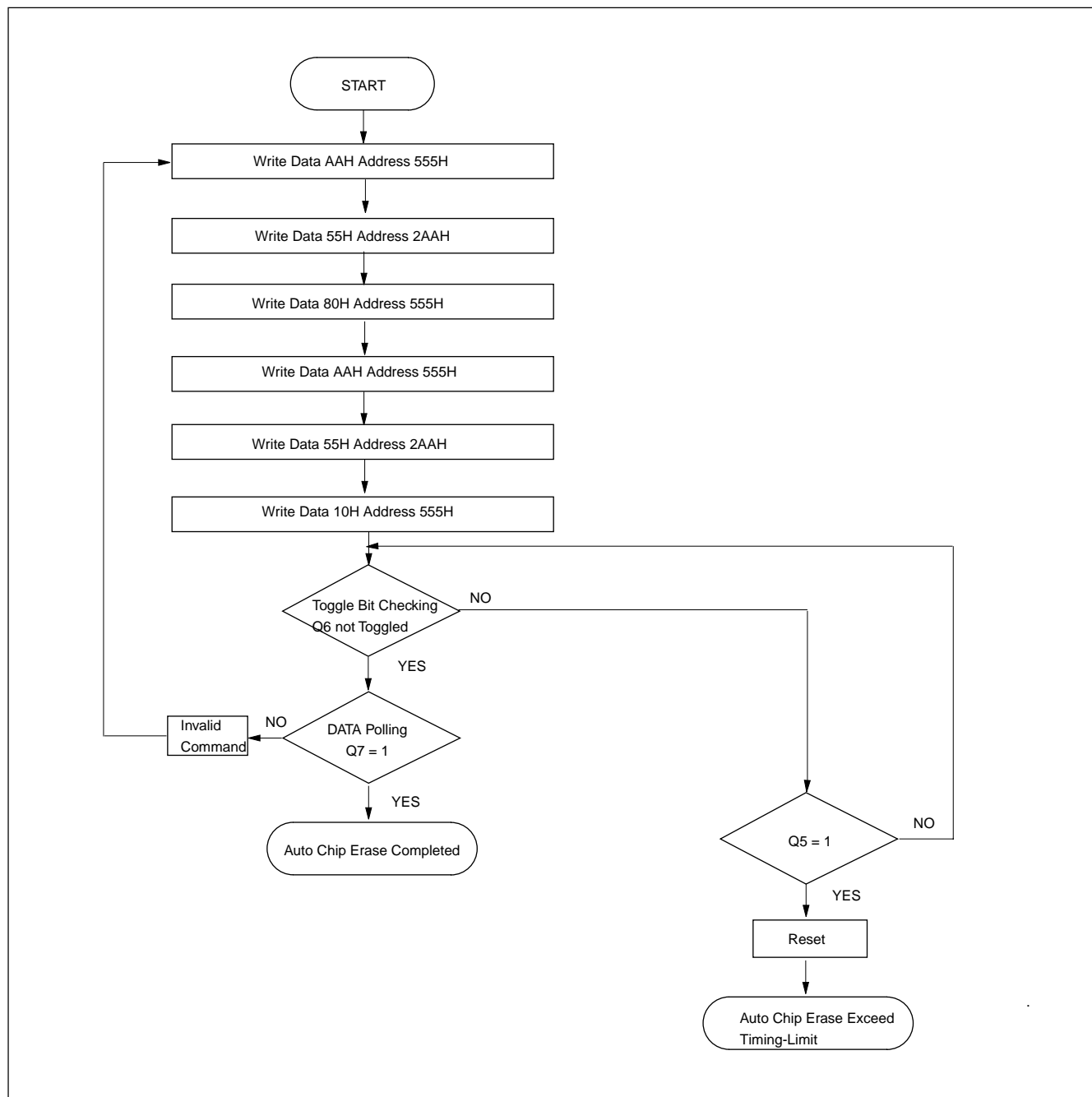
AUTOMATIC CHIP ERASE TIMING WAVEFORM

All data in chip are erased. External erase verification is not required because data is erased automatically by internal control circuit. Erasure completion can be verified by DATA polling and toggle bit checking after

automatic erase starts. Device outputs "0" during erasure and 1 after erasure on Q7. (Q6 is for toggle bit; see toggle bit, DATA polling, timing waveform)

AUTOMATIC CHIP ERASE TIMING WAVEFORM



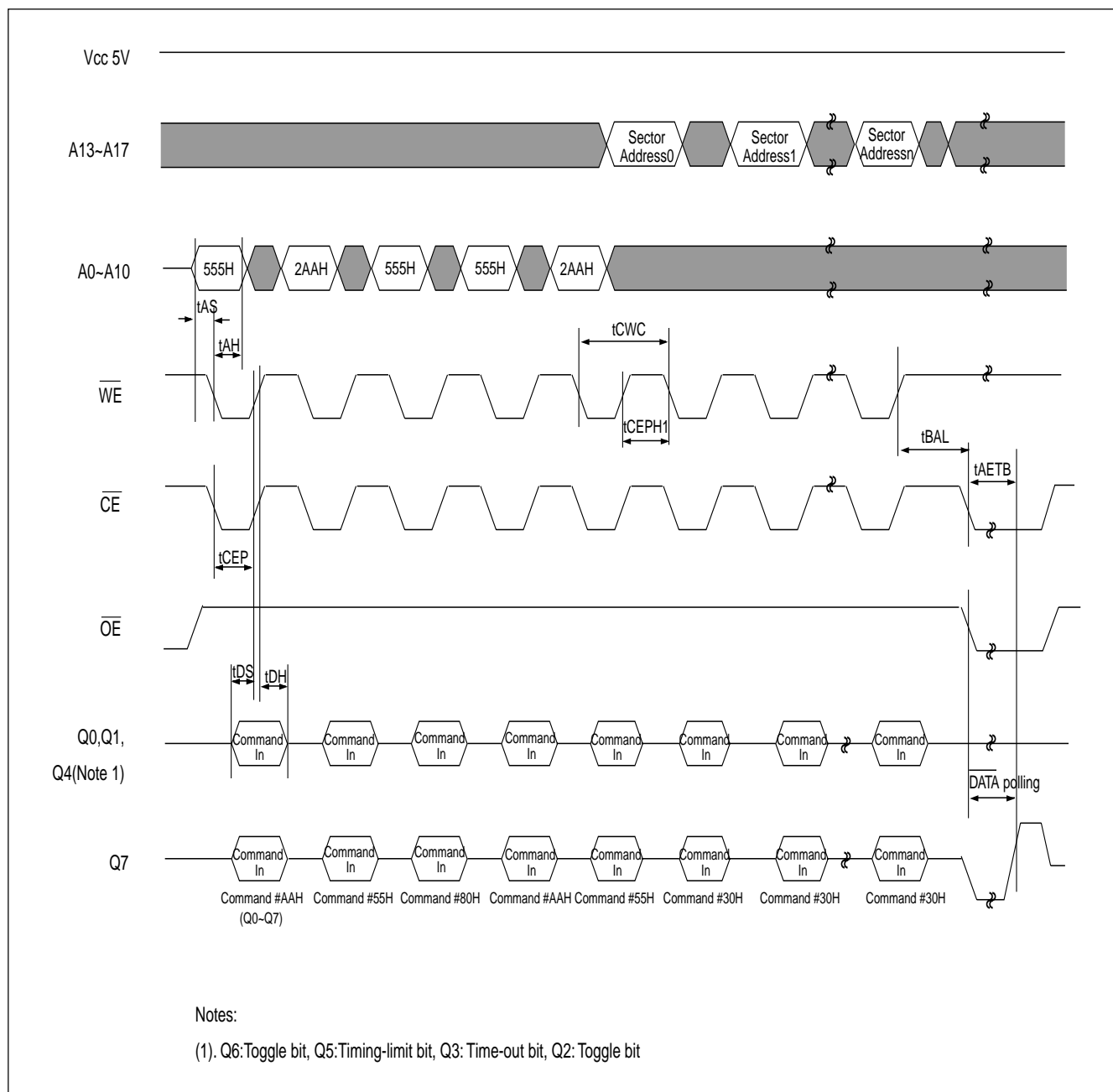
AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART


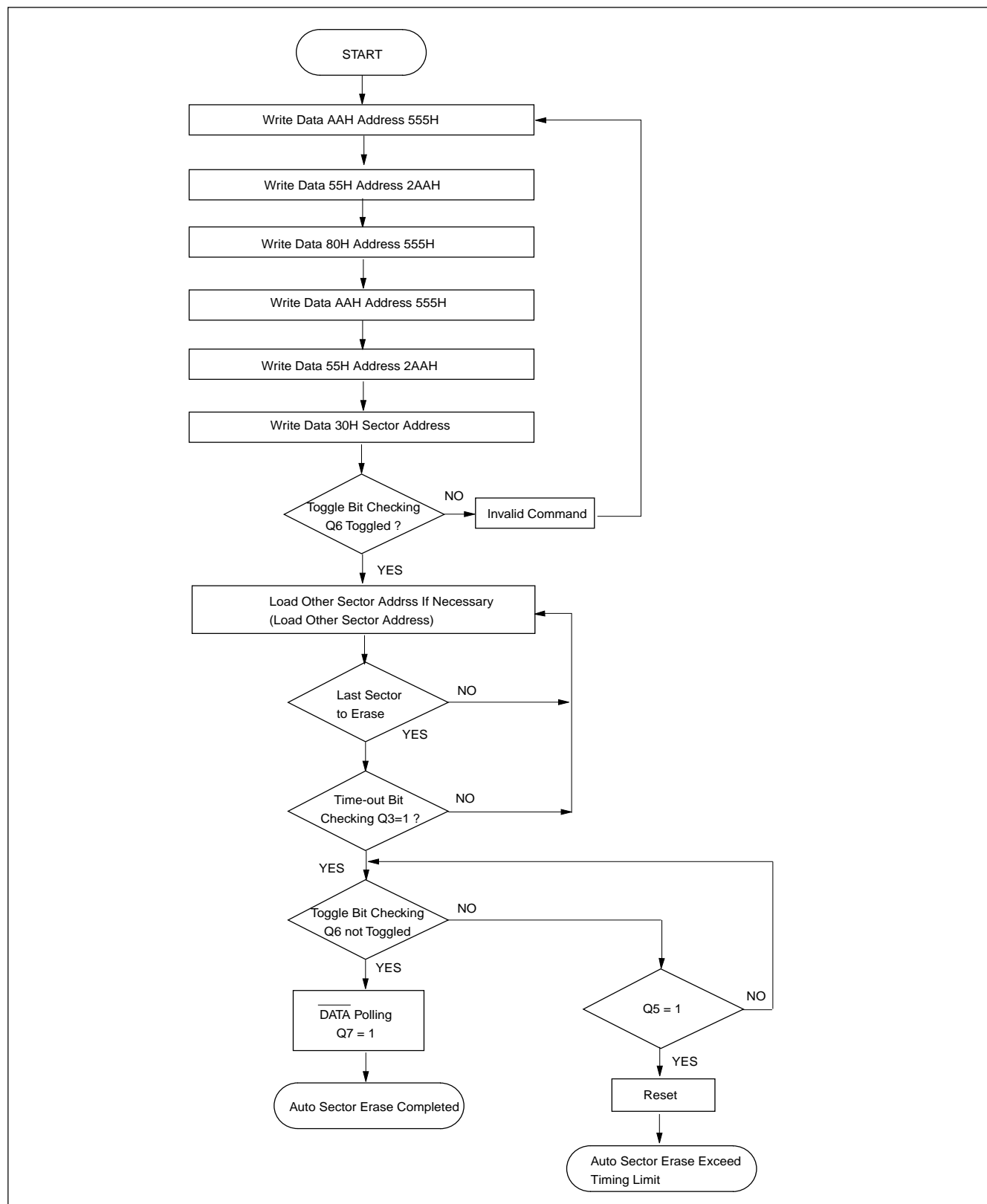
AUTOMATIC SECTOR ERASE TIMING WAVEFORM

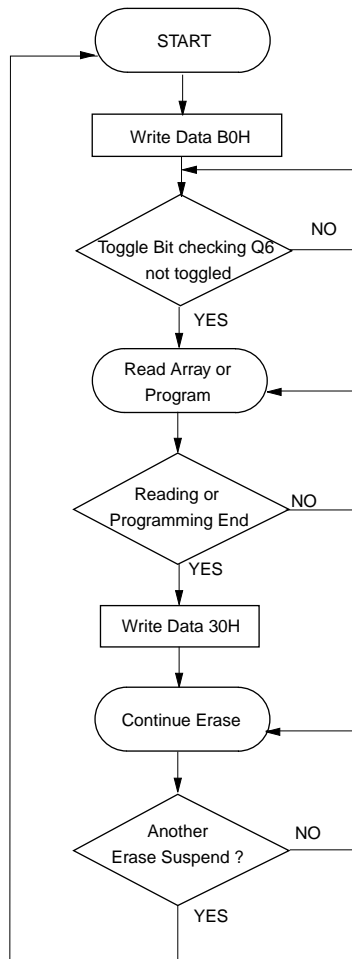
Sector data indicated by A13 to A17 are erased. External erase verification is not required because data are erased automatically by internal control circuit. Erasure completion can be verified by DATA polling and toggle bit

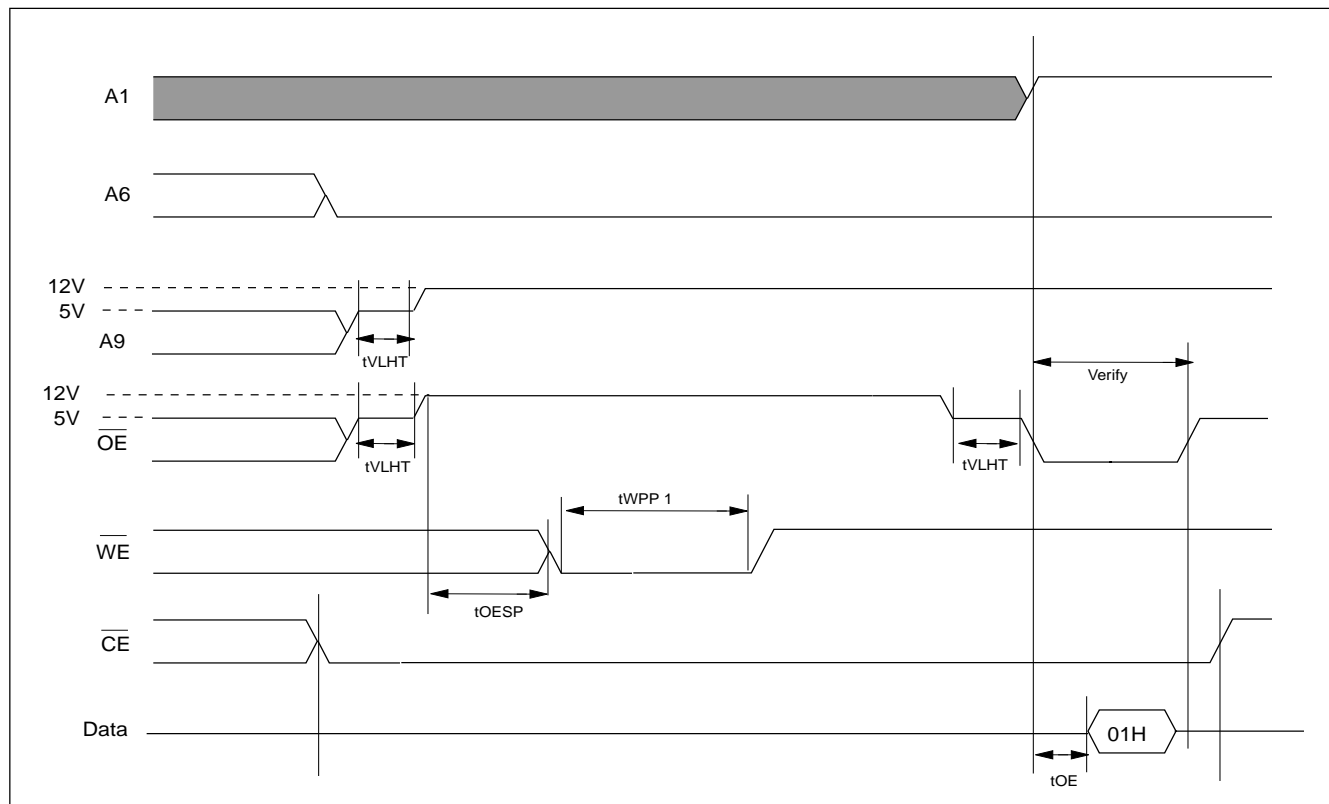
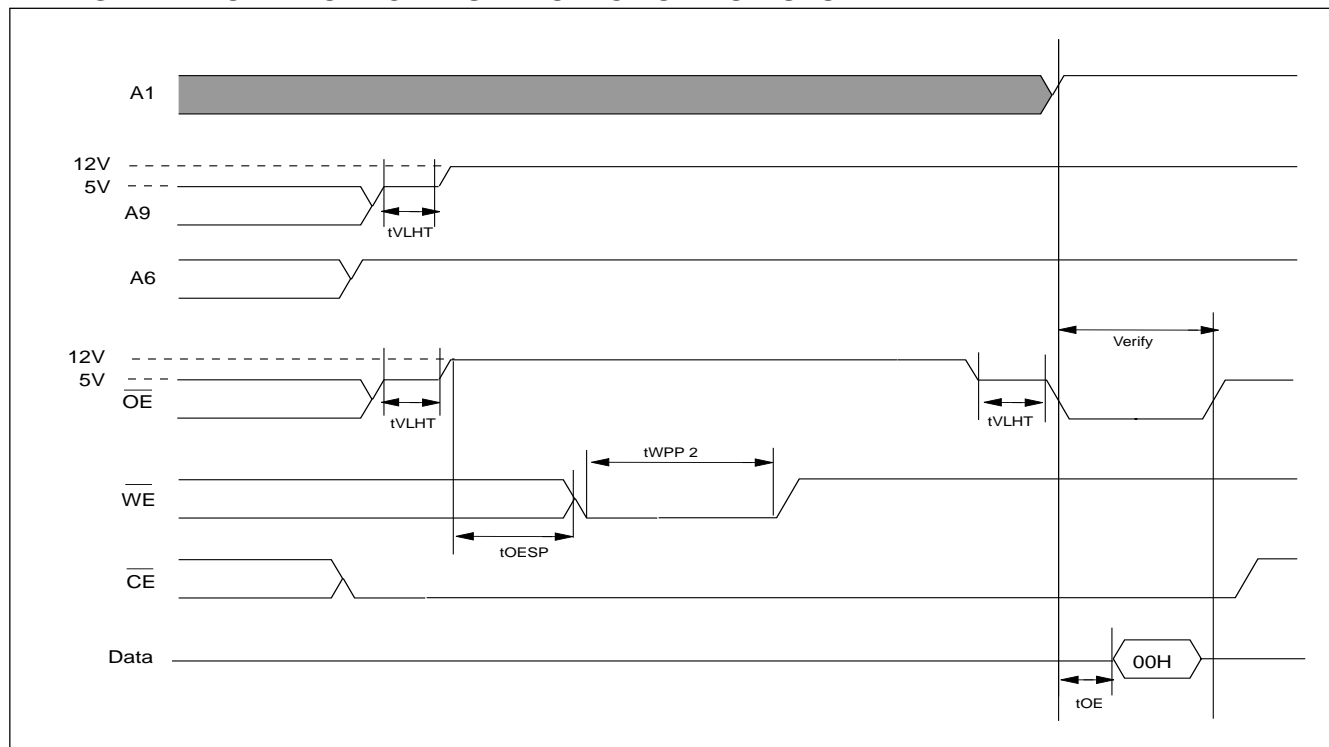
checking after automatic erase starts. Device outputs 0 during erasure and 1 after erasure on Q7. (Q6 is for toggle bit; see toggle bit, DATA polling, timing waveform)

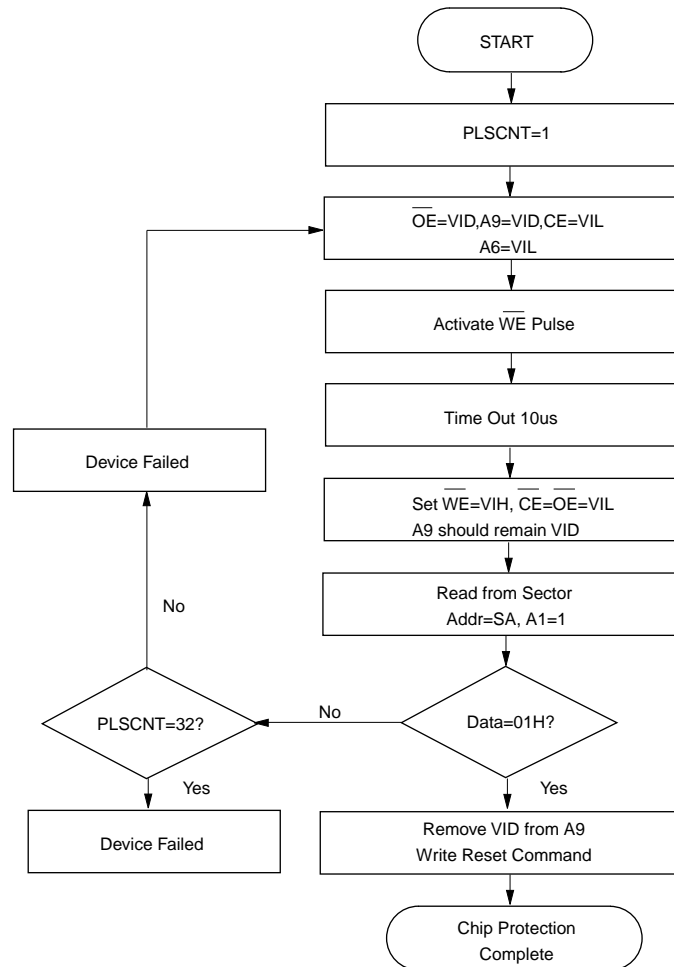
AUTOMATIC SECTOR ERASE TIMING WAVEFORM

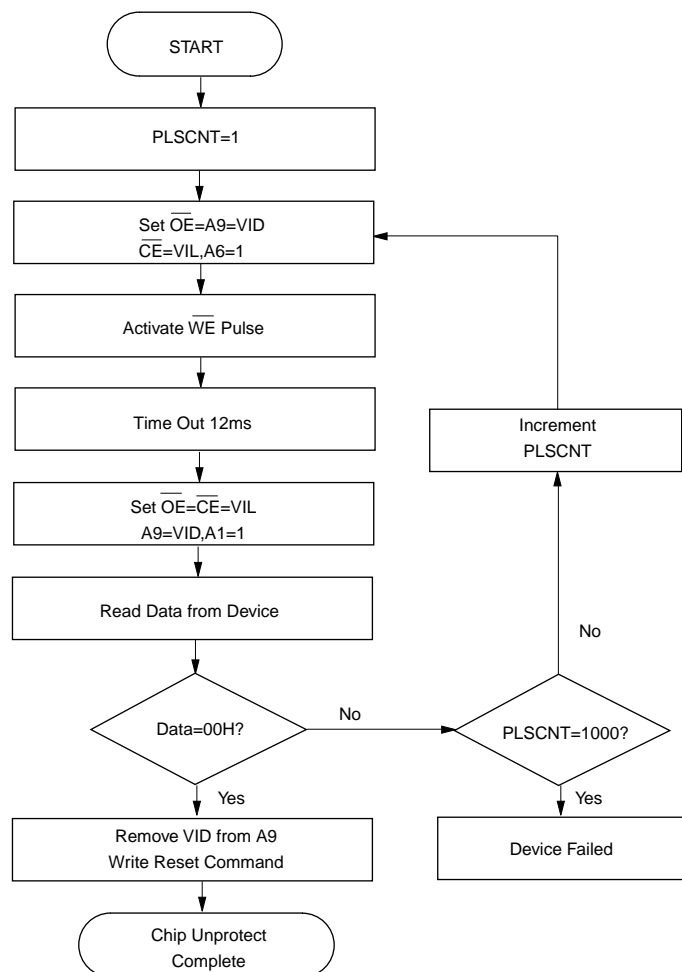


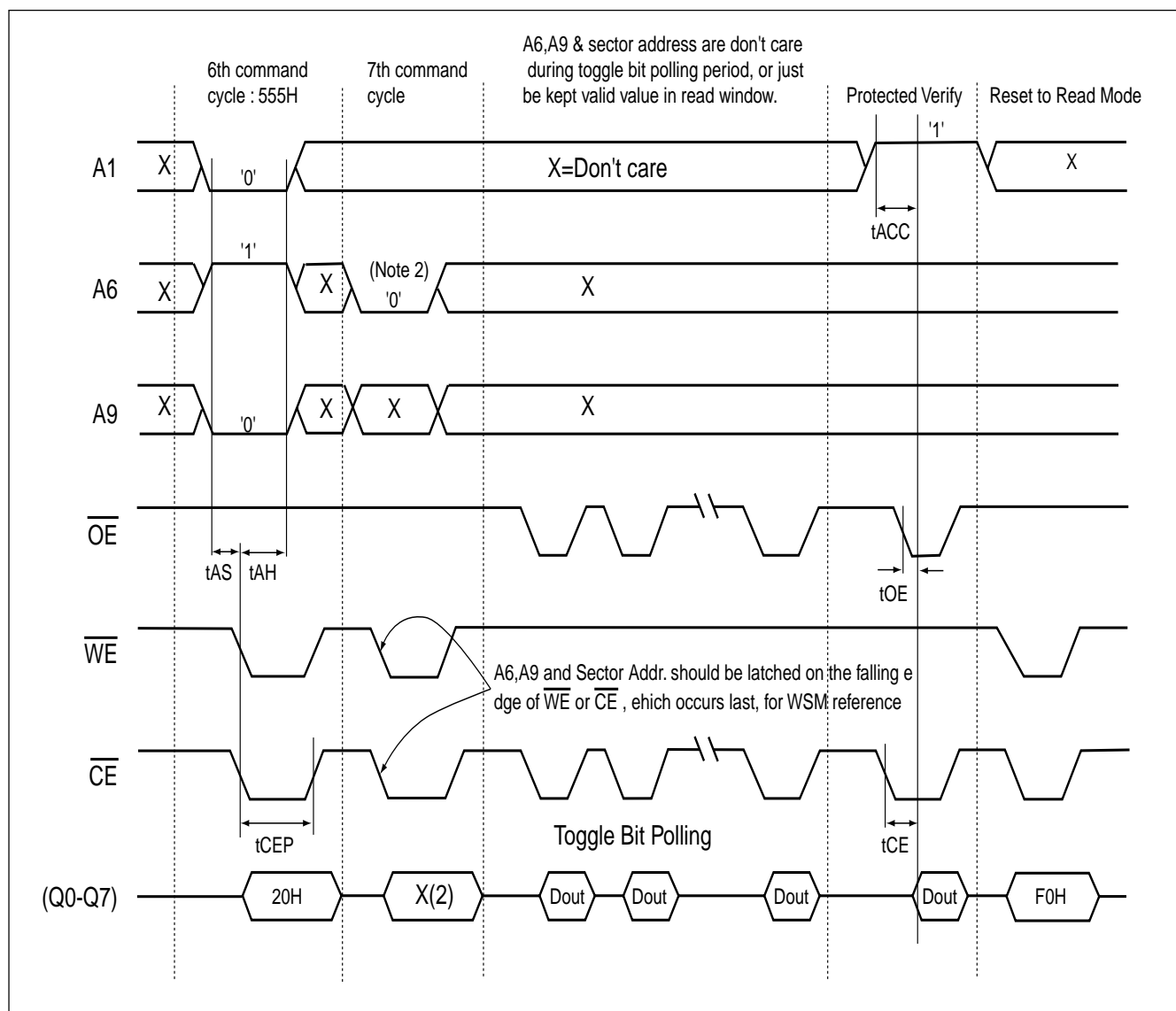
AUTOMATIC SECTOR ERASE ALGORITHM FLOWCHART


ERASE SUSPEND/ERASE RESUME FLOWCHART

TIMING WAVEFORM FOR CHIP PROTECTION FOR SYSTEM WITH 12V

TIMING WAVEFORM FOR CHIP UNPROTECTION FOR SYSTEM WITH 12V


CHIP PROTECTION ALGORITHM FOR SYSTEM WITH 12V


CHIP UNPROTECTION ALGORITHM FOR SYSTEM WITH 12V


TIMING WAVEFORM FOR CHIP PROTECTION/UNPROTECTION FOR SYSTEM WITHOUT 12V


Note1: Don't care except F0H.

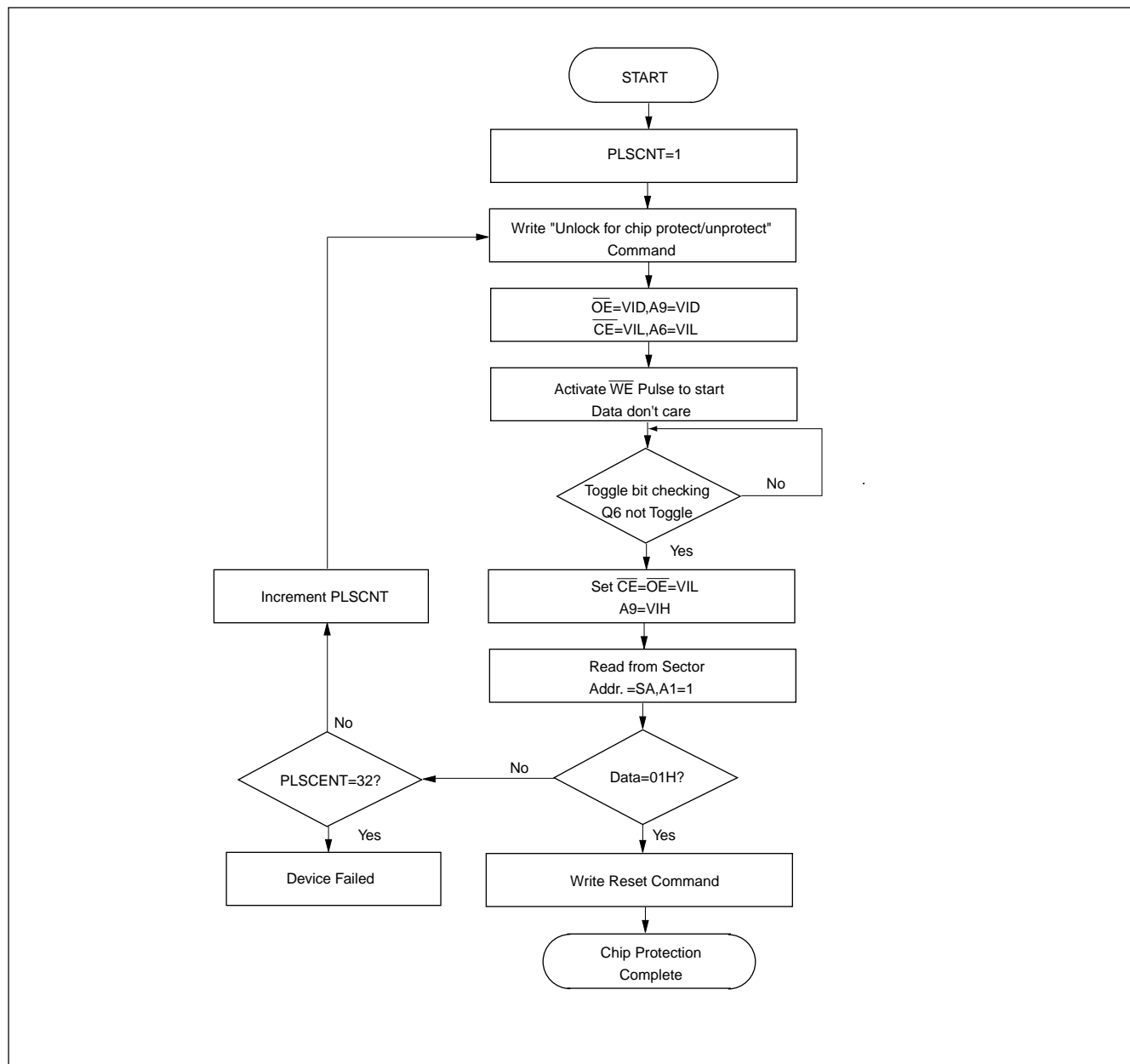
Note2: Protection: 7th command cycle A6 goes low.

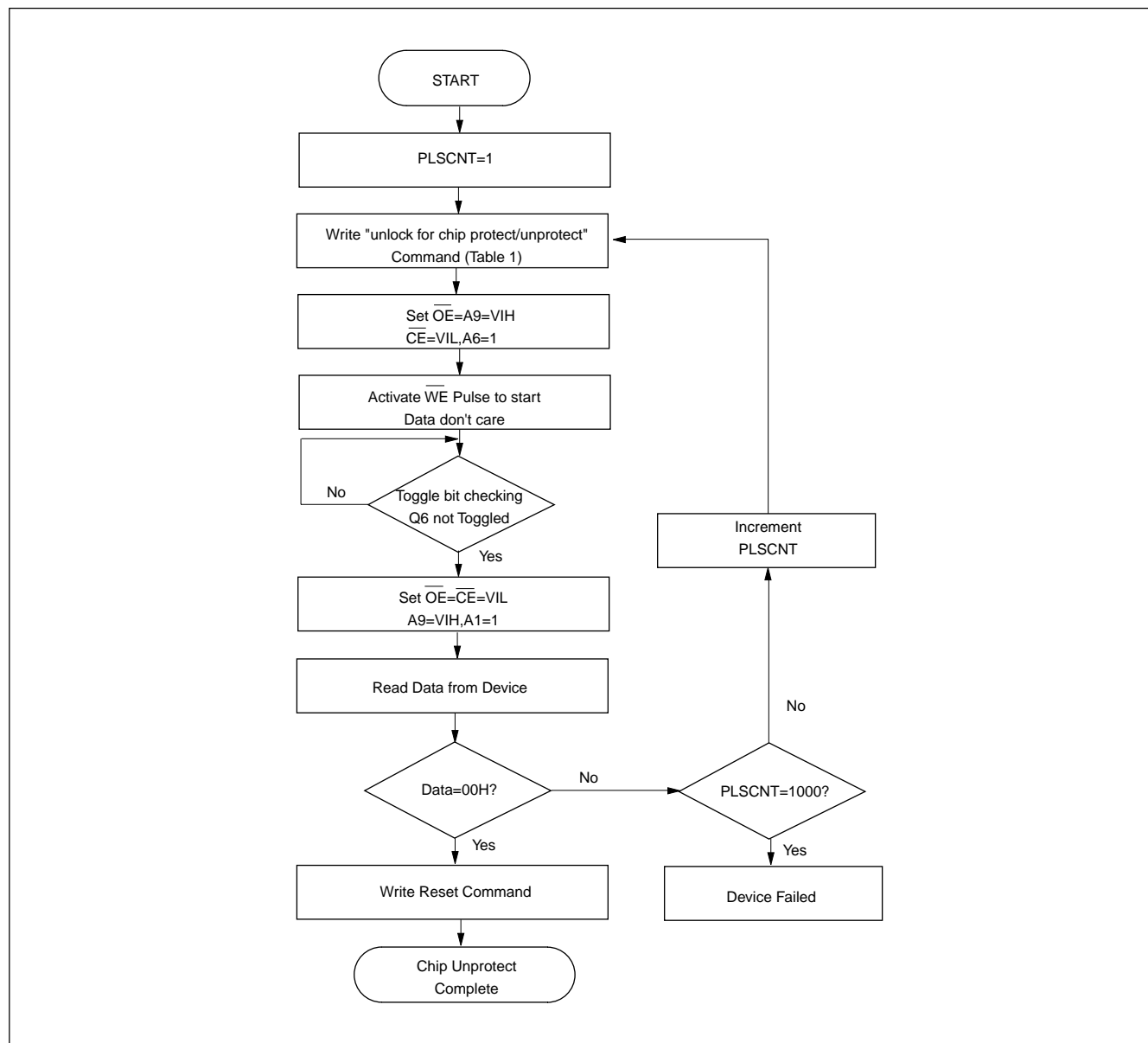
Unprotection: 7th command cycle A6 goes high.

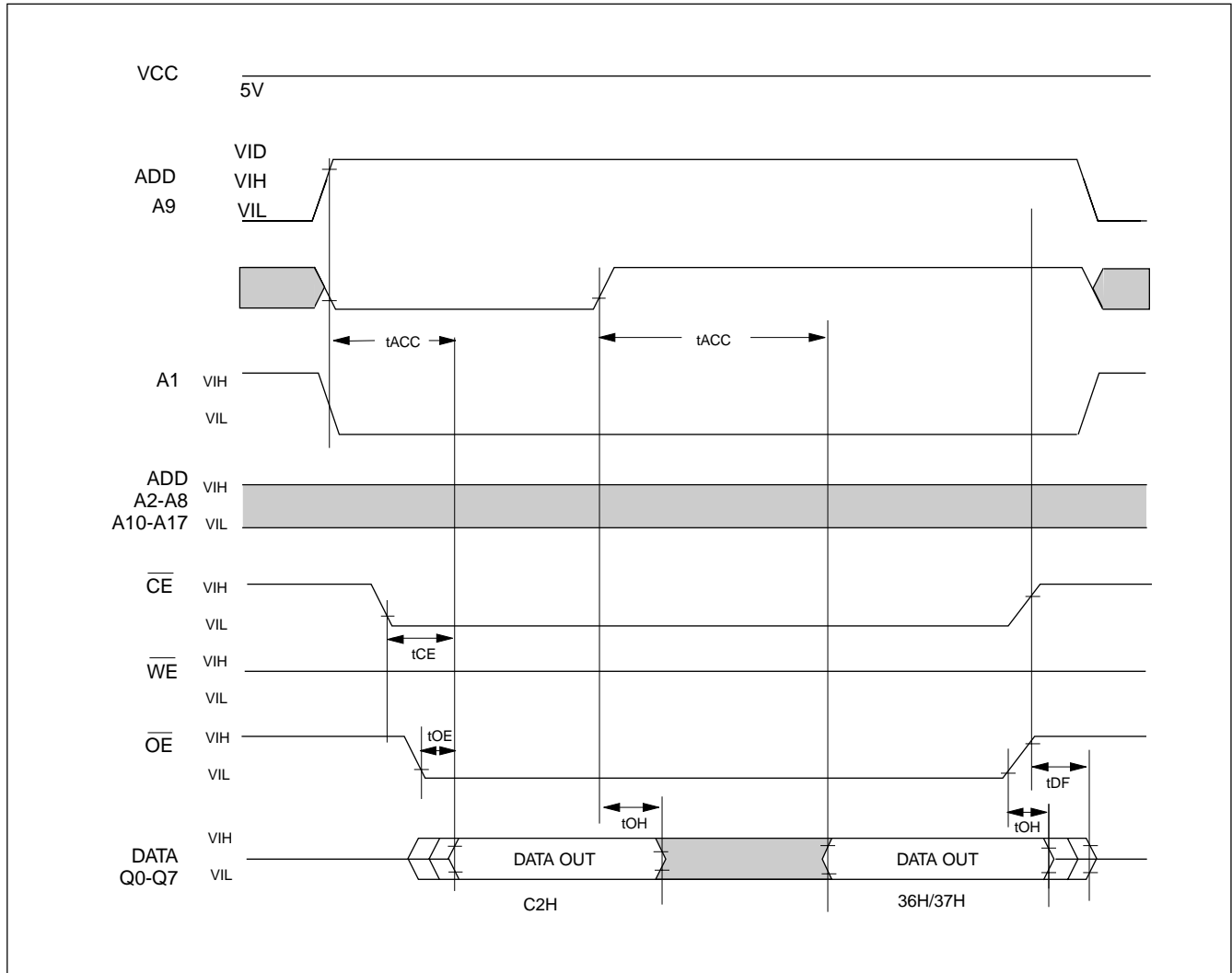
Note3: Protection verify: 01H

Un-protection verify: 00H

Note4: Must issue "unlock for chip protection/unprotection" command before chip protection/un-protection for a system without 12V provided.

CHIP PROTECTION ALGORITHM FOR SYSTEM WITHOUT 12V


CHIP UNPROTECTION ALGORITHM FOR SYSTEM WITHOUT 12V


ID CODE READ TIMING WAVEFORM MODE


ORDERING INFORMATION
PLASTIC PACKAGE

PART NO.	ACCESS TIME (ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(uA)	PACKAGE
MX29F022TPC-55	55	30	5	32 Pin PDIP
MX29F022TPC-70	70	30	5	32 Pin PDIP
MX29F022TPC-90	90	30	5	32 Pin PDIP
MX29F022TPC-12	120	30	5	32 Pin PDIP
MX29F022TTC-55	55	30	5	32 Pin TSOP (Normal Type)
MX29F022TTC-70	70	30	5	32 Pin TSOP (Normal Type)
MX29F022TTC-90	90	30	5	32 Pin TSOP (Normal Type)
MX29F022TTC-12	120	30	5	32 Pin TSOP (Normal Type)
MX29F022TQC-55	55	30	5	32 Pin PLCC
MX29F022TQC-70	70	30	5	32 Pin PLCC
MX29F022TQC-90	90	30	5	32 Pin PLCC
MX29F022TQC-12	120	30	5	32 Pin PLCC
MX29F022BPC-55	55	30	5	32 Pin PDIP
MX29F022BPC-70	70	30	5	32 Pin PDIP
MX29F022BPC-90	90	30	5	32 Pin PDIP
MX29F022BPC-12	120	30	5	32 Pin PDIP
MX29F022BTC-55	55	30	5	32 Pin TSOP (Normal Type)
MX29F022BTC-70	70	30	5	32 Pin TSOP (Normal Type)
MX29F022BTC-90	90	30	5	32 Pin TSOP (Normal Type)
MX29F022BTC-12	120	30	5	32 Pin TSOP (Normal Type)
MX29F022BQC-70	70	30	5	32 Pin PLCC
MX29F022BQC-90	90	30	5	32 Pin PLCC
MX29F022BQC-12	120	30	5	32 Pin PLCC
MX29F022NTPC-55	55	30	5	32 Pin PDIP
MX29F022NTPC-70	70	30	5	32 Pin PDIP
MX29F022NTPC-90	90	30	5	32 Pin PDIP
MX29F022NTPC-12	120	30	5	32 Pin PDIP

PART NO.	ACCESS TIME (ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(uA)	PACKAGE
MX29F022NTTC-55	55	30	5	32 Pin TSOP (Normal Type)
MX29F022NTTC-70	70	30	5	32 Pin TSOP (Normal Type)
MX29F022NTTC-90	90	30	5	32 Pin TSOP (Normal Type)
MX29F022NTTC-12	120	30	5	32 Pin TSOP (Normal Type)
MX29F022NTQC-55	55	30	5	32 Pin PLCC
MX29F022NTQC-70	70	30	5	32 Pin PLCC
MX29F022NTQC-90	90	30	5	32 Pin PLCC
MX29F022NTQC-12	120	30	5	32 Pin PLCC
MX29F022NBPC-55	55	30	5	32 Pin PDIP
MX29F022NBPC-70	70	30	5	32 Pin PDIP
MX29F022NBPC-90	90	30	5	32 Pin PDIP
MX29F022NBPC-12	120	30	5	32 Pin PDIP
MX29F022NBTC-55	55	30	5	32 Pin TSOP (Normal Type)
MX29F022NBTC-70	70	30	5	32 Pin TSOP (Normal Type)
MX29F022NBTC-90	90	30	5	32 Pin TSOP (Normal Type)
MX29F022NBTC-12	120	30	5	32 Pin TSOP (Normal Type)
MX29F022NBQC-70	70	30	5	32 Pin PLCC
MX29F022NBQC-90	90	30	5	32 Pin PLCC
MX29F022NBQC-12	120	30	5	32 Pin PLCC

ERASE AND PROGRAMMING PERFORMANCE (1)

PARAMETER	LIMITS			UNITS
	MIN.	TYP.(2)	MAX.(3)	
Sector Erase Time		1	8	s
Chip Erase Time		3	24	s
Byte Programming Time		7	210	us
Chip Programming Time		3.5	10.5	sec
Erase/Program Cycles	100,000			Cycles

Note: 1.Not 100% Tested, Excludes external system level over head.

2.Typical values measured at 25° C,5V.

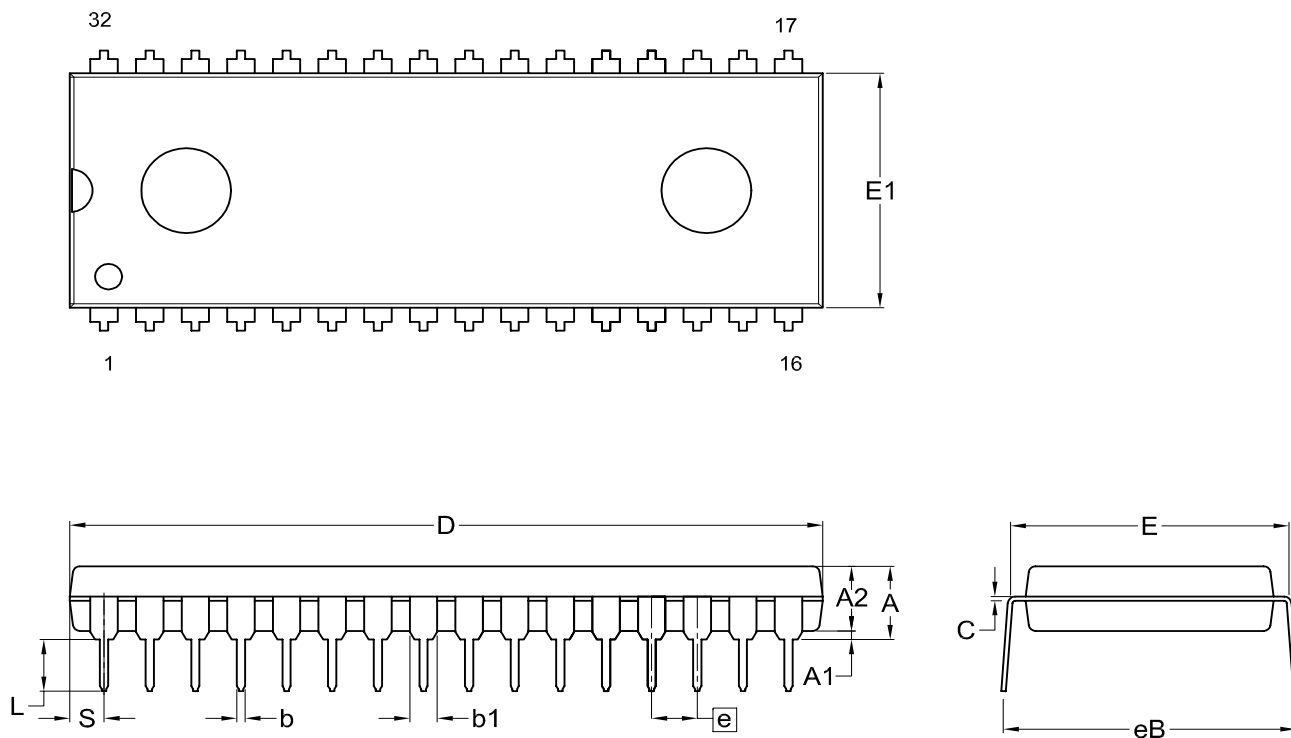
3.Maximum value measured at 25° C,4.5V.

LATCH-UP CHARACTERISTICS

	MIN.	MAX.
Input Voltage with respect to GND on all pins except I/O pins	-1.0V	13.5V
Input Voltage with respect to GND on all I/O pins	-1.0V	Vcc + 1.0V
Current	-100mA	+100mA
Includes all pins except Vcc. Test conditions: Vcc = 5.0V, one pin at a time.		

DATA RETENTION

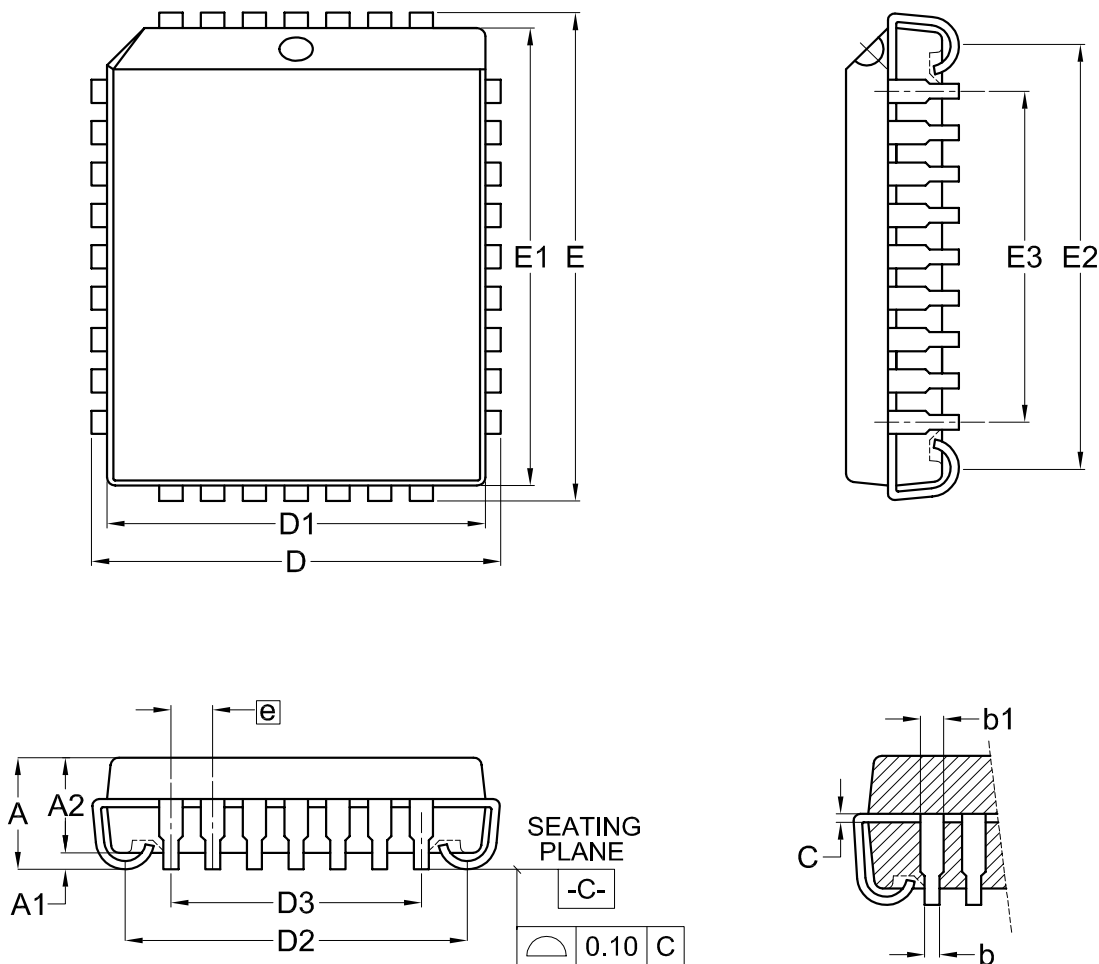
PARAMETER	MIN.	UNIT
Data Retention Time	20	Years

PACKAGE INFORMATION
Title: Package Outline for PDIP 32L(600MIL)


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL UNIT		A	A1	A2	b	b1	C	D	E	E1	e	eB	L	S
mm	Min.	---	0.38	3.73	0.38	1.14	0.20	41.78	15.11	13.84		15.75	2.92	1.65
	Nom.	---	---	3.94	0.46	1.27	0.25	41.91	15.24	13.97	2.54	16.51	3.30	1.90
	Max.	4.90	0.76	4.14	0.53	1.40	0.30	42.04	15.37	14.10		17.27	3.68	2.16
Inch	Min.	---	0.015	0.147	0.015	0.045	0.008	1.645	0.595	0.545		0.620	0.115	0.065
	Nom.	---	---	0.155	0.018	0.050	0.010	1.650	0.600	0.550	0.100	0.650	0.130	0.075
	Max.	0.193	0.030	0.163	0.021	0.055	0.012	1.655	0.605	0.555		0.680	0.145	0.085

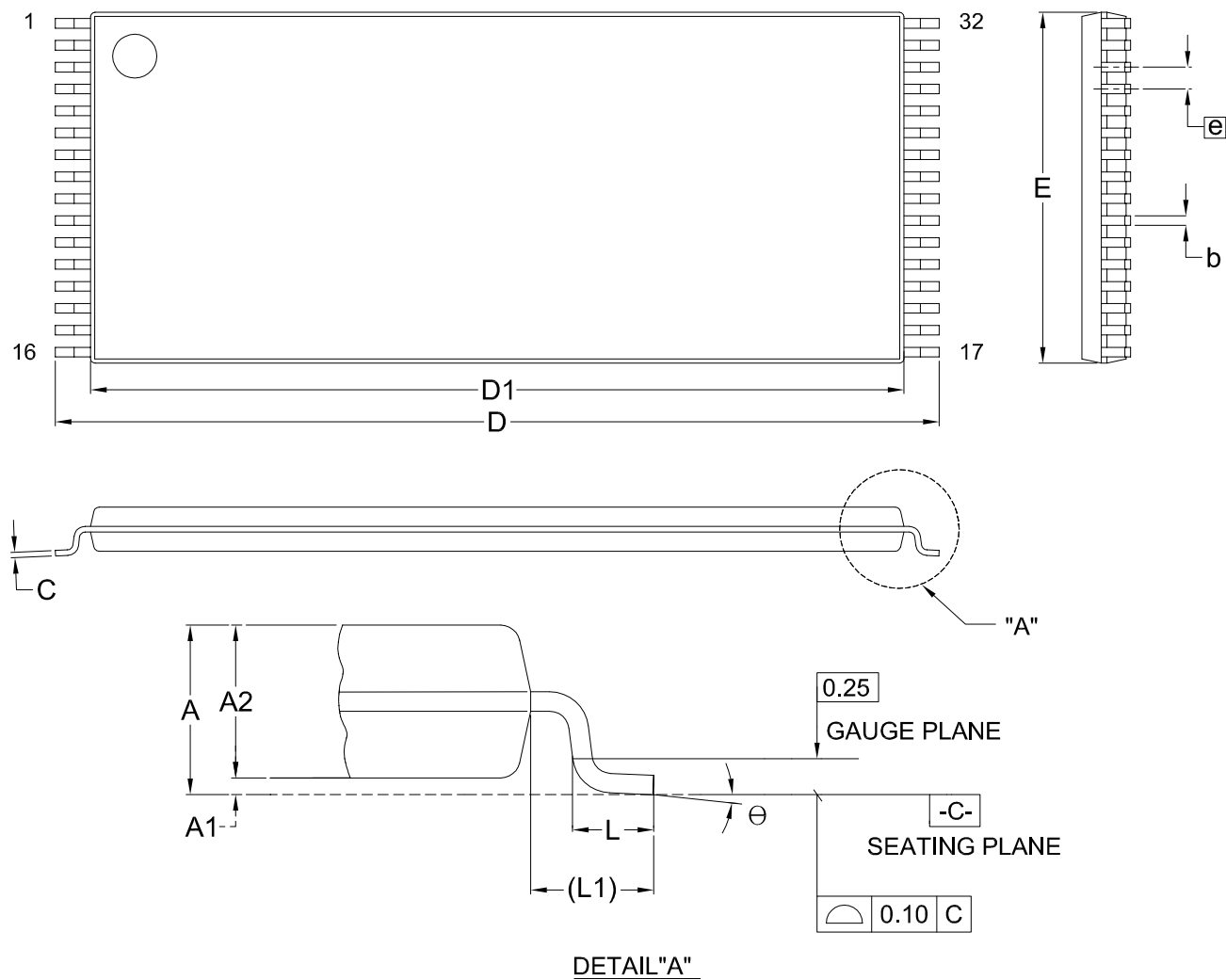
DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-0202.2	7				11-24-'03

Title: Package Outline for 32L PLCC


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL		A	A1	A2	b	b1	C	D	D1	D2	D3	E	E1	E2	E3	e
UNIT																
mm	Min.	---	0.38	2.69	0.38	0.61	0.20	12.32	11.36	10.11		14.86	13.98	12.65		
	Nom.	---	0.58	2.79	0.46	0.71	0.25	12.45	11.43	10.41	7.62	14.99	14.05	12.95	10.16	1.27
	Max.	3.55	0.81	2.89	0.54	0.81	0.30	12.58	11.50	10.71		15.12	14.12	13.25		
Inch	Min.	---	0.015	0.106	0.015	0.024	0.008	0.485	0.447	0.398		0.585	0.550	0.498		
	Nom.	---	0.023	0.110	0.018	0.028	0.010	0.490	0.450	0.410	0.300	0.590	0.553	0.510	0.400	0.050
	Max.	0.140	0.032	0.114	0.021	0.032	0.012	0.495	0.453	0.422		0.595	0.556	0.522		

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-2002	7	MS-016			12-10-'03

Title: Package Outline for TSOP(I) 32L (8X20mm)


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL		A	A1	A2	b	C	D	D1	E	e	L	L1	θ
UNIT													
mm	Min.	---	0.05	0.95	0.17	0.10	19.80	18.30	7.90		0.50	0.70	0
	Nom.	---	0.10	1.00	0.20	0.15	20.00	18.40	8.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	8.10		0.70	0.90	8
Inch	Min.	---	0.002	0.037	0.007	0.004	0.780	0.720	0.311		0.020	0.028	0
	Nom.	---	0.004	0.039	0.008	0.006	0.787	0.724	0.315	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.319		0.028	0.035	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1604	9	MO-142			11-26-'03

REVISION HISTORY

Revision	Description	Page	Date
1.0	1.To remove "Advanced Information" data sheet marking and contain information on products in full production	P1	DEC/21/1999
	2.The modification summary of Revision 0.9.4 to Revision 1.0:		
	2-1.Program/erase cycle times:10K cycles-->100K cycles	P1,41	
	2-2.To add data retention 20 years	P1,41	
	2-3.To remove A9 from the timing waveform of protection/unprotection without 12V	P35	
	2-4.Multi-sector erase time-out:30ms-->30us,	P8	
	2-5.tBAL:80us-->100us	P21	
1.1	To modify "Package Information"	P42~44	JUN/14/2001
1.2	1. To correct typing error	All	JUN/11/2002
1.3	1. To change part no. from MX29F022/022N to MX29F022/022NT/B	All	NOV/11/2002



MX29F022/022NT/B

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