



MIC1232

μ P Supervisory Circuit

Description

The MIC1232 is a multifunction circuit which monitors microprocessor activity, external reset and power supplies in microprocessor based systems. The circuit functions include a watchdog timer, power supply monitor, microprocessor reset, and manual pushbutton reset input.

The power supply line is monitored with a comparator and an internal voltage reference. \overline{RST} is forced low when an out-of-tolerance condition exists and remains asserted for at least 250ms after V_{CC} rises above the threshold voltage (4.5V or 4.75V). The \overline{RST} pin will remain logic low with V_{CC} as low as 1.4V.

The Watchdog input (\overline{ST}) monitors μ P activity and will assert \overline{RST} if no μ P activity has occurred within the watchdog timeout period. The watchdog timeout period is selectable with nominal periods of 150, 600, or 1200 milliseconds.

Typical Applications

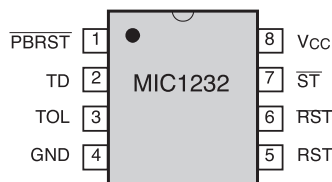
- Automotive Systems
- Intelligent Instruments
- Critical Microprocessor Power Monitoring
- Battery Powered Computers
- Controllers

Ordering Information

Part	Package	Temp. Range
MIC1232N	8-Lead PDIP	-40°C to +85°C
MIC1232M	8-Lead SOIC	-40°C to +85°C

Pin Configuration

Top View

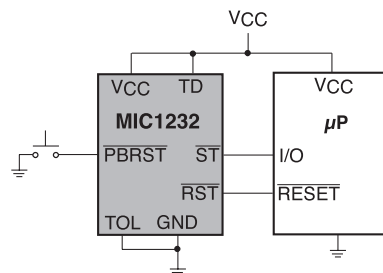


MIC1232N - 8 Lead Plastic DIP Package
MIC1232M - 8 Lead Plastic SOIC Package

Features

- Power OK/Reset Time Delay, 250ms min.
- Watchdog Timer, 150ms, 600ms, or 1.2s typical
- Precision Supply Voltage Monitor, Select Between 5% or 10% of Supply Voltage
- Available in 8-pin Surface Mount (SO)
- Debounced External Reset Input
- Low Supply Current, < 18 μ A Typ.

Typical Operating Circuit



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Absolute Maximum Ratings

Terminal Voltage
VCC, -0.3V to 6.0V
All Other Inputs -0.3V to (VCC + 0.3V)
Input Current
VCC 250mA
Gnd, All Other Inputs 25mA

Operating Temperature Range

MIC1232M/N -40°C to 85°C
MIC1232D 0°C to 70°C
Storage Temperature Range -65°C to 150°C
Lead Temperature (Soldering - 10 sec.) 300°C
Power Dissipation 700mW

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability. Operating ranges define those limits between which the functionality of the device is guaranteed.

Electrical Characteristics

VCC = 4.5V to 5.5V, T_A = Operating Temperature Range, unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage Range	VCC	4.5		5.5	V
Supply Current	ICC (See Note 1)		18	40	μ A
\overline{ST} and \overline{PBRST} Input Levels	V _{IH} (See Note 2) V _{IL}	2.0 -0.3		V _{CC} +0.3 0.8	V
Input Leakage	I _{IL}			± 1	μ A
Output Source Current, RST	V _{OH} = 2.4V	1.0	10		mA
Output Sink Current, \overline{RST} , RST	V _{OL} = 0.4V	2.0	10		mA
VCC 5% Trip Point (Reset Threshold Voltage)	TOL = Gnd	4.50	4.62	4.74	V
VCC 10% Trip Point (Reset Threshold Voltage)	TOL = VCC	4.25	4.37	4.49	V
Input Capacitance, \overline{ST} , TOL	C _{IN} (See Note 3)			5	pF
Output Capacitance, \overline{RST} , RST	C _{OUT} (See Note 3)			7	pF

A.C. Electrical Characteristics

VCC = 4.5V to 5.5V, T_A = Operating Temperature Range, unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units
$\overline{\text{PBRST}}$ Min. Pulse Width, t _{PB}	$\overline{\text{PBRST}} = \text{V}_{\text{IL}}$ (see note 4)	20			ms
$\overline{\text{PBRST}}$ Delay, t _{PBD}		1	4	20	ms
Reset Active Time, t _{RST}		250	610	1000	ms
$\overline{\text{ST}}$ Pulse Width, t _{ST}		20			ns
$\overline{\text{ST}}$ Timeout Period, t _{TD}	TD = 0V TD = Open TD = VCC	62.5 250 500	150 600 1200	250 1000 2000	ms
VCC Fall Time, t _F		10			μ s
VCC Rise Time, t _R		0			ns
VCC Detect to $\overline{\text{RST}}$ Low and RST High, t _{RPD}	VCC Falling (see note 5)		50	150	μ s
VCC Detect to $\overline{\text{RST}}$ Open and RST Low, t _{RPU}	VCC Rising (see note 6)	250	610	1000	ms

Note 1: I_{CC} is measured with outputs open and inputs within 0.5V of supply rails.

Note 2: $\overline{\text{PBRST}}$ has an internal pull-up resistor to VCC (typ. 40k Ω).

Note 3: Guaranteed by design.

Note 4: $\overline{\text{PBRST}}$ must be held low for a minimum of 20ms to guarantee a reset.

Note 5: VCC falling at 1.66mV/ μ s.

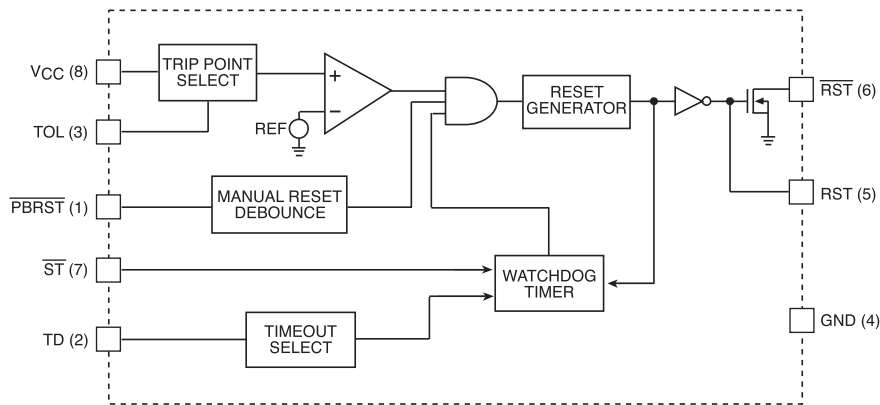
Note 6: $\overline{\text{RST}}$ has an open drain output.

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Pin Functions

- Pin 1: **$\overline{\text{PBRST}}$** - Pushbutton reset input. This input is debounced and can be driven with external logic signals or by means of a mechanical pushbutton to actively force a reset. All pulses less than 1ms in duration on the $\overline{\text{PBRST}}$ pin are ignored, whereas, any pulse with a duration of 20ms or greater is guaranteed to cause a reset.
- Pin 2: **TD** - Time delay input. This input selects the timebase used by the watchdog timer. When TD = 0V, the watchdog timeout period is set to a nominal value of 150ms, when TD = open, the watchdog timeout period is set to a nominal value of 600ms and when TD = V_{CC} , the watchdog timeout period is 1.2sec nominally.
- Pin 3: **TOL** - Tolerance select input. Selects whether 5% or 10% of V_{CC} is used as the reset threshold voltage. When TOL = 0V, the 5% tolerance level is selected and when TOL = V_{CC} , a 10% tolerance level is selected.
- Pin 4: **GND** - IC ground pin, 0V reference.
- Pin 5: **RST** - RST is asserted high if either V_{CC} goes below the reset threshold, the watchdog times out or $\overline{\text{PBRST}}$ is pulled low for a minimum of 20ms. RST remains asserted for one reset timeout period after V_{CC} exceeds the reset threshold or after the watchdog times out or after $\overline{\text{PBRST}}$ goes high.
- Pin 6: **$\overline{\text{RST}}$** - $\overline{\text{RST}}$ is asserted low if either V_{CC} goes below the reset threshold, the watchdog times out or $\overline{\text{PBRST}}$ is pulled low for a minimum of 20ms. $\overline{\text{RST}}$ remains asserted for one reset timeout period after V_{CC} exceeds the reset threshold or after the watchdog times out or after $\overline{\text{PBRST}}$ goes high. Open-drain output.
- Pin 7: **$\overline{\text{ST}}$** - Input to the watchdog timer. If $\overline{\text{ST}}$ does not see a transition from high to low within the watchdog timeout period, RST and $\overline{\text{RST}}$ will be asserted.
- Pin 8: **V_{CC}** - Primary supply input, +5V.

Block Diagram



Circuit Description

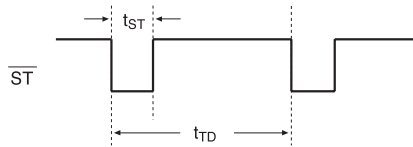
TD Pin	Min.	t _{TD} Typ.	Max.
Gnd	62.5ms	150ms	250ms
Open	250ms	600ms	1000ms
VCC	500ms	1200ms	2000ms

Table 1. Watchdog Timeout Period

Circuit Description

Power Monitor

The $\overline{\text{RST}}$ and RST pins are asserted whenever VCC falls below the reset threshold voltage as determined by the TOL pin. A 5% tolerance level (4.62V reset threshold voltage) can be selected by connecting the TOL pin to ground and a 10% tolerance (4.37V reset threshold voltage) can be selected by connecting the TOL pin to VCC. The reset pins will remain asserted for a period of 250ms after VCC has risen above the reset threshold voltage. The reset function ensures the microprocessor is properly reset and powers up into a known condition after a power failure. $\overline{\text{RST}}$ will remain valid with VCC as low as 1.4V.



Note: The maximum time between high-to-low transitions (t_{TD}) on the watchdog input (ST) is determined by the voltage applied to the TD pin. If the watchdog input sees a high-to-low transition prior to the timeout period, the watchdog timer will be reset.

Figure 2. Watchdog Input

Pushbutton Reset Input

The $\overline{\text{PBRST}}$ input can be driven with a manual pushbutton switch or with external logic signals. The input is internally debounced and requires an active low signal to force the reset outputs into their active states. The $\overline{\text{PBRST}}$ input will recognize any pulse that is 20ms in duration or greater and will ignore all pulses that are less than 1ms in duration.

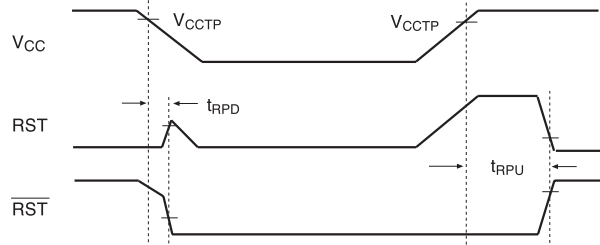


Figure 1. Power-Up/Power-Down Sequence

Watchdog Timer

The microprocessor can be monitored by connecting the $\overline{\text{ST}}$ pin (watchdog input) to a bus line or I/O line. If a high-to-low transition doesn't occur on the $\overline{\text{ST}}$ pin within the watchdog timeout period (determined by TD pin, see Table 1), the $\overline{\text{RST}}$ and RST pins will be asserted resulting in a microprocessor reset. $\overline{\text{RST}}$ and RST will remain asserted for 250ms when this occurs. A minimum pulse of 75ns or any transition high-to-low on the $\overline{\text{ST}}$ pin will reset the watchdog timer. The watchdog timer will be reset if $\overline{\text{ST}}$ sees a valid transition within the watchdog timeout period.

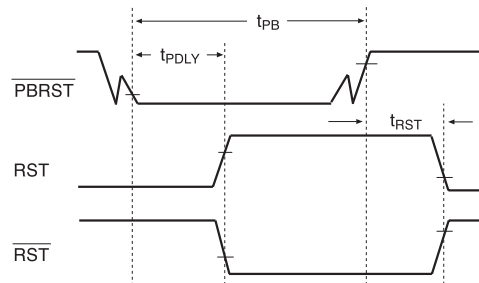


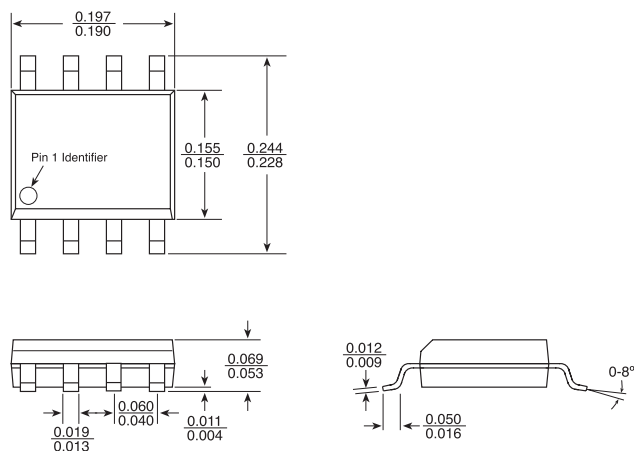
Figure 3. Pushbutton Reset

Alternate Source Cross Reference Guide

<u>Industry P/N</u>	<u>MIC Direct Replacement</u>
DS1232LP	MIC1232N
DS1232LPS-2	MIC1232M
DS1232	MIC1232N
DS1232LPN	MIC1232N
DS1232LPSN-2	MIC1232M
DS1232N	MIC1232N
MAX1232CPA	MIC1232N
MAX1232CSA	MIC1232M
MAX1232EPA	MIC1232N
MAX1232ESA	MIC1232M
MAX1232C/D	MIC1232D

Packaging Information

M Package, 8-Pin Small Outline



N Package, 8-Pin Plastic Dual-In-Line

