

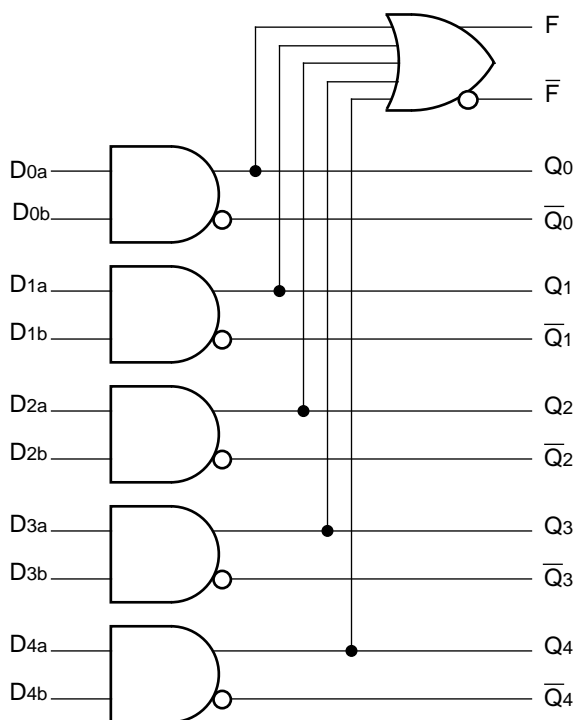
FEATURES

- 600ps max. propagation delay
- Extended 100E VEE range of -4.2V to -5.5V
- True and complementary outputs
- OR/NOR function outputs
- Fully compatible with Industry standard 10KH, 100K I/O levels
- Internal 75KΩ input pulldown resistors
- Fully compatible with Motorola MC10E/100E104
- Available in 28-pin PLCC package

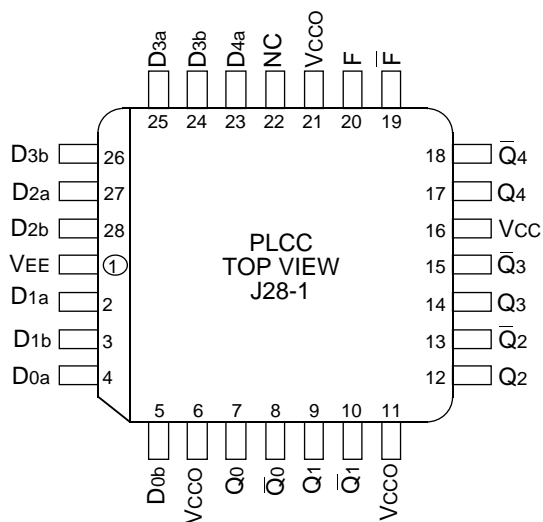
DESCRIPTION

The SY10/100E104 are quint 2-input AND/NAND gates designed for use in new, high-performance ECL systems. The E104 also features a function output, F, which is the OR of all five AND gate outputs, while \bar{F} is the NOR. Both true and complementary outputs are provided.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin	Function
Dna, Dnb	Data Inputs
Q0-Q4	AND Outputs
$\bar{Q}0-\bar{Q}4$	NAND Outputs
F	OR Output
\bar{F}	NOR Output
Vcco	Vcc to Output

LOGIC EQUATION

$$F = (D0a \cdot D0b) + (D1a \cdot D1b) + (D2a \cdot D2b) + (D3a \cdot D3b) + (D4a \cdot D4b)$$

DC ELECTRICAL CHARACTERISTICS

$V_{EE} = V_{EE} (\text{Min.})$ to $V_{EE} (\text{Max.})$; $V_{CC} = V_{CCO} = \text{GND}$

Symbol	Parameter	TA = -40°C			TA = 0°C			TA = +25°C			TA = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I _{IH}	Input HIGH Current	—	—	200	—	—	200	—	—	200	—	—	200	μA
I _{EE}	Power Supply Current	—	38	46	—	38	46	—	38	46	—	38	46	mA
		10E	38	46	—	38	46	—	38	46	—	38	46	
		100E	38	46	—	38	46	—	38	46	—	44	53	

AC ELECTRICAL CHARACTERISTICS

$V_{EE} = V_{EE} (\text{Min.})$ to $V_{EE} (\text{Max.})$; $V_{CC} = V_{CCO} = \text{GND}$

Symbol	Parameter	TA = -40°C			TA = 0°C			TA = +25°C			TA = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t _{PLH} t _{PHL}	Propagation Delay to Output D to Q D to F	225 500	385 725	600 1000	225 500	385 725	600 1000	225 500	385 725	600 1000	225 500	385 725	600 1000	ps
t _{skew}	Within-Device Skew, D to Q ⁽¹⁾	—	75	—	—	75	—	—	75	—	—	75	—	ps
t _r t _f	Rise/Fall Time 20% to 80% Q F	275 300	425 475	700 700	275 300	425 475	700 700	275 300	425 475	700 700	275 300	425 475	700 700	ps

NOTE:

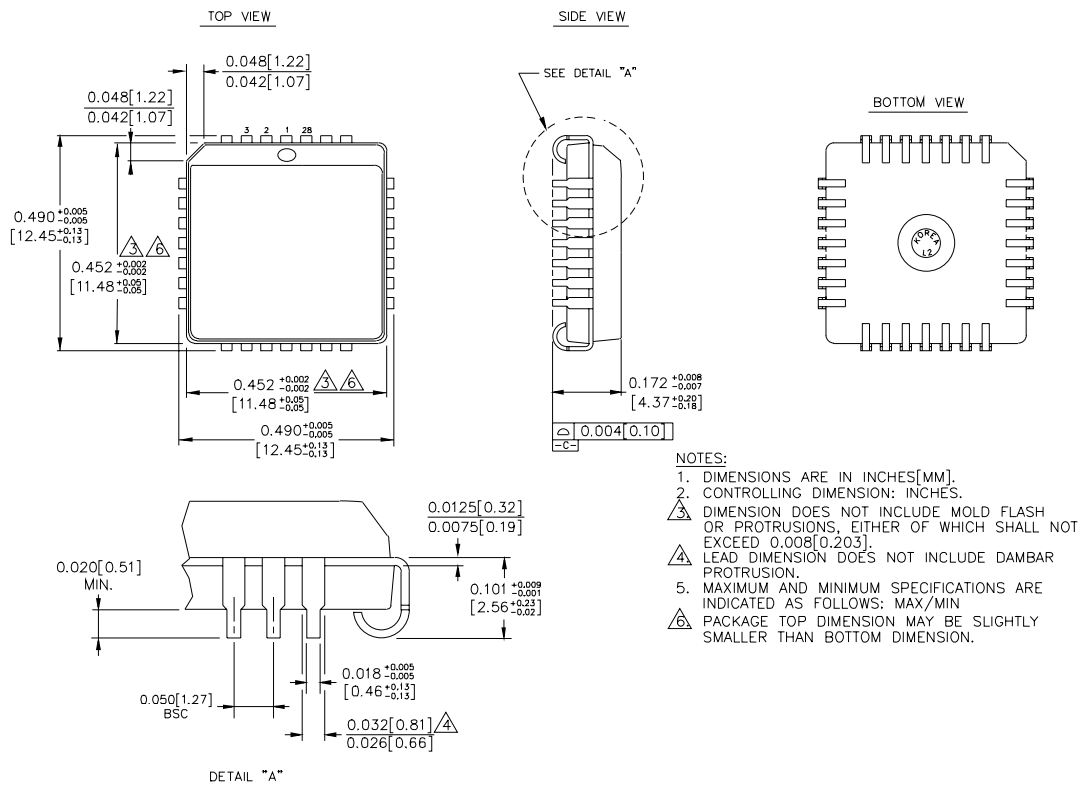
1. Within-device skew is defined as identical transitions on similar paths through a device.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E104JC	J28-1	Commercial
SY10E104JCTR	J28-1	Commercial
SY100E104JC	J28-1	Commercial
SY100E104JCTR	J28-1	Commercial

Ordering Code	Package Type	Operating Range
SY10E104JI	J28-1	Industrial
SY10E104JITR	J28-1	Industrial
SY100E104JI	J28-1	Industrial
SY100E104JITR	J28-1	Industrial

28 LEAD PLCC (J28-1)



Rev. 03

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