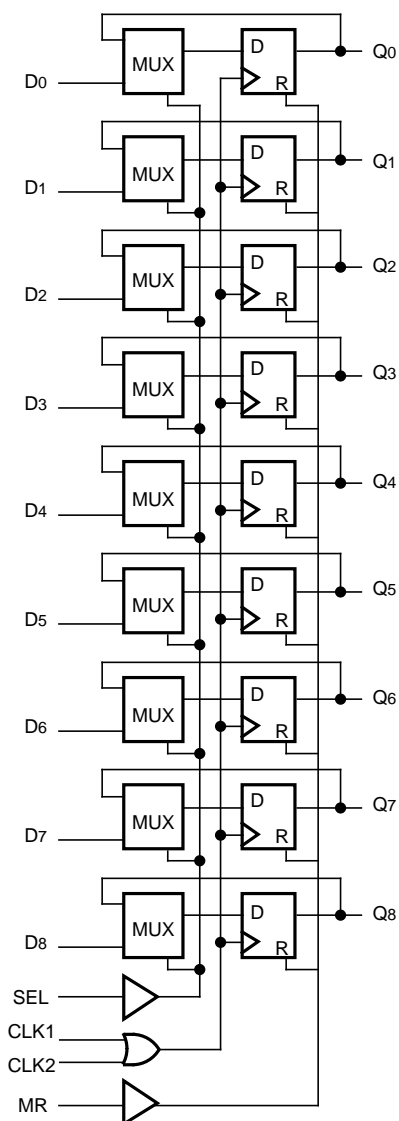


## FEATURES

- 700MHz min. operating frequency
- Extended 100E VEE range of -4.2V to -5.5V
- 9 bits wide for byte-parity applications
- Asynchronous Master Reset
- Dual clocks
- Fully compatible with industry standard 10KH, 100K ECL levels
- Internal 75kΩ input pulldown resistors
- Fully compatible with Motorola MC10E/100E143
- Available in 28-pin PLCC package

## BLOCK DIAGRAM



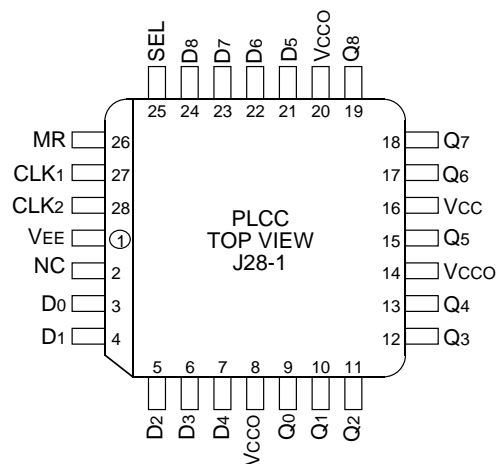
## DESCRIPTION

The SY10/100E143 are high-speed 9-bit hold registers designed for use in new, high-performance ECL systems. The E143 can hold current data or load new data. The nine inputs, D0-D8, accept parallel input data.

The SEL (Select) control pin serves to determine the mode of operation; either HOLD or LOAD. The input data has to meet the set-up time before being clocked into the nine input registers on the rising edge of CLK1 or CLK2. The MR (Master Reset) control signal asynchronously resets all nine registers to a logic LOW when a logic HIGH is applied to MR.

The E143 is designed for applications requiring high-speed registers, pipeline registers, synchronous operation, and is also suitable for byte-wide parity.

## PIN CONFIGURATION



## PIN NAMES

Pin	Function
D0-D8	Parallel Data Inputs
SEL	Mode Select Input
CLK1, CLK2	Clock Inputs
MR	Master Reset
Q0-Q8	Data Outputs
NC	No Connection
VCCO	Vcc to Output

**TRUTH TABLE**

SEL	MODE
L	LOAD
H	HOLD

**DC ELECTRICAL CHARACTERISTICS**

VEE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

Symbol	Parameter	TA = 0°C			TA = +25°C			TA = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I <sub>IH</sub>	Input HIGH Current	—	—	150	—	—	150	—	—	150	μA	—
I <sub>EE</sub>	Power Supply Current	—	—	—	—	—	—	—	—	—	mA	—
		10E	120	145	120	145	145	120	145	145		
		100E	120	145	120	145	145	138	165	165		

**AC ELECTRICAL CHARACTERISTICS**

VEE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

Symbol	Parameter	TA = 0°C			TA = +25°C			TA = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
f <sub>MAX</sub>	Max. Toggle Frequency	700	900	—	700	900	—	700	900	—	MHz	—
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay to Output CLK MR	600 600	800 800	1000 1000	600 600	800 800	1000 1000	600 600	800 800	1000 1000	ps	—
t <sub>S</sub>	Set-up Time D SEL	50 300	—100 150	— —	50 300	—100 150	— —	50 300	—100 150	— —	ps	—
t <sub>H</sub>	Hold Time D SEL	300 75	100 —150	— —	300 75	100 —150	— —	300 75	100 —150	— —	ps	—
t <sub>RR</sub>	Reset Recovery Time	900	700	—	900	700	—	900	700	—	ps	—
t <sub>PW</sub>	Minimum Pulse Width CLK, MR	400	—	—	400	—	—	400	—	—	ps	—
t <sub>skew</sub>	Within-Device Skew	—	75	—	—	75	—	—	75	—	ps	1
t <sub>r</sub> t <sub>f</sub>	Rise/Fall Time 20% to 80%	300	525	800	300	525	800	300	525	800	ps	—

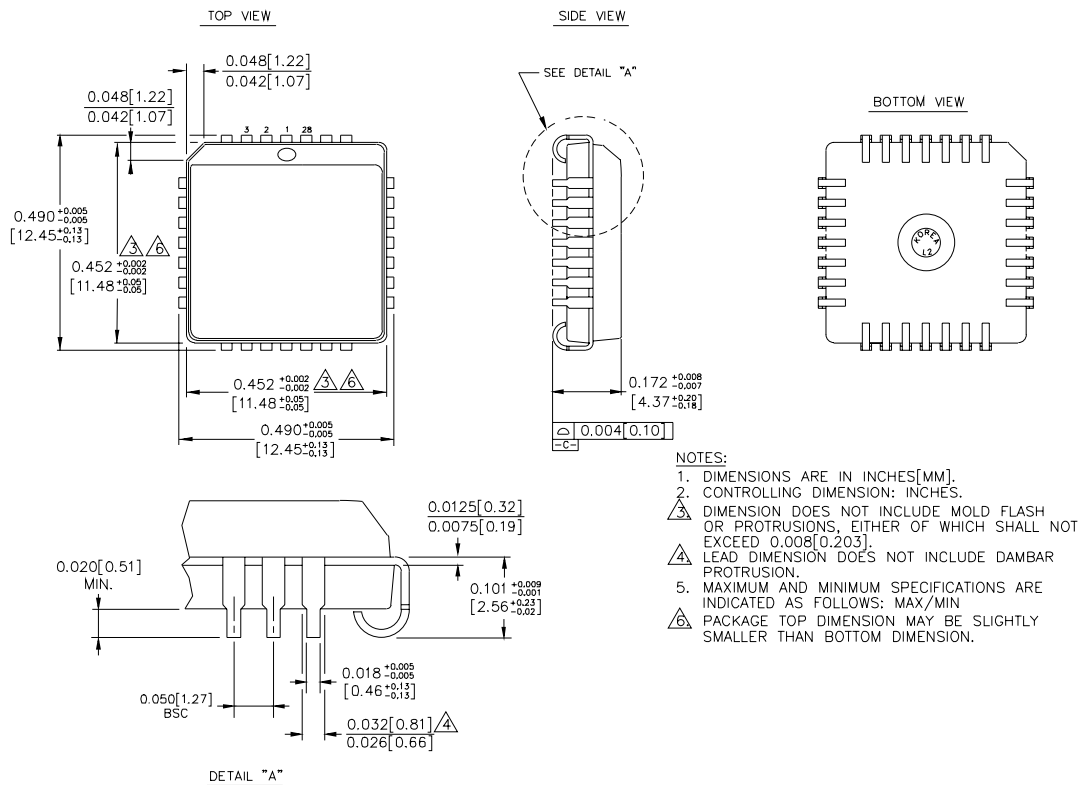
**NOTE:**

1. Within-device skew is defined as identical transitions on similar paths through a device.

**PRODUCT ORDERING CODE**

Ordering Code	Package Type	Operating Range
SY10E143JC	J28-1	Commercial
SY10E143JCTR	J28-1	Commercial
SY100E143JC	J28-1	Commercial
SY100E143JCTR	J28-1	Commercial

## 28 LEAD PLCC (J28-1)



Rev. 03

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**MICREL-SYNERGY 3250 SCOTT BOULEVARD SANTA CLARA CA 95054 USA**

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