

FEATURES

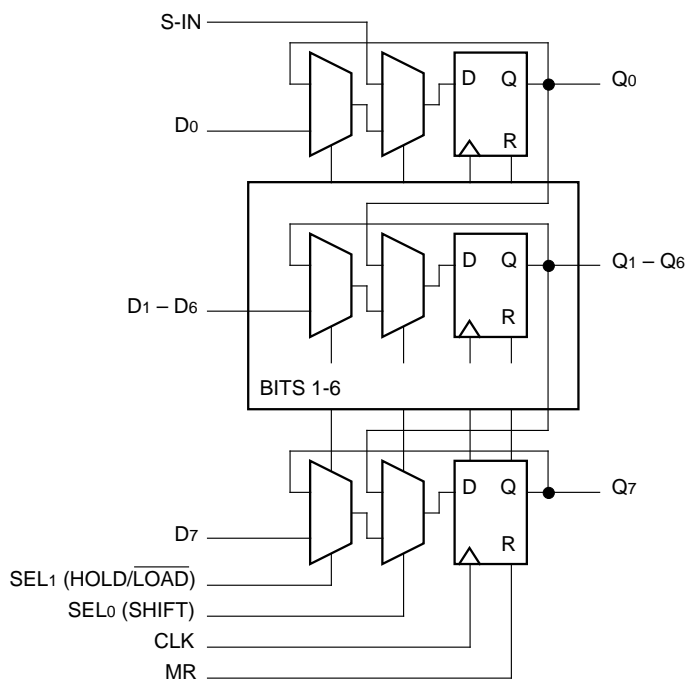
- 1000ps max. CLK to output
- Extended 100E VEE range of -4.2V to -5.5V
- SHIFT overrides HOLD, /LOAD control
- Asynchronous Master Reset
- Pin-compatible with E141
- Fully compatible with industry standard 10KH, 100K ECL levels
- Internal 75K Ω input pulldown resistors
- Fully compatible with Motorola MC10E/100E241
- Available in 28-pin PLCC package

DESCRIPTION

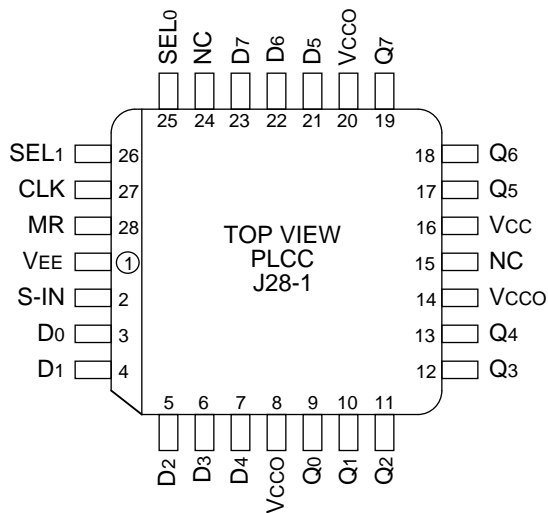
The SY10/100E241 are 8-bit shiftable registers designed for use in new, high-performance ECL systems. Unlike the E141, the E241 features internal data feedback organized such that the SHIFT control overrides the HOLD, /LOAD control. Thus, the normal operations of HOLD and LOAD can be toggled with a single control line without the need for external gating. This configuration also enables switching to scan mode with the single SHIFT control line.

The eight inputs D0–D7 accept parallel input data, while S-IN accepts serial input data when in shift mode. Data is accepted a set-up time before the rising edge of CLK. Shifting is also accomplished on the rising clock edge. A HIGH on the Master Reset pin (MR) asynchronously resets all the registers to zero.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin	Function
D0–D7	Parallel Data Inputs
S-IN	Serial Data Input
SEL0	SHIFT Control
SEL1	HOLD, /LOAD Control
CLK	Clock
MR	Master Reset
Q0–Q7	Data Outputs
VCC0	Vcc to Output

TRUTH TABLE

SEL ₀	SEL ₁	Function
L	L	Load
L	H	Hold
H	X	Shift (D _n to D _{n+1})

DC ELECTRICAL CHARACTERISTICSV_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T _A = 0°C			T _A = +25°C			T _A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I _{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	μA	—
I _{EE}	Power Supply Current	—	—	—	—	—	—	—	—	—	mA	—
	10E	—	125	150	—	125	150	—	125	150		
	100E	—	125	150	—	125	150	—	144	173		

AC ELECTRICAL CHARACTERISTICSV_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T _A = 0°C			T _A = +25°C			T _A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
f _{SHIFT}	Max. Shift Frequency	700	900	—	700	900	—	700	900	—	MHz	—
t _{PLH} t _{PHL}	Propagation Delay to Output CLK MR	625 600	750 725	975 975	625 600	750 725	975 975	625 600	750 725	975 975	ps	—
t _s	Set-up Time	—	—	—	—	—	—	—	—	—	ps	—
	D	175	25	—	175	25	—	175	25	—		
	SEL ₀ (SHIFT)350	200	—	350	200	—	350	200	—	—		
	SEL ₁ (HOLD/LOAD)	400	250	—	400	250	—	400	250	—		
t _H	S-IN	125	—100	—	125	—100	—	125	—100	—	ps	—
	Hold Time	—	—	—	—	—	—	—	—	—		
	D	200	—25	—	200	—25	—	200	—25	—		
	SEL ₀ (SHIFT)	100	—200	—	100	—200	—	100	—200	—		
t _{RR}	SEL ₁ (HOLD/LOAD)	50	—250	—	50	—250	—	50	—250	—	ps	—
	S-IN	300	100	—	300	100	—	300	100	—		
	Reset Recovery Time	900	600	—	900	600	—	900	600	—		
	Minimum Pulse Width	400	—	—	400	—	—	400	—	—		
t _{PW}	CLK, MR	—	—	—	—	—	—	—	—	—	ps	—
t _{skew}	Within-Device Skew	—	60	—	—	60	—	—	60	—	ps	1
t _r t _f	Rise/Fall Time 20% to 80%	300	525	800	300	525	800	300	525	800	ps	—

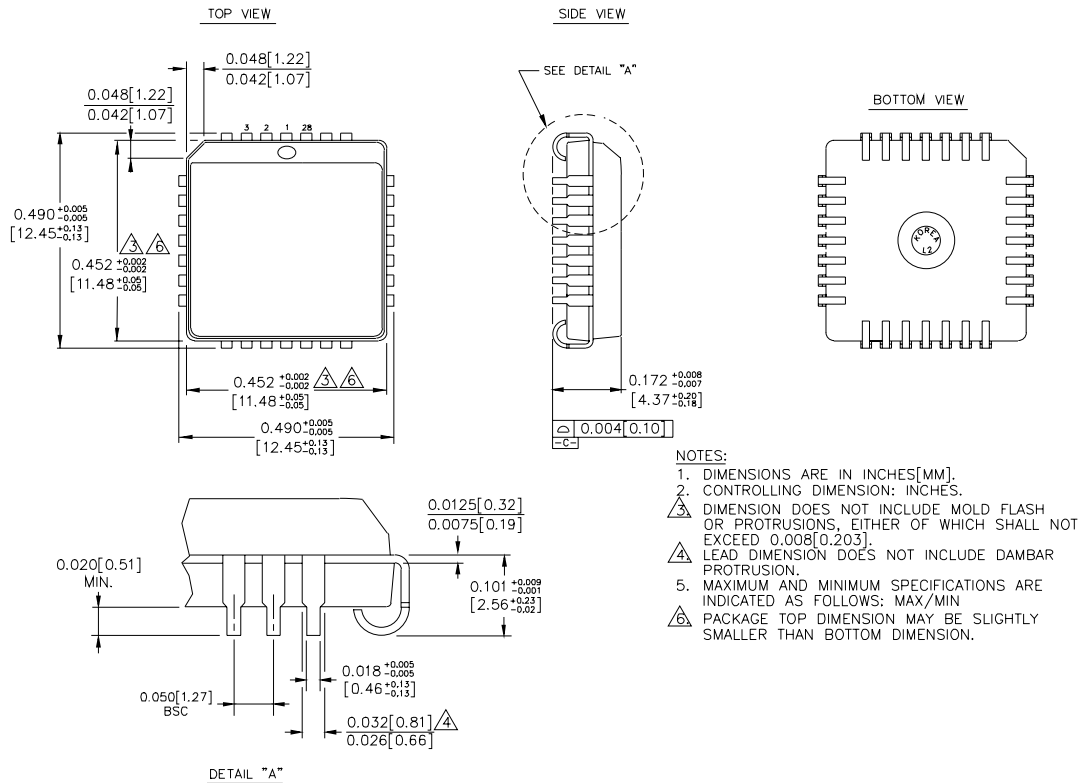
NOTE:

1. Within-device skew is defined as identical transitions on similar paths through a device.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E241JC	J28-1	Commercial
SY10E241JCTR	J28-1	Commercial
SY100E241JC	J28-1	Commercial
SY100E241JCTR	J28-1	Commercial

28 LEAD PLCC (J28-1)



Rev. 03

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