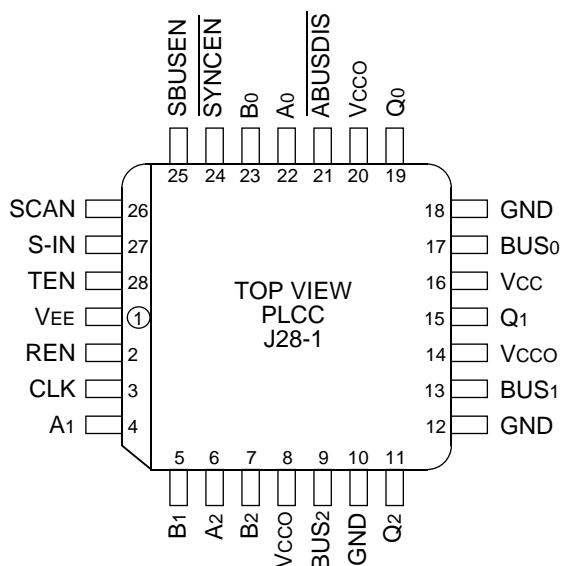


## FEATURES

- 1500ps max. clock to bus (data transmit)
- 1000ps max. clock to Q (data receive)
- Extended 100E VEE range of  $-4.2V$  to  $-5.5V$
- $25\Omega$  cutoff bus outputs
- $50\Omega$  receiver outputs
- Scannable implementation of E336
- Synchronous and asynchronous bus enables
- Non-inverting data path
- Bus outputs feature internal edge slow-down capacitors
- Additional package ground pins
- Fully compatible with industry standard 10KH, 100K ECL levels
- Internal  $75K\Omega$  input pulldown resistors
- Fully compatible with Motorola MC10E/100E337
- Available in 28-pin PLCC package

## PIN CONFIGURATION



## DESCRIPTION

The SY10/100E337 are 3-bit registered bus transceivers with scan designed for use in new, high-performance ECL systems. The bus outputs (BUS0–BUS2) are designed to drive a  $25\Omega$  bus; the receive outputs (Q0–Q2) are designed for  $50\Omega$ . The bus outputs feature a normal logic HIGH level (VOH) and a cutoff LOW level of  $-2.0V$  and the output emitter-follower is “off”, presenting a high impedance to the bus. The bus outputs also feature edge slow-down capacitors.

Both drive and receive sides feature the same logic, including a loopback path to hold data. The LOAD/HOLD function is controlled by Transmit Enable (TEN) and Receive Enable (REN) on the transmit and receive sides, respectively, with a HIGH selecting LOAD. The implementation of the E337 Receive Enable differs from that of the E336.

A synchronous bus enable (SBUSEN) is provided for normal, non-scan operation. The asynchronous bus disable (ABUSDIS) disables the bus for scan mode.

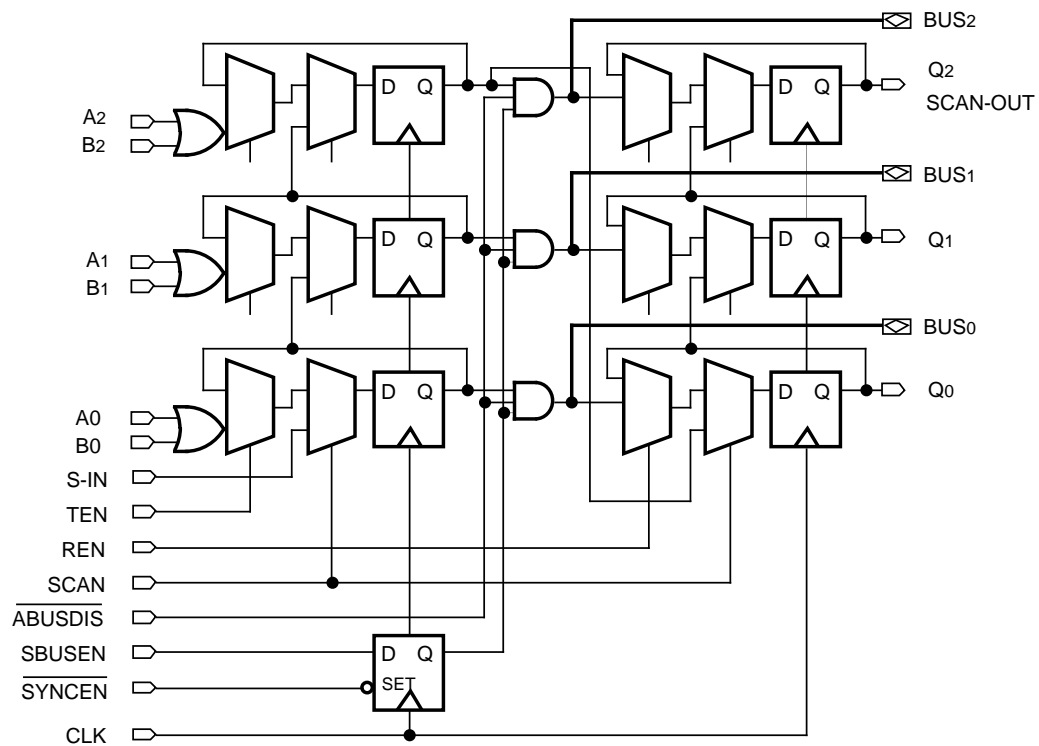
The SYNCEN input allows either synchronous or asynchronous re-enabling after disabling with ABUSDIS. An alternative use is asynchronous-only operation with ABUSDIS, in which case SYNCEN is tied LOW. SYNCEN is implemented as an overriding SET control to the enable flip-flop.

Scan mode is selected by a logic HIGH at the SCAN input. Scan input data is shifted in through S-IN, and output data appears at the Q2 output.

All registers are clocked on the rising edge of CLK. Additional lead-frame grounding is provided through the ground pins (GND) which should be connected to 0V. The GND pins are not electrically connected to the chip.

## PIN NAMES

Pin	Function
A0–A2	Data Inputs A
B0–B2	Data Inputs B
S-IN	Serial (Scan) Data Input
TEN, REN	LOAD/HOLD Controls
SCAN	Scan Control
ABUSDIS	Asynchronous Bus Disable
SBUSEN	Synchronous Bus Enable
SYNCEN	Synchronous Enable Control
CLK	Clock
BUS0–BUS2	$25\Omega$ Cutoff BUS Outputs
Q0–Q2	Receive Data Outputs (Q2 serves as SCAN_OUT in scan mode)
VCCO	Vcc to Output

**BLOCK DIAGRAM**

**DC ELECTRICAL CHARACTERISTICS**

VEE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

Symbol	Parameter	TA = 0°C			TA = +25°C			TA = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
VCUT	Cut-off Output Voltage	-2.10	—	-2.03	-2.10	—	-2.03	-2.10	—	-2.03	V	1
I <sub>IH</sub>	Input HIGH Current All Other Inputs	—	—	150	—	—	150	—	—	150	μA	—
I <sub>EE</sub>	Power Supply Current	—	—	—	—	—	—	—	—	—	mA	—
	10E	—	145	174	—	145	174	—	145	174		
	100E	—	145	174	—	125	174	—	167	200		

**NOTE:**1. Applies to BUS outputs only. Measured with V<sub>TT</sub> = -2.10V.**AC ELECTRICAL CHARACTERISTICS**

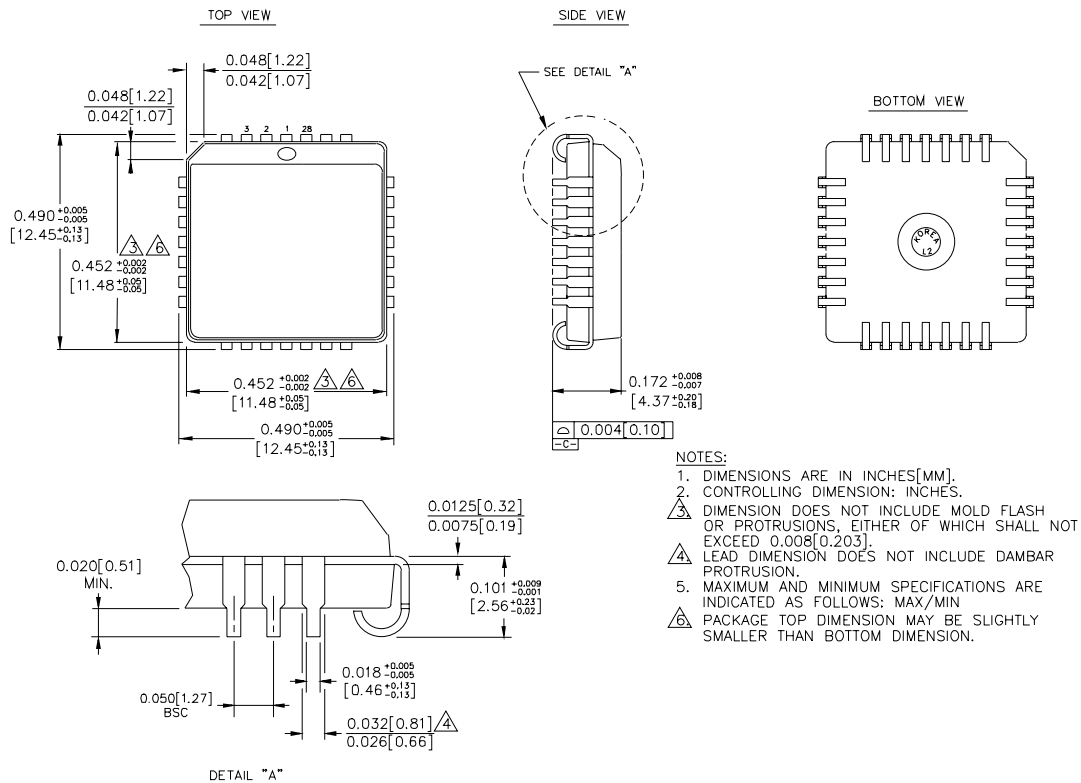
VEE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

Symbol	Parameter	TA = 0°C			TA = +25°C			TA = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay to Output CLK to Q CLK to BUS ABUSDIS SYNSEN	450 800 500 800	— — — —	1000 1800 1500 1800	450 800 500 800	— — — —	1000 1800 1500 1800	450 800 500 800	— — — —	1000 1800 1500 1800	ps	—
t <sub>s</sub>	Set-up Time BUS	350	—	—	350	—	—	350	—	—	ps	—
	SBUSEN	100	—	—	100	—	—	100	—	—		
	Data, S-IN	400	—	—	400	—	—	400	—	—		
	TEN, REN, SCAN	550	—	—	550	—	—	550	—	—		
t <sub>H</sub>	Hold Time BUS	350	—	—	350	—	—	350	—	—	ps	—
	SBUSEN	500	—	—	500	—	—	500	—	—		
	Data, S-IN	350	—	—	350	—	—	350	—	—		
	TEN, REN, SCAN	200	—	—	200	—	—	200	—	—		
t <sub>PW</sub>	Minimum Pulse Width	400	—	—	400	—	—	400	—	—	ps	—
t <sub>r</sub> t <sub>f</sub>	Rise/Fall Time	—	—	—	—	—	—	—	—	—	ps	—
	20% to 80% (Q <sub>n</sub> )	300	—	800	300	—	800	300	—	800		
	20% to 80% (BUS <sub>n</sub> Rise)	500	—	1000	500	—	1000	500	—	1000		
	20% to 80% (BUS <sub>n</sub> Fall)	300	—	800	300	—	800	300	—	800		

**PRODUCT ORDERING CODE**

Ordering Code	Package Type	Operating Range
SY10E337JC	J28-1	Commercial
SY10E337JCTR	J28-1	Commercial
SY100E337JC	J28-1	Commercial
SY100E337JCTR	J28-1	Commercial

## 28 LEAD PLCC (J28-1)



Rev. 03

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