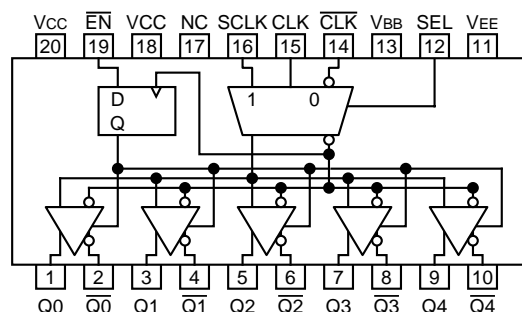


### FEATURES

- 3.3V and 5V power supply options
- Typical 30ps output-to-output skew
- Max. 50ps output-to-output skew
- Synchronous enable/disable
- Multiplexed clock input
- 75K $\Omega$  internal input pull-down resistors
- Available in 20-pin SOIC package

### PIN CONFIGURATION/BLOCK DIAGRAM



SOIC  
TOP VIEW

### DESCRIPTION

The SY100EL14V is a low skew 1:5 clock distribution chip designed explicitly for low skew clock distribution applications. The device can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal. The EL14V is suitable for operation in systems operating from 3.3V to 5.0V supplies. If a single-ended input is to be used the VBB output should be connected to the  $\overline{\text{CLK}}$  input and bypassed to ground via a 0.01 $\mu\text{F}$  capacitor. The VBB output is designed to act as the switching reference for the input of the EL14V under single-ended input conditions, as a result this pin can only source/sink up to 0.5mA of current.

The EL14V features a multiplexed clock input to allow for the distribution of a lower speed scan or test clock along with the high speed system clock. When LOW (or left open and pulled LOW by the input pull-down resistor) the SEL pin will select the differential clock input.

The common enable ( $\overline{\text{EN}}$ ) is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids any chance of generating a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip flop is clocked on the falling edge of the input clock, therefore all associated specification limits are referenced to the negative edge of the clock input.

When both differential inputs are left open, CLK input will pull down to VEE and  $\overline{\text{CLK}}$  input will bias around VCC/2.

### PIN NAMES

Pin	Function
CLK	Differential Clock Inputs
SCLK	Scan Clock Input
$\overline{\text{EN}}$	Synchronous Enable
SEL	Clock Select Input
VBB	Reference Output
Q0-4	Differential Clock Outputs

### TRUTH TABLE

CLK	SCLK	SEL	$\overline{\text{EN}}$	Q
L	X	L	L	L
H	X	L	L	H
X	L	H	L	L
X	H	H	L	H
X	X	X	H	L*

\* On next negative transition of CLK or SCLK

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Rating	Value	Unit
VEE	Power Supply (VCC = 0V)	-8.0 to 0	VDC
VI <sup>(3)</sup>	Input Voltage (VCC = 0V)	0 to -6.0	VDC
IOUT	Output Current - Continuous - Surge	50 100	mA
TA	Operating Temperature Range	-40 to +85	°C
VEE	Operating Range <sup>(1),(2)</sup>	-5.7 to -3.0	V

**NOTES:**

1. Absolute maximum rating, beyond which, device life may be impaired, unless otherwise specified on an individual data sheet.
2. Parametric values specified at: 100EL14V Series: -3.0V to -5.5V.
3. In PECL mode operation, VI(Max) = VCC.

**DC ELECTRICAL CHARACTERISTICS**VEE = VEE (Min) to VEE (Max); VCC = GND<sup>(1)</sup>

Symbol	Parameter	TA = -40°C			TA = 0°C			TA = +25°C			TA = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
VOH	Output HIGH Voltage <sup>(2)</sup>	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	-1025	-955	-880	mV
VOL	Output LOW Voltage <sup>(2)</sup>	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	-1810	-1705	-1620	mV
VOHA	Output HIGH Voltage <sup>(2)</sup>	-1095	—	—	-1035	—	—	-1035	—	—	-1035	—	—	mV
VOLA	Output LOW Voltage <sup>(2)</sup>	—	—	-1555	—	—	-1610	—	—	-1610	—	—	-1610	mV
VIH	Input HIGH Voltage	-1165	—	-880	-1165	—	-880	-1165	—	-880	-1165	—	-880	mV
VIL	Input LOW Voltage	-1810	—	-1475	-1810	—	-1475	-1810	—	-1475	-1810	—	-1475	mV
IIL	Input LOW Current <sup>(3)</sup> CLK	0.5 -300	— —	— —	0.5 -300	— —	— —	0.5 -300	— —	— —	0.5 -300	— —	— —	μA
IIH	Input High Current	—	—	150	—	—	150	—	—	150	—	—	150	μA
IEE	Power Supply Current	—	32	40	—	32	40	—	32	40	—	34	42	mA
VBB	Output Reference Voltage	-1.38	—	-1.26	-1.38	—	-1.26	-1.38	—	-1.26	-1.38	—	-1.26	V

**NOTES:**

1. This table replaces the three traditionally seen in ECL 100K data books. The same DC parameter values at VEE = -4.5V now apply across the full VEE range of -3.0V to -5.5V. Outputs are terminated through a 50Ω resistor to -2.0V except where otherwise specified on the individual data sheets.
2. VIN = VIH(Max) or VIL(Min).
3. VIN = VIL(Max).

**AC ELECTRICAL CHARACTERISTICS**

VEE = VEE (Min) to VEE (Max); VCC = GND

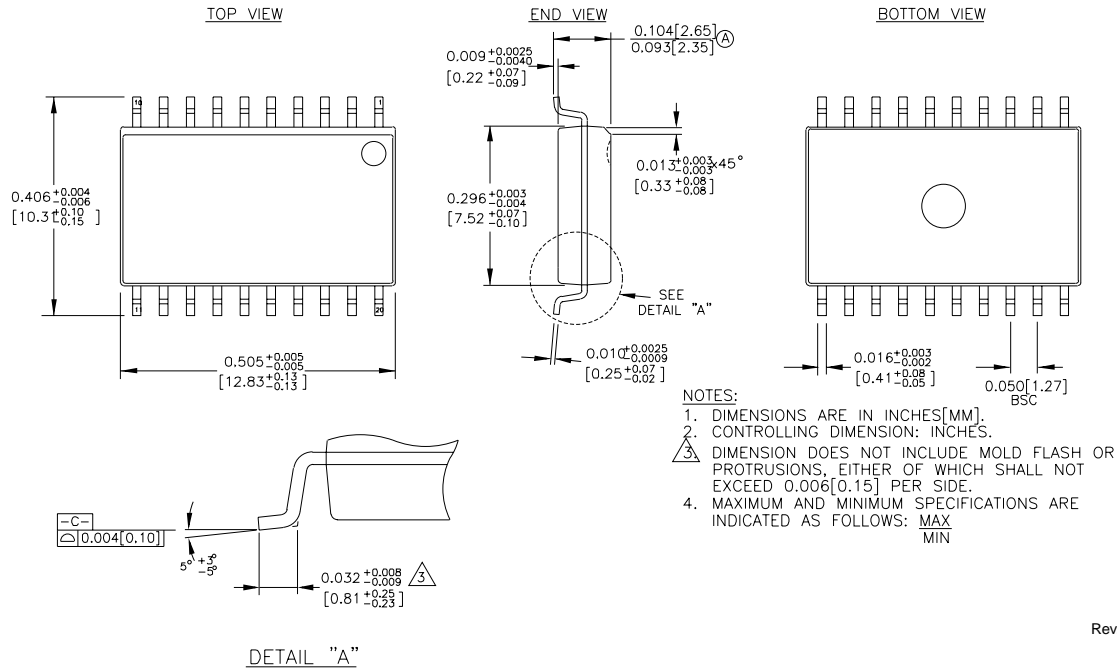
Symbol	Parameter	TA = -40°C		TA = 0°C		TA = +25°C			TA = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
tPLH tPHL	Propagation Delay CLK to Q (Diff) CLK to Q (SE) SCLK to Q	520 470 470	720 770 770	550 500 500	750 800 800	580 530 530	680 680 680	780 830 830	630 580 580	830 880 880	ps
tskew	Part-to-Part Skew <sup>(1)</sup> Within-Device Skew	— —	200 50	— —	200 50	— —	— —	200 50	— —	200 50	ps
ts	Setup Time $\overline{EN}$	150	—	150	—	150	—	—	150	—	ps
th	Hold Time $\overline{EN}$	200	—	200	—	200	—	—	200	—	ps
VPP	Minimum Input CLK Swing	150	—	150	—	150	—	—	150	—	mV
VCMR	Common Mode Range <sup>(2)</sup>										mV
	VPP < 500mV	-2.0	-0.4	-2.1	-0.4	-2.1	—	-0.4	-2.1	-0.4	
	VPP ≥ 500mV	-1.8	-0.4	-1.9	-0.4	-1.9	—	-0.4	-1.9	-0.4	
tr tf	Output Rise/Fall Times Q (20% – 80%)	230	500	230	500	230	360	500	230	500	ps

**NOTES:**

- Skews are specified for identical LOW-to-HIGH or HIGH-to-LOW transitions.
- The VCMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between VPP(Min) and 1V. The lower end of the VCMR range varies 1:1 with VEE. The numbers in the specification table assume a nominal VEE = -3.3V. For PECL operation, the VCMR(Min) will be fixed at 3.3V – |VCMR(Min)|.

**PRODUCT ORDERING CODE**

Ordering Code	Package Type	Operating Range
SY100EL14VZC	Z20-1	Commercial
SY100EL14VZCTR	Z20-1	Commercial

**20 LEAD SOIC .300" WIDE (Z20-1)**

Rev. 03

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