

FEATURES

- Pin-for-pin, plug-in compatible to the ON Semiconductor MC100EP195
- Maximum frequency > 2.5GHz
- Programmable range: 2.2ns to 12.2ns
- 10ps increments
- PECL mode operating range: $V_{CC} = 3.0V$ to $5.5V$ with $V_{EE} = 0V$
- NECL mode operating range: $V_{CC} = 0V$ with $V_{EE} = -3.0V$ to $-5.5V$
- Open input default state
- Safety clamp on inputs
- A logic high on the /EN pin will force Q to logic low
- D[0:10] can accept either ECL, CMOS, or TTL inputs
- V_{BB} output reference voltage
- Available in a 32-pin TQFP package



ECL Pro®

DESCRIPTION

The SY100EP195V is a programmable delay line, varying the time a logic signal takes to traverse from IN to Q. This delay can vary from about 2.2ns to about 12.2ns. The input can be PECL, LVPECL, NECL, or LVNECL.

The delay varies in discrete steps based on a control word presented to SY100EP195V. The 10-bit width of this latched control register allows for delay increments of approximately 10ps.

An eleventh control bit allows the cascading of multiple SY100EP195V devices, for a wider delay range. Each additional SY100EP195V effectively doubles the delay range available.

For maximum flexibility, the control register interface accepts CMOS or TTL level signals, as well as the input level at the IN± pins.

All support documentation can be found on Micrel's web site at www.micrel.com.

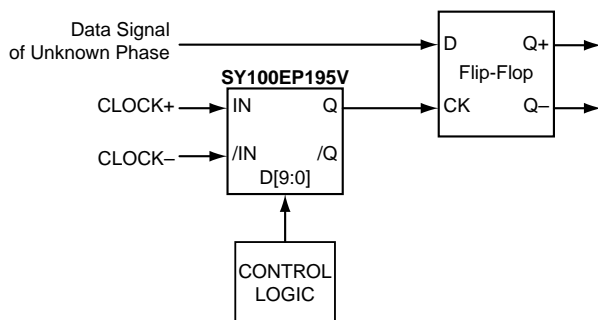
APPLICATIONS

- Clock de-skewing
- Timing adjustment
- Aperture centering

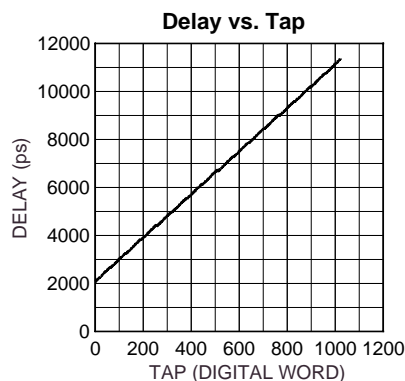
CROSS REFERENCE TABLE

| Micrel Semiconductor | ON Semiconductor |
|----------------------|------------------|
| SY100EP195VTI | MC100EP195FA |
| SY100EP195VTITR | MC100EP195FAR2 |

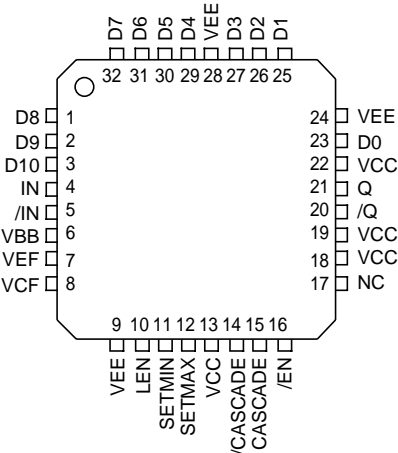
TYPICAL APPLICATIONS CIRCUIT



TYPICAL PERFORMANCE



PACKAGE/ORDERING INFORMATION



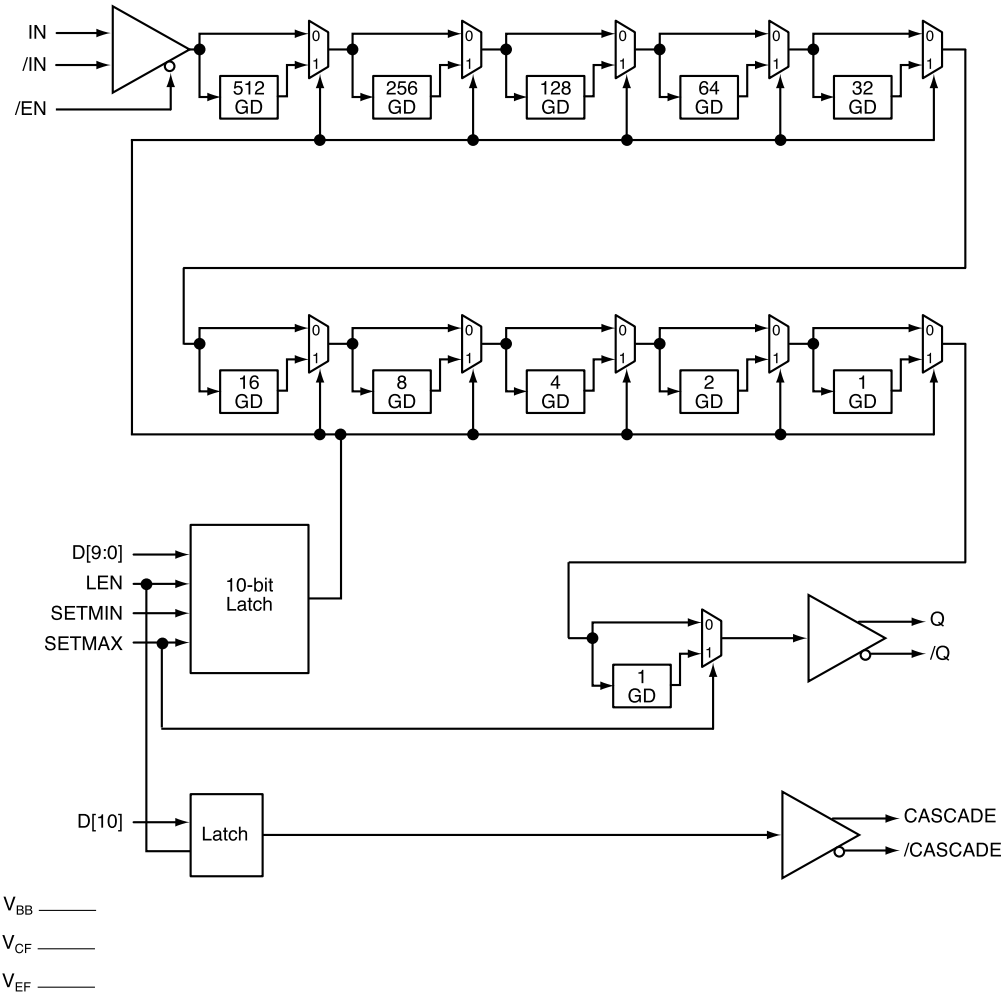
32-Pin TQFP (T32-1)

Ordering Information

| Part Number | Package Type | Operating Range | Package Marking |
|--------------------------------|--------------|-----------------|-----------------|
| SY100EP195VTI | T32-1 | Industrial | SY100EP195V |
| SY100EP195VTITR ⁽¹⁾ | T32-1 | Industrial | SY100EP195V |

Note:
1. Tape and Reel.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

| Pin Number | Pin Name | Pin Function |
|--------------------------------------|-------------------|--|
| 23, 25, 26, 27, 29, 30, 31, 32, 1, 2 | D[0:9] | CMOS, ECL, or TTL Select Inputs: These digital control signals adjust the amount of delay from IN to Q. Please refer to the "Ac Electrical Table" (page 7) and Table 7 (page 17) for delay values. Figure 9 shows how to interface these inputs to various logic family standards. These inputs default to logic low when left unconnected. Bit 0 is the least significant bit, and bit 9 is the most significant bit. |
| 3 | D[10] | CMOS, ECL, or TTL Select Input: This input latches just like D[0:9] does. It drives the CASCADE, /CASCADE differential pair. Use only when cascading two or more SY100EP195V to extend the range of delays required. |
| 4, 5 | IN, /IN | ECL Input: This is the signal to be delayed. If this input pair is left unconnected, this is equivalent to a logic low input. |
| 6 | VBB | Voltage Output: When using a single-ended logic source for IN and /IN, connect the unused input of the differential pair to this pin. This pin can also re-bias AC-coupled inputs to IN and /IN. When used, de-couple this pin to V _{CC} through an 0.01μF capacitor. Limit current sinking or sourcing to 0.5mA or less. |
| 7 | VEF | Voltage Output: Connect this pin to VCF when the D inputs are ECL. Refer to the "Digital Control Logic Standard" section of the "Functional Description" to interface the D inputs to CMOS or TTL. |
| 8 | VCF | Voltage Input: The voltage at this pin sets the logic transition threshold for the D inputs. |
| 9, 24, 28 | VEE | Most Negative Supply: Supply ground for PECL systems. |
| 10 | LEN | ECL Control Input: When logic low, the D inputs flow through. Any changes to the D inputs reflect in the delay between IN, /IN and Q, /Q. When logic high, the logic values at D are latched, and these latched bits determine the delay. |
| 11 | SETMIN | ECL Control Input: When logic high, the contents of the D register are reset. This sets the delay to the minimum possible, equivalent to D[0:9] being set to 0000000000. When logic low, the value of the D register, or the logic value of SETMAX determines the delay from IN, /IN to Q, /Q. This input defaults to logic low when left unconnected. |
| 12 | SETMAX | ECL Control Input: When logic high and SETMIN is logic low, the contents of the D register are set high, and the delay is set to one step greater than the maximum possible with D[0:9] set to 1111111111. When logic low, the value of the D register, or the logic value of SETMIN determines the delay from IN, /IN to Q, /Q. This input defaults to logic low when left unconnected. |
| 13, 18, 19, 22 | VCC | Most Positive Supply: Supply ground for NECL systems. Bypass to V _{EE} with 0.1μF and 0.01μF low ESR capacitors. |
| 15, 14 | CASCADE, /CASCADE | 100 ECL Outputs: These outputs are used when cascading two or more SY100EP195V to extend the delay range required. |
| 16 | /EN | ECL Control Input: When set active low, Q, /Q are a delayed version of IN, /IN. When set inactive high, IN, /IN are gated such that Q, /Q become a differential logic low. This input defaults to logic low when left unconnected. |
| 20, 21 | Q, /Q | 100k ECL Outputs: This signal pair is the delayed version of IN, /IN. |
| 17 | NC | No Connect: Leave this pin unconnected. |

Absolute Maximum Ratings⁽¹⁾

| | |
|---------------------------------------|------------------------|
| Supply Voltage (V_{CC}) | |
| PECL Mode ($V_{EE}=0V$) | –0.5V to +6.0V |
| Supply Voltage (V_{EE}) | |
| NECL Mode ($V_{CC}=0V$) | +0.5V to –6.0V |
| Any Input Voltage (V_{IN}) | |
| PECL Mode | –0.5V to $V_{CC}+0.5V$ |
| NECL Mode | +0.5V to $V_{EE}-0.5V$ |
| ECL Output Current (I_{OUT}) | |
| Continuous | 50mA |
| Surge | 100mA |
| I_{BB} Sink/Source Current | $\pm 0.5mA$ |
| Lead Temperature (soldering, 10 sec.) | +300°C |
| Storage Temperature (T_S) | –65°C to +150°C |
| ESD Rating ⁽³⁾ | >1.5kV |

Operating Ratings⁽²⁾

| | |
|-------------------------------|----------------|
| Supply Voltage (V_{CC}) | |
| PECL Mode ($V_{EE}=0V$) | +3.0V to +5.5V |
| Supply Voltage (V_{EE}) | |
| NECL Mode ($V_{CC}=0V$) | –3.0V to –5.5V |
| Ambient Temperature (T_A) | –40°C to +85°C |
| Package Thermal Resistance | |
| TQFP-32 (θ_{JA}) | |
| Still-air | 50°C/W |
| 500lfpm | 42°C/W |
| TQFP-32 (θ_{JC}) | 20°C/W |

DC ELECTRICAL CHARACTERISTICS $T_A = -40^\circ\text{C to } +85^\circ\text{C}$.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|----------|-------------------------------------|------------------------------|------|------|------|-------|
| V_{CC} | Power Supply Voltage (PECL) | | 3.0 | 3.3 | 3.6 | V |
| | | | 4.5 | 5.0 | 5.5 | V |
| V_{EE} | Power Supply Voltage (NECL) | | –3.6 | –3.3 | –3.0 | V |
| | | | –5.5 | –5.0 | –4.5 | V |
| I_{EE} | Power Supply Current ⁽⁴⁾ | No load, over supply voltage | | 150 | 175 | mA |

Notes:

1. Permanent device damage may occur if “*Absolute Maximum Ratings*” are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to “*Absolute Maximum Rating*” conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Devices are ESD sensitive. Handling precautions recommended.
4. Required 500lfpm air flow when using +5V or –5V power supply.

LVPECL DC ELECTRICAL CHARACTERISTICS (100kEP)
 $V_{CC} = 3.3V$, $V_{EE} = 0V$; $T_A = -40^{\circ}C$ to $+85^{\circ}C$.^(5, 6)

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|-------------|---|-----------------|----------------------|------|---------------------|--------------------|
| V_{OH} | Output HIGH Voltage | Figures 2, 3, 6 | 2155 | 2280 | 2405 | mV |
| V_{OL} | Output LOW Voltage | Figures 2, 3, 6 | 1355 | 1480 | 1605 | mV |
| V_{IH} | Input HIGH Voltage PECL CMOS TTL | Figures 1, 4 | 2075 1815 2000 | | 2420 | mV mV mV |
| V_{IL} | Input LOW Voltage PECL CMOS TTL | Figures 1, 4 | 1355 | | 1675 1485 800 | mV mV mV |
| V_{BB} | Output Voltage Reference | | 1775 | 1875 | 1975 | mV |
| V_{CF} | Input Select Voltage | | 1610 | 1720 | 1825 | mV |
| V_{EF} | Mode Connection | | 1900 | 2000 | 2100 | mV |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range ⁽⁷⁾ | Figure 5 | 2.0 | | 3.3 | V |
| I_{IH} | Input HIGH Current | | | | 150 | μA |
| I_{IL} | Input LOW Current IN /IN | | 0.5 -150 | | | μA μA |

Notes:

- Device is guaranteed to meet the DC specifications, shown in the table below, after thermal equilibrium has been established. The device is tested in a socket such that transverse airflow of ≥ 500 lfpm is maintained.
- Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.3V to -2.2V.
- V_{IHCMR} maximum varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

PECL DC ELECTRICAL CHARACTERISTICS (100kEP)
 $V_{CC} = 5.0V$, $V_{EE} = 0V$; $T_A = -40^{\circ}C$ to $+85^{\circ}C$.^(8, 9)

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|-------------|--|-----------------|----------------------|------|---------------------|--------------------|
| V_{OH} | Output HIGH Voltage | Figures 2, 3, 6 | 3855 | 3980 | 4105 | mV |
| V_{OL} | Output LOW Voltage | Figures 2, 3, 6 | 3055 | 3180 | 3305 | mV |
| V_{IH} | Input HIGH Voltage PECL CMOS TTL | Figures 1, 4 | 3775 2750 2000 | | 4120 | mV mV mV |
| V_{IL} | Input LOW Voltage PECL CMOS TTL | Figures 1, 4 | 3055 | | 3375 2250 800 | mV mV mV |
| V_{BB} | Output Voltage Reference | | 3475 | 3575 | 3675 | mV |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range ⁽¹⁰⁾ | Figure 5 | 2.0 | | 5.0 | V |
| I_{IH} | Input HIGH Current | | | | 150 | μA |
| I_{IL} | Input LOW Current IN /IN | | 0.5 -150 | | | μA μA |

NECL DC ELECTRICAL CHARACTERISTICS (100kEP)
 $V_{CC} = 0V$, $V_{EE} = -5.5V$ to $-3.0V$; $T_A = -40^{\circ}C$ to $+85^{\circ}C$.⁽⁸⁾

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|-------------|--|--------------|--------------|-------|-------|--------------------|
| V_{OH} | Output HIGH Voltage | Figures 2, 3 | -1145 | -1020 | -895 | mV |
| V_{OL} | Output LOW Voltage | Figures 2, 3 | -1945 | -1820 | -1695 | mV |
| V_{IH} | Input HIGH Voltage NECL | Figures 1, 4 | -1225 | | -880 | mV |
| V_{IL} | Input LOW Voltage NECL | Figures 1, 4 | -1945 | | -1625 | mV |
| V_{BB} | Output Voltage Reference | | -1525 | -1425 | -1325 | mV |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range ⁽¹¹⁾ | Figure 5 | $V_{EE}+2.0$ | | 0.0 | V |
| I_{IH} | Input HIGH Current | | | | 150 | μA |
| I_{IL} | Input LOW Current IN /IN | | 0.5 -150 | | | μA μA |

Notes:

8. Device is guaranteed to meet the DC specifications, shown in the table above, after thermal equilibrium has been established. The device is tested in a socket such that transverse airflow of ≥ 500 lfpm is maintained.
9. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +2.0V to -0.5V.
10. V_{IHCMR} maximum varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.
11. V_{IHCMR} minimum varies 1:1 with V_{EE} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

AC ELECTRICAL CHARACTERISTICS
 $V_{CC} = 3.0$ to $5.5V$, $V_{EE} = 0V$ or $V_{CC} = 0V$, $V_{EE} = -3.0$ to $-5.5V$; $T_A = -40^{\circ}C$ to $+85^{\circ}C$.^(12, 13)

| Symbol | Parameter | $T_A = -40^{\circ}C$ | | | $T_A = +25^{\circ}C$ | | | $T_A = +85^{\circ}C$ | | | Unit |
|----------------|--|----------------------|----------|-------|----------------------|----------|-------|----------------------|----------|-------|-------------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| f_{MAX} | Maximum Frequency ⁽¹⁴⁾ | | 2.5 | | | 2.5 | | | 2.5 | | GHz |
| t_{PD} | Propagation Delay | | | | | | | | | | |
| | IN to Q; D[0-10]=0 | 1650 | 2000 | 2450 | 1800 | 2050 | 2600 | 1950 | 2250 | 2750 | ps |
| | IN to Q; D[0-10]=1023 | 9500 | 11500 | 13500 | 9800 | 12200 | 14000 | 10600 | 13300 | 15800 | ps |
| | /EN to Q; D[0-10]=0 | 1600 | 2150 | 2600 | 1800 | 2300 | 2800 | 2000 | 2500 | 3000 | ps |
| | D10 to CASCADE | 300 | 420 | 500 | 325 | 450 | 550 | 325 | 525 | 625 | ps |
| t_{RANGE} | Programmable Range $t_{PD(max)} - t_{PD(min)}$ | 7850 | 9450 | | 8200 | 10000 | | 8850 | 10950 | | ps |
| Δt | Step Delay ⁽¹⁵⁾ | | | | | | | | | | |
| | D0 High | | 9 | | | 10 | | | 10 | | ps |
| | D1 High | | 25 | | | 26 | | | 27 | | ps |
| | D2 High | | 42 | | | 42 | | | 43 | | ps |
| | D3 High | | 75 | | | 80 | | | 81 | | ps |
| | D4 High | | 142 | | | 143 | | | 150 | | ps |
| | D5 High | | 296 | | | 300 | | | 310 | | ps |
| | D6 High | | 532 | | | 540 | | | 565 | | ps |
| | D7 High | | 1080 | | | 1095 | | | 1140 | | ps |
| | D8 High | | 2100 | | | 2150 | | | 2250 | | ps |
| | D9 High | | 4250 | | | 4300 | | | 4500 | | ps |
| Lin | Linearity ⁽¹⁶⁾ | | ± 10 | | | ± 10 | | | ± 10 | | %LSB |
| t_{SKEW} | Duty Cycle Skew ⁽¹⁷⁾ $t_{PHL} - t_{PLH}$ | | | | | 25 | | | | | ps |
| t_S | Setup Time | | | | | | | | | | |
| | D to LEN | 200 | 0 | | 200 | 0 | | 200 | 0 | | ps |
| | D to IN ⁽¹⁸⁾ | 300 | 140 | | 300 | 160 | | 300 | 180 | | ps |
| | /EN to IN ⁽¹⁹⁾ | 300 | 150 | | 300 | 170 | | 300 | 180 | | ps |
| t_H | Hold Time | | | | | | | | | | |
| | LEN to D | 200 | 60 | | 200 | 100 | | 200 | 80 | | ps |
| | IN to /EN ⁽²⁰⁾ | 400 | 250 | | 400 | 280 | | 400 | 300 | | ps |
| t_R | Release Time | | | | | | | | | | |
| | /EN to IN ⁽²¹⁾ | | | | | 500 | | | | | ps |
| | SETMAX to LEN | 400 | 200 | | 400 | 250 | | 400 | 300 | | ps |
| | SETMIN to LEN | 350 | 275 | | 350 | 200 | | 350 | 335 | | ps |
| t_{JIT} | Cycle-to-Cycle Jitter ⁽²²⁾ | | 0.2 | < 1 | | 0.2 | < 1 | | 0.2 | < 1 | ps _{rms} |
| V_{PP} | Input Voltage Swing (Differential) | 150 | 800 | 1200 | 150 | 800 | 1200 | 150 | 800 | 1200 | mV |
| t_r t_f | Output Rise/Fall Time | | | | | | | | | | |
| | 20% to 80% (Q) | | 180 | 250 | | 210 | 300 | | 230 | 325 | ps |
| | 20% to 80% (CASCADE) | | 180 | 250 | | 210 | 300 | | 230 | 325 | ps |

Notes:

12. AC characteristics are guaranteed by design and characterization.

13. Measured using 750mV source, 50% duty cycle clock source, $R_L = 50\Omega$ to $V_{CC} - 2V$.

14. Refer to "Typical Operating Characteristics" for output swing performance.

15. The delays of the individual bits are cumulative.

16. Linearity is the deviation from the ideal delay.

17. Duty cycle skew guaranteed only for differential operation measured from the crosspoint of the input edge to the crosspoint of the corresponding output edge.

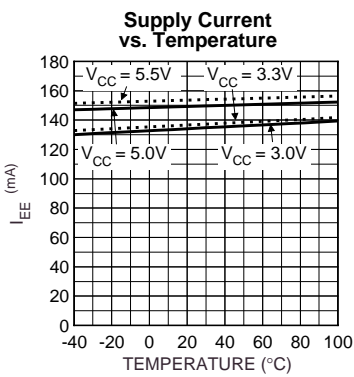
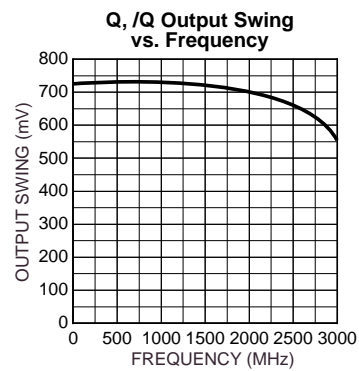
18. Setup time defines the amount of time prior to an edge on IN, /IN that the D[0:9] bits must be set to guarantee the new delay will occur for that edge.

19. Setup time is the minimum that /EN must be asserted prior to the next transition of IN, /IN to prevent an output response greater than $\pm 75mV$ to that IN, /IN transition.20. Hold time is the minimum time that /EN must remain asserted after a negative going IN or a positive going /IN to prevent an output response greater than $\pm 75mV$ to that IN, /IN transition.

21. Release time is the minimum time that /EN must be deasserted prior to the next IN, /IN transition to ensure an output response that meets the specified IN to Q propagation delay and transition times.

22. This is the amount of generated jitter added to an otherwise jitter free clock signal, going from IN, /IN to Q, /Q, where the clock may be any frequency between 0.0 and 2.5GHz.

TYPICAL OPERATING CHARACTERISTICS



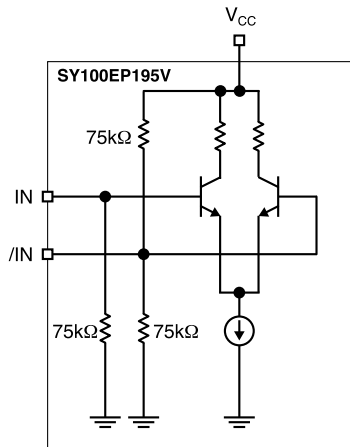


Figure 1a. Differential Input Structure

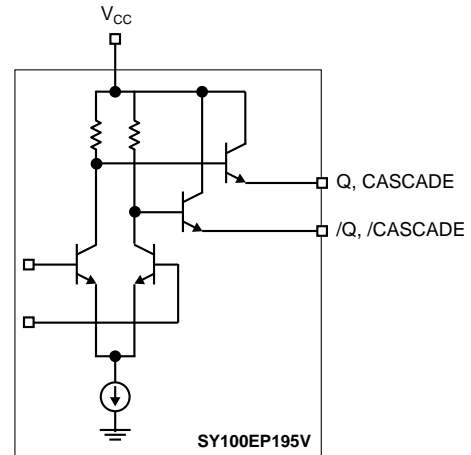


Figure 2. Emitter Output Structure

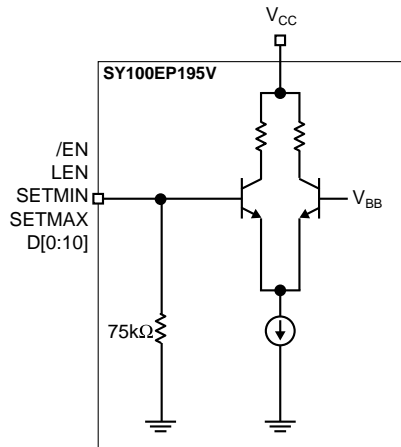


Figure 1b. Single-Ended Input Structure

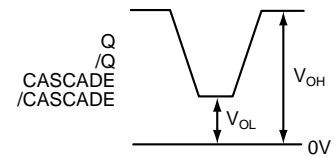


Figure 3a. Output Levels, PECL, LVPECL

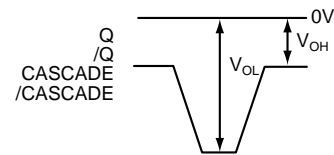


Figure 3b. Output Levels, NECL

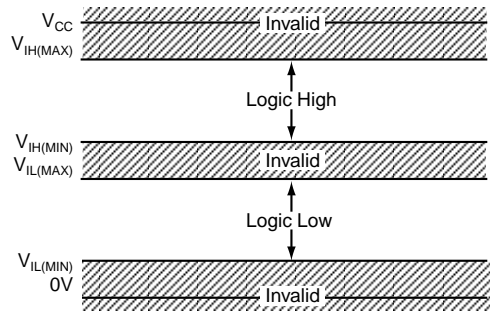


Figure 4a. Input Levels, PECL

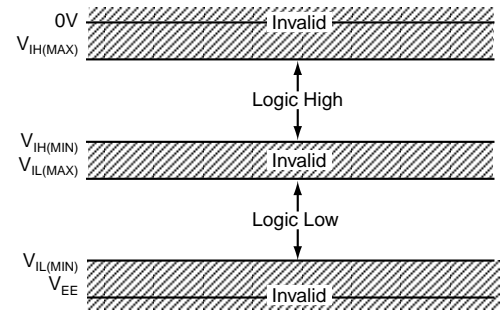


Figure 4c. Input Levels, NECL

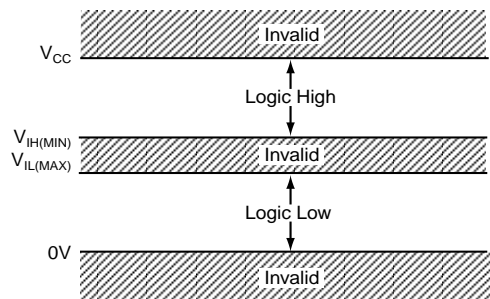


Figure 4b. Input Levels, CMOS, TTL

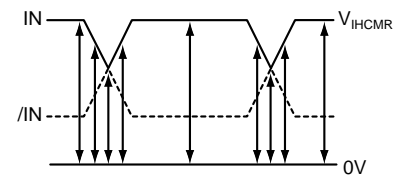


Figure 5a. Input Common Mode, PECL, LVPECL

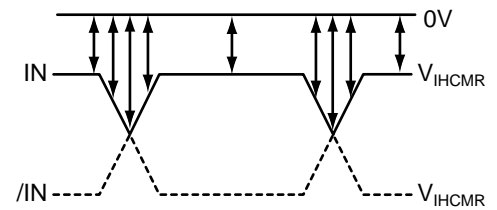


Figure 5b. Input Common Mode, NECL

TERMINATING PECL

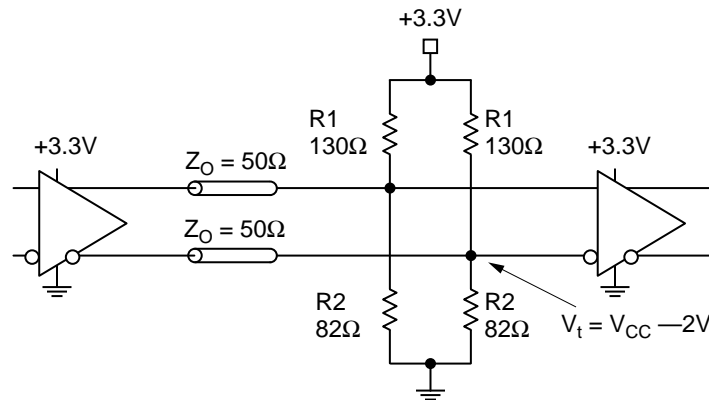


Figure 6a. Parallel Termination—Thevenin Equivalent

Note:

1. For +5.0V systems: $R_1 = 82\Omega$, $R_2 = 130\Omega$.

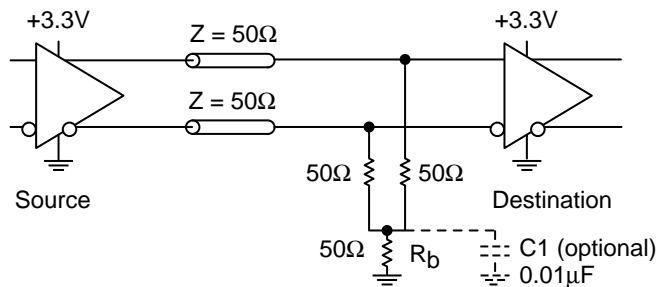


Figure 6b. Three-Resistor "Y-Termination"

Notes:

1. Power-saving alternative to Thevenin termination.
2. Place termination resistors as close to destination inputs as possible.
3. R_b resistor sets the DC bias voltage, equal to V_t . For +3.3V systems $R_b = 46\Omega$ to 50Ω . For +5V systems, $R_b = 110\Omega$.

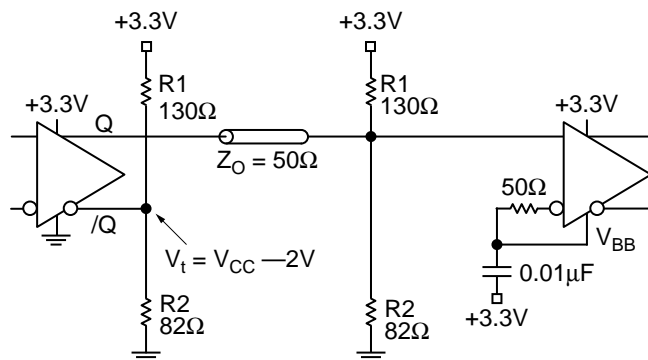


Figure 6c. Terminating Unused I/O

Notes:

1. Unused output (/Q) must be terminated to balance the output.
2. Micrel's differential I/O logic devices include a V_{BB} reference pin.
3. Connect unused input through 50Ω to V_{BB} . Bypass with a $0.01\mu F$ capacitor to V_{CC} , not GND, as PECL is referenced to V_{CC} .

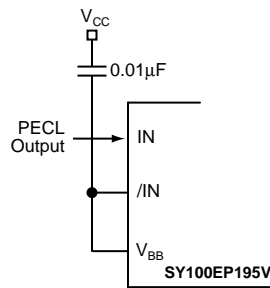


Figure 7a. Interfacing to a Single-Ended PECL Signal

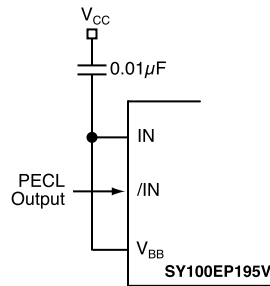


Figure 7b. Interfacing to and Inverting a Single-Ended PECL Signal

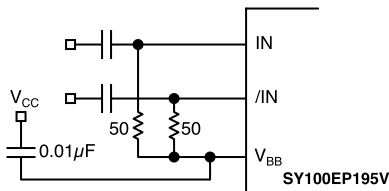


Figure 8. Re-Biasing an AC-Coupled Signal

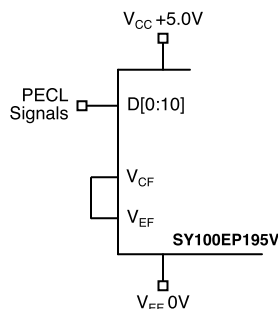


Figure 9a. Connecting PECL Signals to the D Inputs

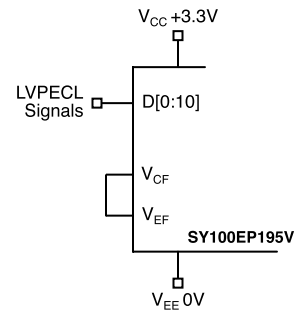


Figure 9b. Connecting LVPECL Signals to the D Inputs

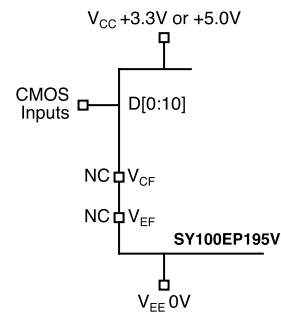


Figure 9c. Connecting CMOS Signals to the D Inputs
Note: V_{CF} and V_{EF} are not connected.

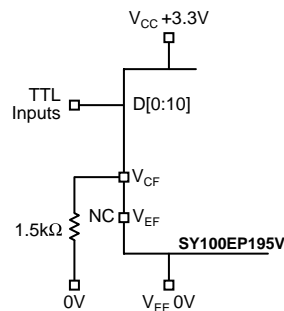


Figure 9d. Connecting TTL Signals to the D Inputs, with $V_{CC} = 3.3V$

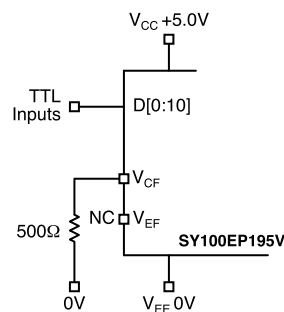


Figure 9e. Connecting TTL Signals to the D Inputs, with $V_{CC} = 5.0V$

FUNCTIONAL DESCRIPTION

SY100EP195V is a programmable delay line, varying the delay of a PECL or NECL input signal by any amount between about 2.2ns and 12.2ns. A 10-bit digital control register affords delay steps of approximately 10ps.

SY100EP195V implements the delay using a multiplexer chain and a set of fixed delay elements. Under digital control, various subsets of the delay elements are included in the signal chain. To simplify interfacing, the 10-bit digital delay control word interfaces to PECL, CMOS, or TTL interface standards.

Since multiplexers must appear in the delay path, SY100EP195V has a minimum delay of about 2.2ns. Delays below this value are not possible. In addition, when cascading multiple SY100EP195V to extend the delay range, the minimum delay is about 2.2ns times the number of SY100EP195V in cascade. An eleventh control bit, D[10], along with the CASCADE and /CASCADE outputs and the SETMIN and SETMAX inputs, simplifies the task of cascading.

Signal Path Logic Standard

The signal path, from IN, /IN to Q, /Q, interfaces to PECL, LVPECL, or NECL signals, as shown in Table 6. The choice of signal path logic standard may limit possible choices for the delay control inputs, D.

Input Enable

The /EN input gates the signal at IN, /IN. When disabled, the input is effectively gated out, just as if a logic low was being provided to SY100EP195V.

| /EN | Value at Q, /Q |
|-----|-------------------|
| L | IN, /IN Delayed |
| H | Logic Low Delayed |

Table 1. /EN Truth Table

Digital Control Latch

SY100EP195V can capture the digital delay control word into its internal 11-bit latch, 10 bits for D[0:9], and an extra bit for the D[10] cascade control. The LEN input controls the action of this latch, as per Table 2.

Note that the LEN input is always PECL, LVPECL, or NECL, the same as the IN, /IN signal pair. The 11-bit delay control word, however, may also be CMOS or TTL.

| LEN | Latch Action |
|-----|----------------------|
| L | Pass Through D[0:10] |
| H | Latch D[0:10] |

Table 2. LEN Truth Table

The nominal delay value is based on the binary value in D[0:9], where D[0] is the least significant bit, and D[9] is the most significant bit. This delay from IN, /IN to Q, /Q is about:

$$\Delta t = 2200 + 10 \times \text{value}(D[9:0]), \text{ ps}$$

Digital Control Logic Standard

When used in systems where V_{EE} connects to ground, SY100EP195V may interface either to PECL, CMOS, or TTL on its D[0:10] inputs. To this end, the V_{CF} pin sets the threshold at which the D inputs switch between logic low and logic high.

As shown in Table 3, connecting V_{CF} to V_{EF} sets the threshold to PECL (if V_{CC} is 5V) or LVPECL (if V_{CC} is 3.3V). Leaving V_{CF} and V_{EF} open yields a threshold suitable for detecting CMOS output logic levels. Leaving V_{EF} open and connecting V_{CF} to a 1.5V source allows the D inputs to accept TTL signals.

| Logic Standard | V_{CF} Connection |
|----------------|---------------------|
| ECL, PECL | V_{EF} |
| CMOS | No Connect |
| TTL | 1.5V Source |

Table 3. Digital Control Standard Truth Table

If a 1.5V source is not available, connecting V_{CF} to V_{EE} through an appropriate resistor will bias V_{CF} at about 1.5V. The value of this resistor depends on the V_{CC} supply, as indicated in Table 4.

| V_{CC} | Resistor Value |
|----------|----------------|
| 3.3V | 1.5k Ω |
| 5.0V | 500 Ω |

Table 4. Resistor Values for TTL Input

Cascade Logic

SY100EP195V is designed to ease cascading multiple devices in order to achieve a greater delay range. The SETMIN and SETMAX pins accomplish this, as set out in the applications section below. SETMIN and SETMAX override the delay by changing the value in the D latch register. Table 5 lists the action of these pins.

| SETMIN | SETMAX | Nominal Delay (ps) |
|--------|--------|-------------------------|
| L | L | As per D Latch |
| L | H | $2200 + 10 \times 1024$ |
| H | L | 2200 |
| H | H | Not Allowed |

Table 5. SETMIN and SETMAX Action

| Signal Path Logic Standard | V _{CC} | V _{EE} | Delay Control Input Choices |
|----------------------------|-----------------|-----------------|-----------------------------|
| PECL | +4.5V to +5.5V | 0V | PECL, CMOS, TTL |
| LVPECL | +3.0V to +3.6V | 0V | LVPECL, CMOS, TTL |
| NECL | 0V | −3.0 to −5.5V | NECL |

Table 6. Signal Path Logic Standard

APPLICATIONS INFORMATION

For best performance, use good high frequency layout techniques, filter V_{CC} supplies, and keep ground connections short. Use multiple vias where possible. Also, use controlled impedance transmission lines to interface with the SY100EP195V data inputs and outputs.

V_{BB} Supply

The V_{BB} pin is an internally generated supply, and is available for use only by the SY100EP195V. When unused, this pin should be left unconnected. The two common uses for V_{BB} are to handle a single-ended PECL input, and to re-bias inputs for AC-coupling applications.

If IN, /IN is driven by a single-ended output, V_{BB} is used to bias the unused input. Please refer to Figures 7. The PECL signal driving SY100EP195V may optionally be inverted in this case.

When the signal is AC-coupled, V_{BB} is used, as shown in Figure 8, to re-bias IN, /IN. This ensures that SY100EP195V inputs are within its acceptable common mode range.

In all cases, V_{BB} current sinking or sourcing must be limited to 0.5mA or less.

Setting D Input Logic Thresholds

As explained earlier, in all designs where the SY100EP195V V_{EE} supply is at zero volts, the D inputs may accommodate CMOS and TTL level signals, as well as PECL or LVPECL. Figures 9 show how to connect V_{CF} and V_{EF} for all possible cases.

Cascading

Two or more SY100EP195V may be cascaded, in order to extend the range of delays permitted. Each additional SY100EP195V adds about 2200ps to the minimum delay, and adds another 10240ps to the delay range.

Internal cascade circuitry has been included in the SY100EP195V. Using this internal circuitry, SY100EP195V may be cascaded without any external gating.

Examples of cascading 2, 3, or 4 SY100EP195V appear in Figures 10. Table 7 lists the nominal delay for all the cases that appear in Figures 10.

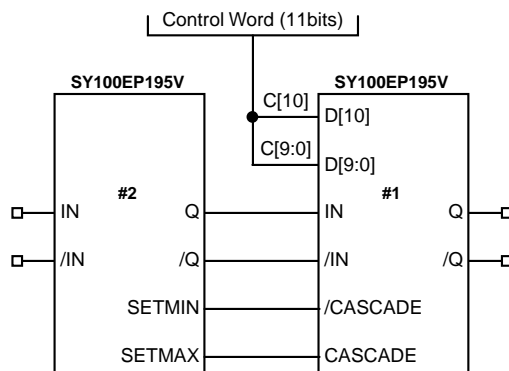


Figure 10a. Cascading Two SY100EP195V

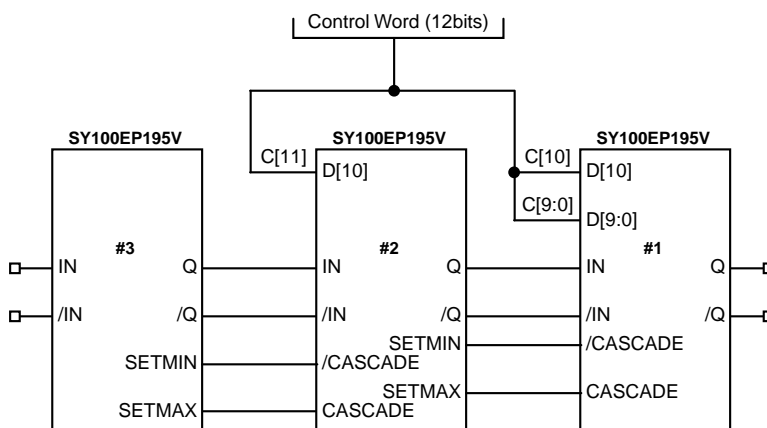


Figure 10b. Cascading Three SY100EP195V

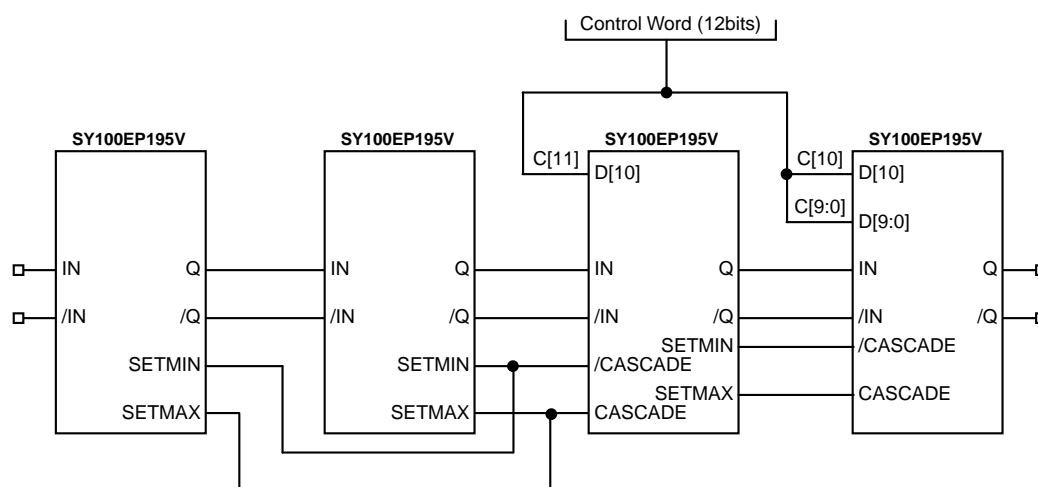


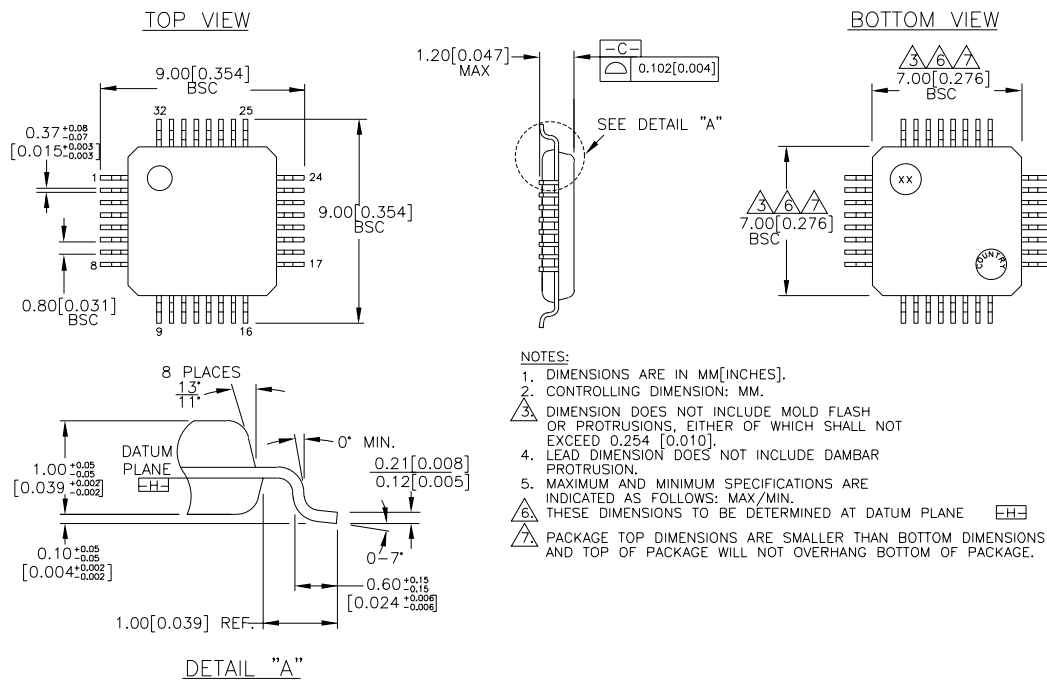
Figure 10c. Cascading Four SY100EP195V

RELATED PRODUCT AND SUPPORT DOCUMENTATION

| Part Number | Function | Data Sheet Link |
|---------------|--|---|
| SY100EP196VTI | 3.3V/5V Programmable Delay Chip with Fine Tune Control | http://www.micrel.com/product-info/products/sy100ep196v.shtml |
| SY55856UHI | 2.5V/3.3V 2.5GHz Differential 2-Channel Precision CML Delay Line | http://www.micrel.com/product-info/products/sy55856u.shtml |

| Control Inputs | | | Nominal Delay (ps) | | | |
|----------------|-------|------------|--------------------|-----------|-------------|------------|
| D[11] | D[10] | D[9:0] | One Chip | Two Chips | Three Chips | Four Chips |
| 0 | 0 | 0000000000 | 2,200 | 4,400 | 6,600 | 8,800 |
| 0 | 0 | 0000000001 | 2,210 | 4,410 | 6,610 | 8,810 |
| 0 | 0 | 0000000010 | 2,220 | 4,420 | 6,620 | 8,820 |
| 0 | 0 | 0000000100 | 2,240 | 4,440 | 6,640 | 8,840 |
| 0 | 0 | 0000001000 | 2,280 | 4,480 | 6,680 | 8,880 |
| 0 | 0 | 0000010000 | 2,360 | 4,560 | 6,760 | 8,960 |
| 0 | 0 | 0000100000 | 2,520 | 4,720 | 6,920 | 9,120 |
| 0 | 0 | 0001000000 | 2,840 | 5,040 | 7,240 | 9,440 |
| 0 | 0 | 0010000000 | 3,480 | 5,680 | 7,880 | 10,080 |
| 0 | 0 | 0100000000 | 4,760 | 6,960 | 9,160 | 11,360 |
| 0 | 0 | 1000000000 | 7,320 | 9,520 | 11,720 | 13,920 |
| 0 | 0 | 1111111111 | 12,430 | 14,630 | 16,830 | 19,030 |
| 0 | 1 | 0000000000 | | 14,640 | 16,840 | 19,040 |
| 0 | 1 | 0000000001 | | 14,650 | 16,850 | 19,050 |
| 0 | 1 | 0000000010 | | 14,660 | 16,860 | 19,060 |
| 0 | 1 | 0000000100 | | 14,680 | 16,880 | 19,080 |
| 0 | 1 | 0000001000 | | 14,720 | 16,920 | 19,120 |
| 0 | 1 | 0000010000 | | 14,800 | 17,000 | 19,200 |
| 0 | 1 | 0000100000 | | 14,960 | 17,160 | 19,360 |
| 0 | 1 | 0001000000 | | 15,280 | 17,480 | 19,680 |
| 0 | 1 | 0010000000 | | 15,920 | 18,120 | 20,320 |
| 0 | 1 | 0100000000 | | 17,200 | 19,400 | 21,600 |
| 0 | 1 | 1000000000 | | 19,760 | 21,960 | 24,160 |
| 0 | 1 | 1111111111 | | 24,870 | 27,070 | 29,270 |
| 1 | 0 | 0000000000 | | | 27,080 | 29,280 |
| 1 | 0 | 0000000001 | | | 27,090 | 29,290 |
| 1 | 0 | 0000000010 | | | 27,100 | 29,300 |
| 1 | 0 | 0000000100 | | | 27,120 | 29,320 |
| 1 | 0 | 0000001000 | | | 27,160 | 29,360 |
| 1 | 0 | 0000010000 | | | 27,240 | 29,440 |
| 1 | 0 | 0000100000 | | | 27,400 | 29,600 |
| 1 | 0 | 0001000000 | | | 27,720 | 29,920 |
| 1 | 0 | 0010000000 | | | 28,360 | 30,560 |
| 1 | 0 | 0100000000 | | | 29,640 | 31,840 |
| 1 | 0 | 1000000000 | | | 32,200 | 34,400 |
| 1 | 0 | 1111111111 | | | 37,310 | 39,510 |
| 1 | 1 | 0000000000 | | | 27,080 | 39,520 |
| 1 | 1 | 0000000001 | | | 27,090 | 39,530 |
| 1 | 1 | 0000000010 | | | 27,100 | 39,540 |
| 1 | 1 | 0000000100 | | | 27,120 | 39,560 |
| 1 | 1 | 0000001000 | | | 27,160 | 39,600 |
| 1 | 1 | 0000010000 | | | 27,240 | 39,680 |
| 1 | 1 | 0000100000 | | | 27,400 | 39,840 |
| 1 | 1 | 0001000000 | | | 27,720 | 40,160 |
| 1 | 1 | 0010000000 | | | 28,360 | 40,800 |
| 1 | 1 | 0100000000 | | | 29,640 | 42,080 |
| 1 | 1 | 1000000000 | | | 32,200 | 44,640 |
| 1 | 1 | 1111111111 | | | 37,310 | 49,750 |

Table 7. List of Nominal Delay Values for Cascaded SY100EP195V

32 LEAD TQFP (T32-1)

Rev. 01

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