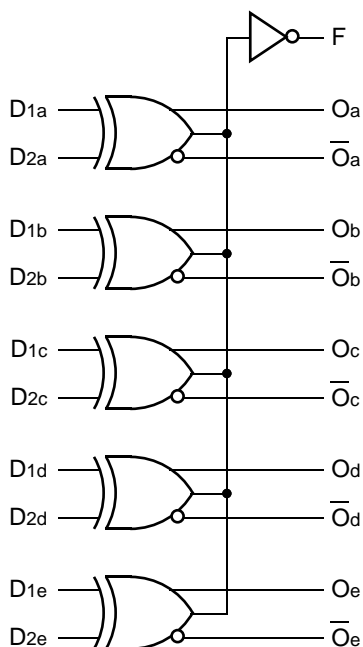


### FEATURES

- Max. propagation delay of 1000ps
- IEE min. of -58mA
- Extended supply voltage option:  
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75K $\Omega$  input pull-down resistors
- 50% faster than Fairchild 300K at lower power
- Function and pinout compatible with Fairchild F100K
- Available in 24-pin CERPACK and 28-pin PLCC packages

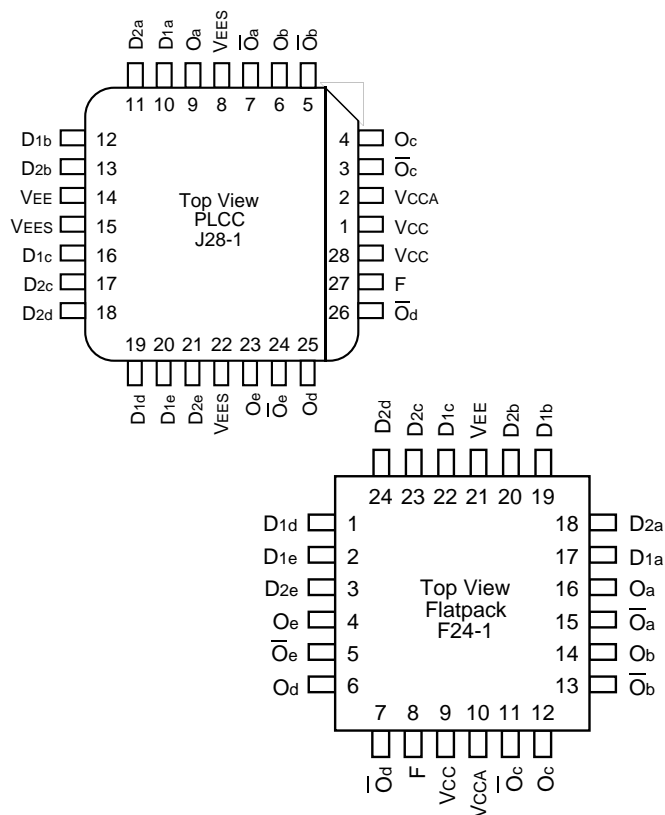
### BLOCK DIAGRAM



### DESCRIPTION

The SY100S307 is an ultra-fast quint exclusive-OR/NOR gate designed for use in high-performance ECL systems. A function output that is the wire-OR result of the exclusive-OR outputs is also available. The inputs on the device have 75K $\Omega$  pull-down resistors.

### PIN CONFIGURATIONS



### PIN NAMES

Pin	Function
Dna - Dne	Data Inputs (n-1...5)
E	Enable Input
Oa - Oe	Data Outputs
$\overline{Oa} - \overline{Oe}$	Complementary Data Outputs
VEES	VEE Substrate
VCCA	Vcco for ECL Outputs

## LOGIC EQUATION

$$F = (D1a \oplus D2a) + (D1b \oplus D2b) + (D1c \oplus D2c) + (D1d \oplus D2d) + (D1e \oplus D2e).$$

## DC ELECTRICAL CHARACTERISTICS

$V_{EE} = -4.2V$  to  $-5.5V$  unless otherwise specified,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
$I_{IH}$	Input HIGH Current D2a — D2e D2a — D2e	— —	— —	200 250	$\mu A$	$V_{IN} = V_{IH} (Max.)$
$I_{EE}$	Power Supply Current	-58	-40	-27	mA	Inputs Open

## AC ELECTRICAL CHARACTERISTICS

### CERPACK

$V_{EE} = -4.2V$  to  $-5.5V$  unless otherwise specified,  $V_{CC} = V_{CCA} = GND$

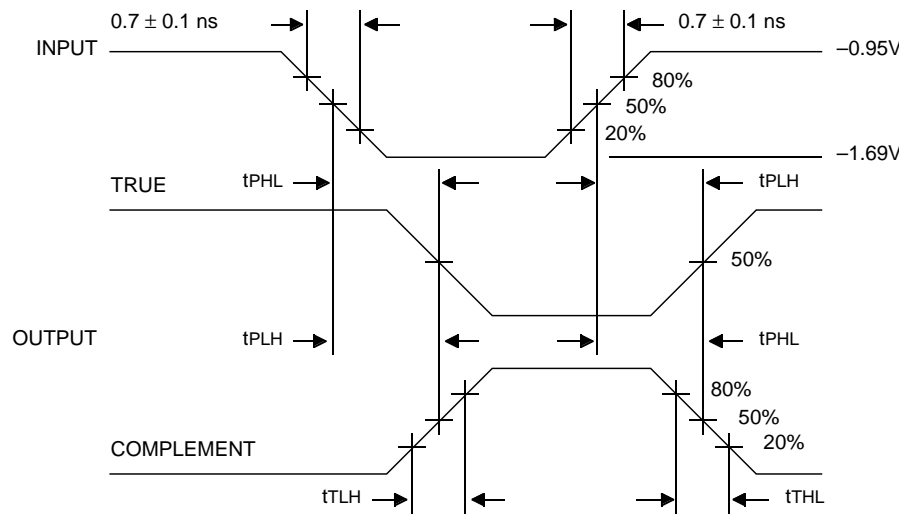
Symbol	Parameter	$T_A = 0^{\circ}C$		$T_A = +25^{\circ}C$		$T_A = +85^{\circ}C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
$t_{PLH}$ $t_{PH2}$	Propagation Delay D2a — D2e to O, $\bar{O}$	200	1100	200	1150	200	1100	ps	
$t_{PLH}$ $t_{PHL}$	Propagation Delay D1a — D1e to O, $\bar{O}$	200	1000	200	950	200	1000	ps	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Data to F	300	1525	300	1525	300	1525	ps	
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

### PLCC

$V_{EE} = -4.2V$  to  $-5.5V$  unless otherwise specified,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_A = 0^{\circ}C$		$T_A = +25^{\circ}C$		$T_A = +85^{\circ}C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
$t_{PLH}$ $t_{PH2}$	Propagation Delay D2a — D2e to O, $\bar{O}$	300	1000	300	1000	300	1000	ps	
$t_{PLH}$ $t_{PHL}$	Propagation Delay D1a — D1e to O, $\bar{O}$	300	900	300	900	300	930	ps	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Data to F	300	1425	300	1425	300	1425	ps	
$t_{TLH}$ $t_{THL}$	Transition Time 3 20% to 80%, 80% to 20%	00	900	300	900	300	900	ps	

TIMING DIAGRAM



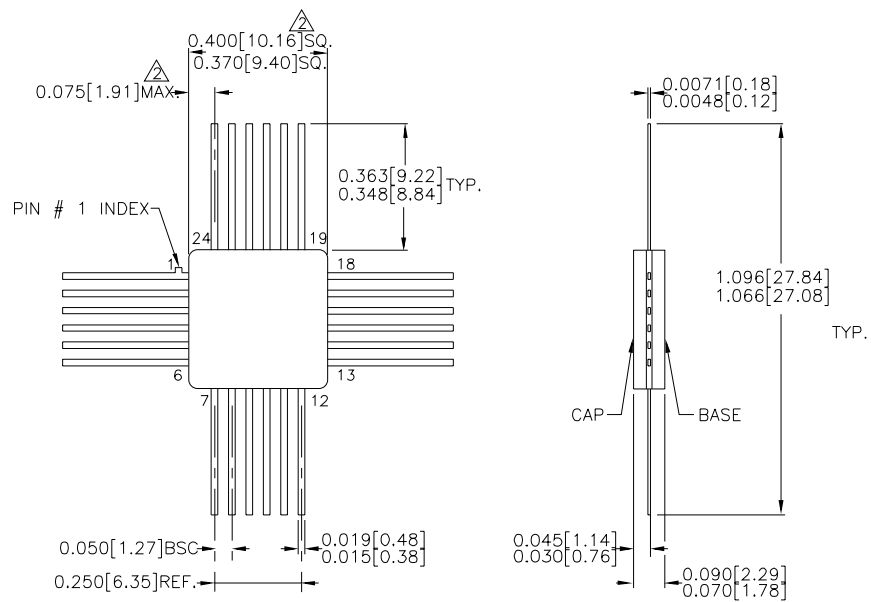
Propagation Delay and Transition Times

**NOTE:**  
 $V_{EE} = -4.2V$  to  $-5.5V$  unless otherwise specified,  $V_{CC} = V_{CCA} = GND$

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S307FC	F24-1	Commercial
SY100S307JC	J28-1	Commercial
SY100S307JCTR	J28-1	Commercial

## 24 LEAD CERPACK (F24-1)

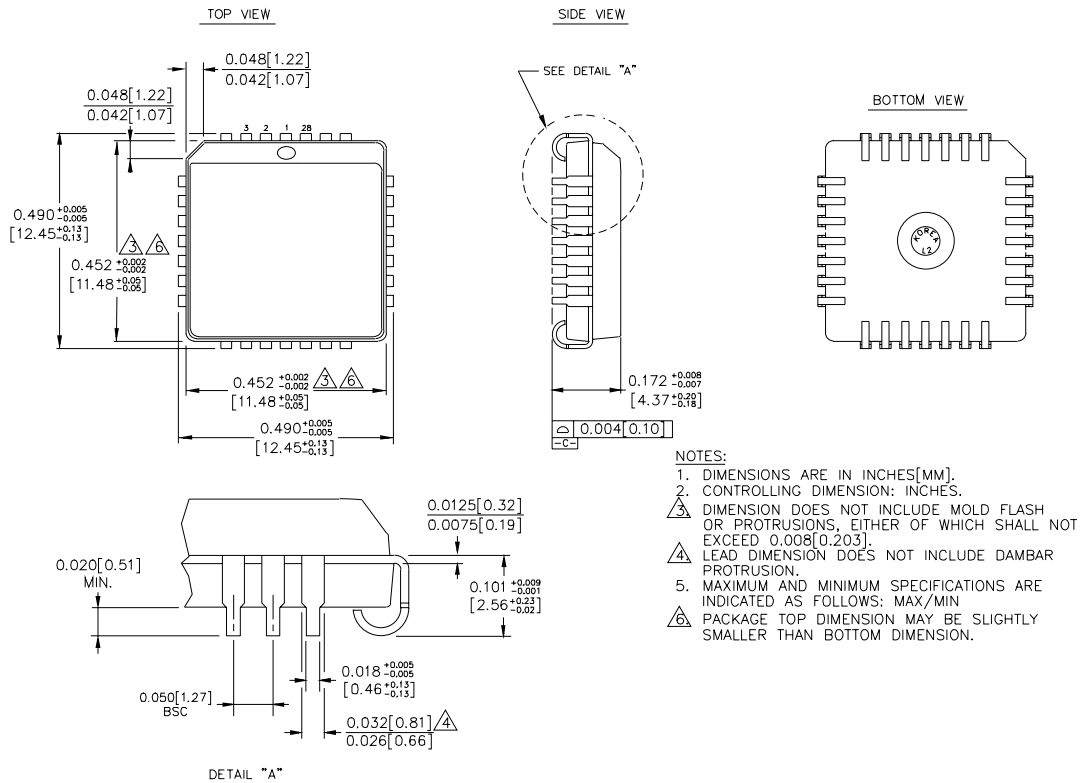


### NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

Rev. 03

## 28 LEAD PLCC (J28-1)



Rev. 03

**MICREL-SYNERGY 3250 SCOTT BOULEVARD SANTA CLARA CA 95054 USA**

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