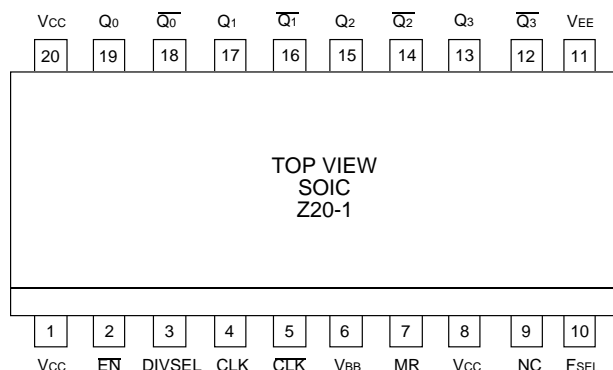


FEATURES

- 3.3V and 5V power supply options
- 50ps output-to-output skew
- Synchronous enable/disable
- Master Reset for synchronization
- Internal 75KΩ input pull-down resistors
- Available in 20-pin SOIC package

PIN CONFIGURATION



TRUTH TABLE

CLK	EN	MR	Function
Z	L	L	Divide
ZZ	H	L	Hold Q0-3
X	X	H	Reset Q0-3

NOTES:

Z = LOW-to-HIGH transition

ZZ = HIGH-to-LOW transition

FSEL	DIVSEL	Q0, Q1 OUTPUTS	Q2, Q3 OUTPUTS
L	L	Divide by 2	Divide by 4
L	H	Divide by 2	Divide by 6
H	L	Divide by 1	Divide by 2
H	H	Divide by 1	Divide by 3

DESCRIPTION

The SY100S838/L is a low skew (÷1, ÷2/3) or (÷2, ÷4/6) clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The devices can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal. In addition, by using the VBB output, a sinusoidal source can be AC-coupled into the device. If a single-ended input is to be used, the VBB output should be connected to the CLK input and bypassed to ground via a 0.01μF capacitor. The VBB output is designed to act as the switching reference for the input of the SY100S838/L under single-ended input conditions. As a result, this pin can only source/sink up to 0.5mA of current.

The Function Select (FSEL) input is used to determine what clock generation chip function is. When FSEL input is LOW, SY100S838/L functions as a divide by 2 and by 4/6 clock generation chip. However, if FSEL input is HIGH, it functions as a divide by 1 and by 2/3 clock chip.

The common enable (EN) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

Upon start-up, the internal flip-flops will attain a random state; the master reset (MR) input allows for the synchronization of the internal dividers, as well as for multiple SY100S838/Ls in a system.

PIN NAMES

Pin	Function
CLK	Differential Clock Inputs
FSEL	Function Select Input
EN	Synchronous Enable
MR	Master Reset
VBB	Reference Output
Q0, Q1	Differential ÷1 or ÷2 Outputs
Q2, Q3	Differential ÷2/3 or ÷4/6 Outputs
DIVSEL	Frequency Select Input

$V_{EE} = V_{EE} \text{ (Min.) to } V_{EE} \text{ (Max.)}; V_{CC} = \text{GND}$

Symbol	Parameter	T _A = -40°C			T _A = 0°C			T _A = +25°C			T _A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I _{EE}	Power Supply Current	35	50	65	35	50	65	35	50	65	35	54	75	mA
V _{BB}	Output Reference Voltage	-1.38	—	-1.26	-1.38	—	-1.26	-1.38	—	-1.26	-1.38	—	-1.26	V
I _{IH}	Input High Current	—	—	150	—	—	150	—	—	150	—	—	150	μA

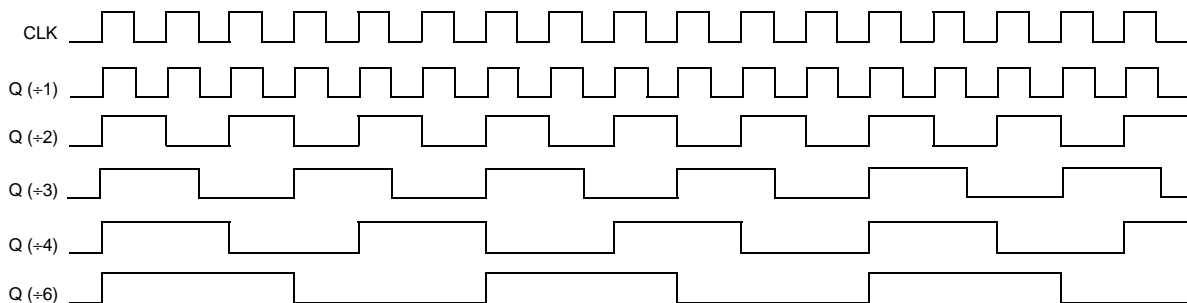
1. Parametric values specified at:	5 volt Power Supply Range	100S838 Series:	-4.2V to -5.5V.
	3 volt Power Supply Range	100S838L Series	-3.0V to -3.8V.

AC ELECTRICAL CHARACTERISTICS⁽¹⁾V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

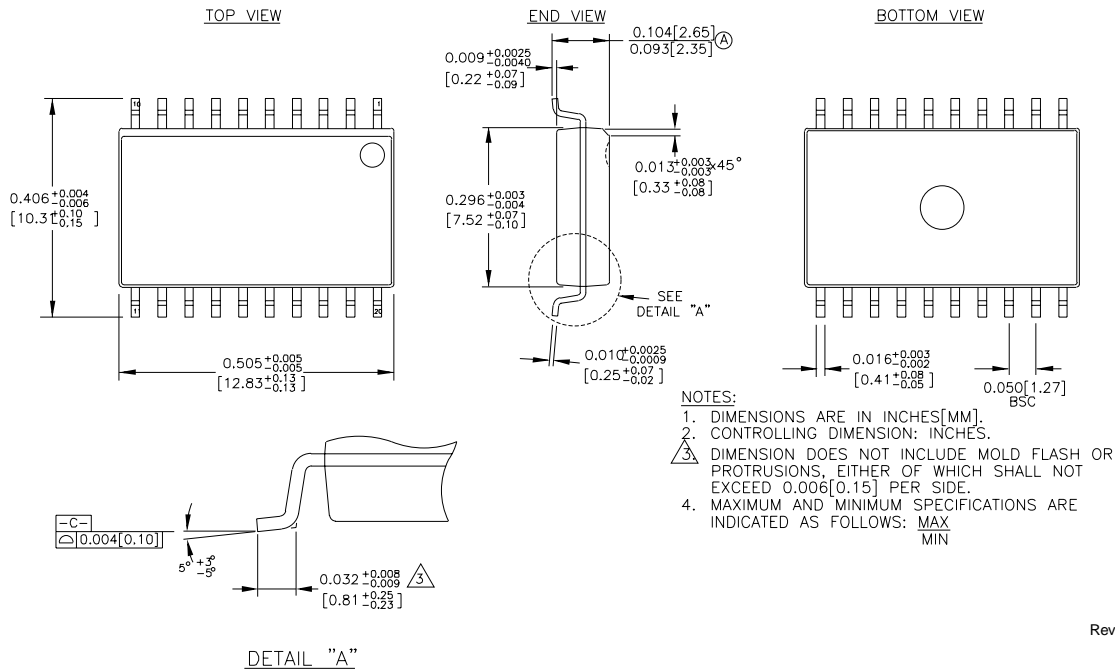
Symbol	Parameter	T _A = -40°C			T _A = 0°C			T _A = +25°C			T _A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
f _{MAX}	Maximum Toggle Frequency	1000	—	—	1000	—	—	1000	—	—	1000	—	—	MHz
t _{PLH} t _{PHL}	Propagation Delay to Output CLK → Output (Diff.) CLK → Output (S.E.) MR → Q	950 900 600	— — —	1150 1200 900	950 900 600	— — —	1150 1200 900	970 920 600	— — —	1170 1220 900	1050 1000 600	— — —	1250 1300 900	ps
tskew	Within-Device Skew ⁽²⁾ Q0 — Q3	—	—	50	—	—	50	—	—	50	—	—	50	ps
	Part-to-Part Q0 — Q3 (Diff.)	—	—	200	—	—	200	—	—	200	—	—	200	
ts	Set-up Time $\overline{\text{EN}} \rightarrow \overline{\text{CLK}}$	300	150	—	300	150	—	300	150	—	300	150	—	ps
	DIVSEL → CLK	300	—	—	300	—	—	300	—	—	300	—	—	
t _H	Hold Time $\overline{\text{CLK}} \rightarrow \overline{\text{EN}}$	400	150	—	400	150	—	400	150	—	400	150	—	ps
	CLK → DIVSEL	400	200	—	400	200	—	400	200	—	400	200	—	
V _{PP}	Minimum Input Swing ⁽³⁾ CLK	250	—	—	250	—	—	250	—	—	250	—	—	mV
V _{CMR}	Common Mode Range ⁽⁴⁾ CLK	(4)	—	-0.55	(4)	—	-0.55	(4)	—	-0.55	(4)	—	-0.55	V
t _{RR}	Reset Recovery Time	—	—	100	—	—	100	—	—	100	—	—	100	ps
t _{PW}	Minimum Pulse Width CLK	800	—	—	800	—	—	800	—	—	800	—	—	ps
	MR	700	—	—	700	—	—	700	—	—	700	—	—	
t _r t _f	Output Rise/Fall Times (20% — 80%) Q	280	—	550	280	—	550	280	—	550	280	—	550	ps

NOTES:

- Parametric values specified at: 5 volt Power Supply Range 100S838 Series: -4.2V to -5.5V.
3 volt Power Supply Range 100S838L Series: -3.0V to -3.8V.
- Skew is measured between outputs under identical transitions.
- Minimum input swing for which AC parameters are guaranteed. The device will function reliably with differential inputs down to 100mV.
- The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP} (min) and 1.0V. The lower end of the CMR range is dependent on V_{EE} and is equal to V_{EE} + 1.65V.

TIMING DIAGRAM**PRODUCT ORDERING CODE**

Ordering Code	Package Type	Operating Range	V _{EE} Range (V)	Ordering Code	Package Type	Operating Range	V _{EE} Range (V)
SY100S838ZC	Z20-1	Commercial	-4.2 to -5.5	SY100S838ZI	Z20-1	Industrial	-4.2 to -5.5
SY100S838ZCTR	Z20-1	Commercial	-4.2 to -5.5	SY100S838ZITR	Z20-1	Industrial	-4.2 to -5.5
SY100S838LZC	Z20-1	Commercial	-3.0 to -3.8	SY100S838LZI	Z20-1	Industrial	-3.0 to -3.8
SY100S838LZCTR	Z20-1	Commercial	-3.0 to -3.8	SY100S838LZITR	Z20-1	Industrial	-3.0 to -3.8

20 LEAD SOIC .300" WIDE (Z20-1)

Rev. 03

MICREL-SYNERGY 3250 SCOTT BOULEVARD SANTA CLARA CA 95054 USATEL + 1 (408) 980-9191 FAX + 1 (408) 914-7878 WEB <http://www.micrel.com>

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