

## FEATURES

- 3.0ns typical propagation delay
- <500ps typical output-to-output skew
- Differential PECL inputs
- 24mA TTL outputs
- Flow-through pinouts
- Available in 8-pin SOIC package



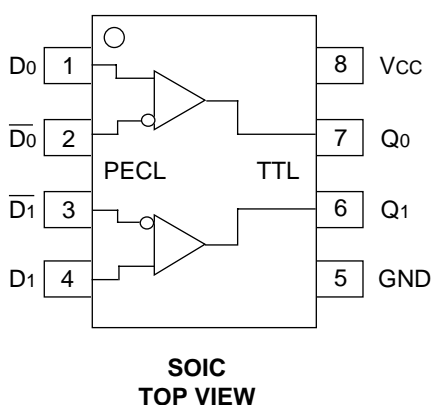
Precision Edge™

## DESCRIPTION

The SY10/100ELT23 are dual differential PECL-to-TTL translators. Because PECL (Positive ECL) levels are used, only +5V and ground are required. The small outline 8-lead SOIC package and the low skew dual gate design of the ELT23 makes it ideal for applications which require the translation of a clock and a data signal.

The ELT23 is available in both ECL standards: the 10ELT is compatible with positive ECL 10H logic levels, while the 100ELT is compatible with positive ECL 100K logic levels.

## PIN CONFIGURATION/BLOCK DIAGRAM



## PIN NAMES

Pin	Function
Q <sub>n</sub>	TTL Outputs
D <sub>n</sub>	Differential PECL Inputs
V <sub>cc</sub>	+5.0V Supply
GND	Ground

## TRUTH TABLE

<b>D</b>	<b><math>\bar{D}</math></b>	<b>Q</b>
L	H	L
H	L	H
Open	Open	L

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

Symbol	Parameter	T <sub>A</sub> = -40°C		T <sub>A</sub> = 0°C		T <sub>A</sub> = +25°C		T <sub>A</sub> = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
I <sub>CC</sub>	Power Supply Current	—	30	—	30	—	30	—	30	mA	—

1. Parametric values specified at:	5 volt Power Supply Range	100ELT23 Series:	+4.5V to +5.5V.
		10ELT23 Series	+4.75V to +5.5V.

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		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
tPLH tPHL	Propagation Delay D to Output Q	2.5	3.5	2.5	3.5	2.5	3.5	2.5	3.5	ns	CL = 50pF
tskpp	Part-to-Part Skew <sup>(2,5)</sup>	—	0.5	—	0.5	—	0.5	—	0.5	ns	CL = 50pF
tskew++	Within-Device Skew <sup>(3,5)</sup>	—	0.3	—	0.3	—	0.3	—	0.3	ns	CL = 50pF
tskew--	Within-Device Skew <sup>(4,5)</sup>	—	0.3	—	0.3	—	0.3	—	0.3	ns	CL = 50pF
tr tf	Output Rise/Fall Time 1.0V to 2.0V	—	1.5	—	1.5	—	1.5	—	1.5	ns	CL = 50pF
fMAX	Maximum Input Frequency <sup>(5)</sup>	160	—	160	—	160	—	160	—	MHz	CL = 50pF

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2. Device-to-Device Skew considering HIGH-to-HIGH transitions at common Vcc level.
3. Within-Device Skew considering HIGH-to-HIGH transitions at common Vcc level.
4. Within-Device Skew considering LOW-to-LOW transitions at common Vcc level.
5. These parameters are guaranteed but not tested.

VCC = VCC (Min.) to VCC (Max.)

**NOTE:**

- |                                    |                           |                  |                  |
|------------------------------------|---------------------------|------------------|------------------|
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|                                    |                           | 10ELT23 Series   | +4.75V to +5.5V. |

VCC = VCC (Min.) to VCC (Max.)

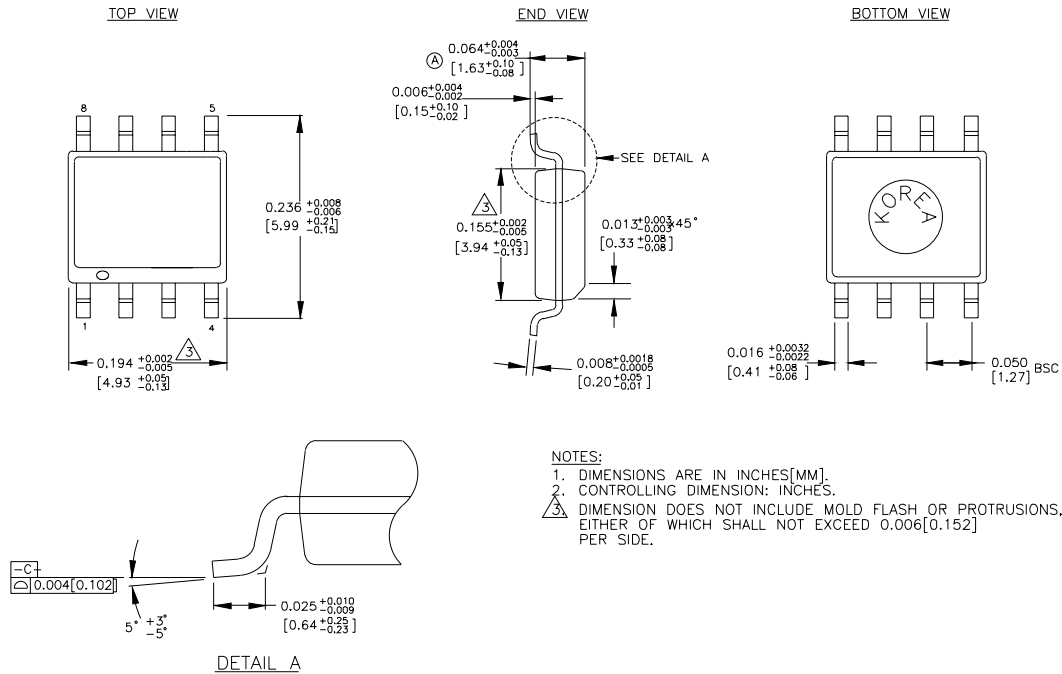
**NOTES:**

1. Parametric values specified at: 5 volt Power Supply Range 100ELT23 Series: +4.5V to +5.5V.  
10ELT23 Series +4.75V to +5.5V.
2. 200mV input guarantees full logic at output.
3. These values are for Vcc = 5.0V. Level Specifications will vary 1:1 Vcc.

Ordering Code	Package Type	Operating Range	Marking Code
SY10ELT23ZI <sup>(1)</sup>	Z8-1	Industrial	HEL23
SY10ELT23ZITR <sup>*(1)</sup>	Z8-1	Industrial	HEL23
SY100ELT23ZI <sup>(1)</sup>	Z8-1	Industrial	XEL23
SY100ELT23ZITR <sup>*(1)</sup>	Z8-1	Industrial	XEL23

\*Tape and Reel

**Note 1.** Recommended for new designs.

**8 LEAD SOIC .150" WIDE (Z8-1)**

Rev. 03

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