

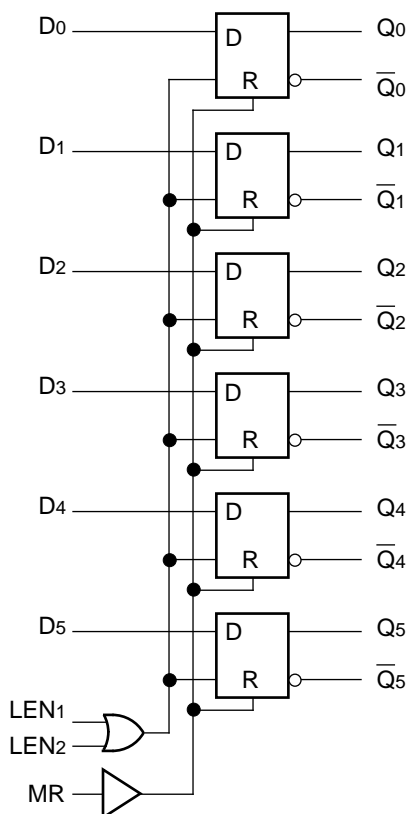
FEATURES

- 700ps max. propagation delay
- Extended 100E VEE range of $-4.2V$ to $-5.5V$
- Differential outputs
- Fully compatible with industry standard 10KH, 100K ECL levels
- Internal 75K Ω input pulldown resistors
- Fully compatible with Motorola MC10E/100E150
- Available in 28-pin PLCC package

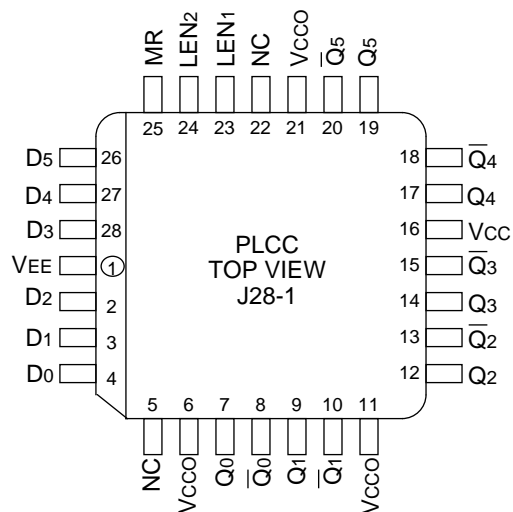
DESCRIPTION

The SY10/100E150 are 6-bit D latches with differential outputs designed for use in new, high- performance ECL systems. When both Latch Enables (LEN₁, LEN₂) are at a logic LOW, the latch is in the transparent mode and input data propagates through to the output. A logic HIGH on either LEN₁ or LEN₂ (or both) latches the input data. The Master Reset (MR) overrides all other signals to set the Q outputs to a logic LOW.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin	Function
D0–D5	Data Inputs
LEN1, LEN2	Latch Enables
MR	Master Reset
Q0–Q5	True Outputs
$\overline{Q}0$ – $\overline{Q}5$	Inverting Outputs
VCCO	Vcc to Output

TRUTH TABLE⁽¹⁾

(Each Latch)

INPUTS				OUTPUTS		Operating Mode
D _n	LEN ₁	LEN ₂	MR	Q _n	\overline{Q}_n	
H	L	L	L	H	L	Latch
L	L	L	L	L	H	
X	X	H	L	Latched ⁽²⁾	Latched ⁽²⁾	
X	H	X	L	Latched ⁽²⁾	Latched ⁽²⁾	
X	X	X	H	L	H	Asynchronous

NOTES:

1. H = HIGH state
L = LOW state
X = Don't care
2. Retains Data that is present before the LEN positive transition.

DC ELECTRICAL CHARACTERISTICSV_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T _A = 0°C			T _A = +25°C			T _A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I _{IH}	Input HIGH Current D LEN MR	—	—	200 150	—	—	200 150	—	—	200 150	μA	—
I _{EE}	Power Supply Current 10E 100E	—	52 52	62 62	—	52 52	62 62	—	52 60	62 72	mA	—

AC ELECTRICAL CHARACTERISTICS

VEE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

Symbol	Parameter	TA = 0°C			TA = +25°C			TA = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
tPLH tPHL	Propagation Delay to Output D LEN MR	250 375 450	375 500 625	550 700 750	250 375 450	375 500 625	550 700 750	250 375 450	375 500 625	550 700 750	ps	—
ts	Set-up Time, D	200	50	—	200	50	—	200	50	—	ps	—
tH	Hold Time, D	200	–50	—	200	–50	—	200	–50	—	ps	—
tRR	Reset Recovery Time	750	650	—	750	650	—	750	650	—	ps	—
tPW	Minimum Pulse Width, MR	400	—	—	400	—	—	400	—	—	ps	—
tskew	Within-Device Skew	—	50	—	—	50	—	—	50	—	ps	1
tr tf	Rise/Fall Time 20% to 80%	300	450	650	300	450	650	300	450	650	ps	—

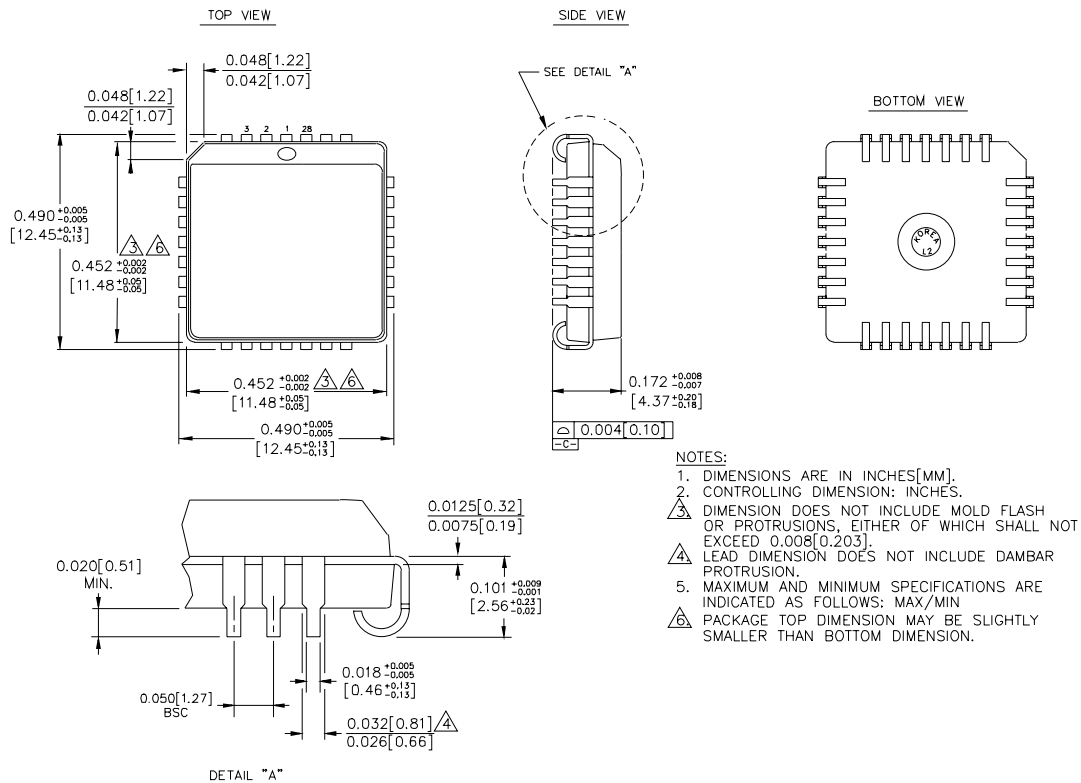
NOTE:

1. Within-device skew is defined as identical transitions on similar paths through a device.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E150JC	J28-1	Commercial
SY10E150JCTR	J28-1	Commercial
SY100E150JC	J28-1	Commercial
SY100E150JCTR	J28-1	Commercial

28 LEAD PLCC (J28-1)



Rev. 03

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