

FEATURES

- 9-bit ideal for byte-parity applications
- Flow-through configuration
- Extra TTL and ECL power/ground pins to minimize switching noise
- Dual supply
- 3.5ns max. D to Q
- PNP TTL inputs for low loading
- Choice of ECL compatibility: MECL 10KH (10Hxxx) or 100K (100Hxxx)
- Fully compatible with Motorola MC10H/100H602
- Available in 28-pin PLCC package

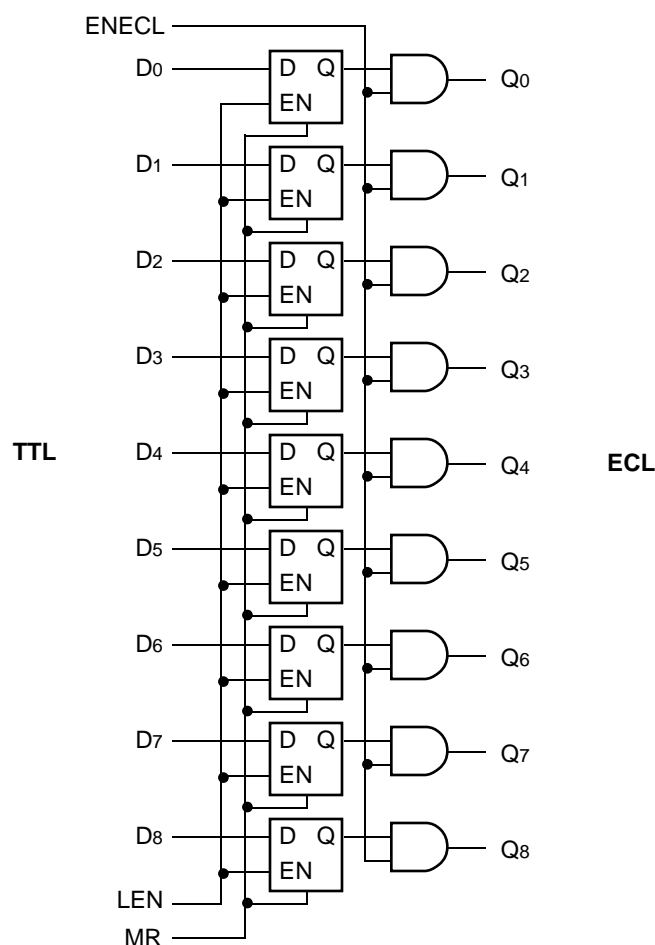
DESCRIPTION

The SY10/100H602 are 9-bit, dual supply TTL-to-ECL translators with latches. Devices in the Micrel-Synergy 9-bit translator series utilize the 28-lead PLCC for optimal power pinning, signal flow-through and electrical performance.

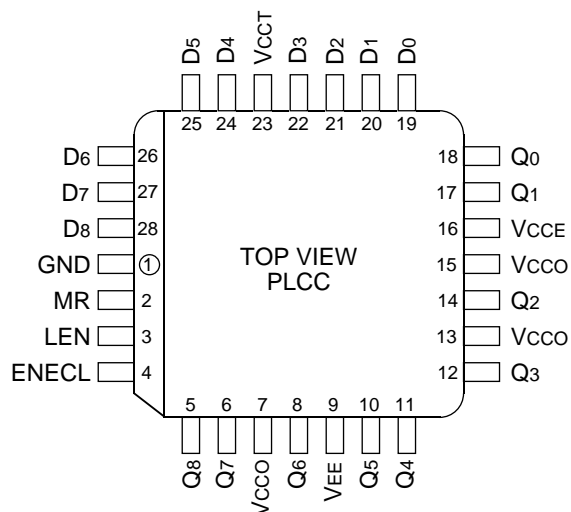
The H602 features D-type latches. Latching is controlled by Latch Enable (LEN), while the Master Reset input resets the latches. A post-latch logic enable is also provided (ENECL), allowing control of the output state without destroying latch data. All control inputs are ECL level.

The 10H version is compatible with MECL 10KH ECL logic levels. The 100H version is compatible with 100K levels.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin	Function
GND	TTL Ground (0V)
VCC	ECL Vcc (0V)
VCCO	ECL Vcc (0V) — Outputs
VCC	TTL Supply (+5.0V)
VEE	ECL Supply (–5.2/–4.5V)
D0–D8	Data Inputs (TTL)
Q0–Q8	Data Outputs (ECL)
ENECL	Enable Control (ECL)
LEN	Latch Enable (ECL)
MR	Master Reset (ECL)

TRUTH TABLE

D	LEN	MR	ENECL	Q
L	L	L	H	L
H	L	L	H	H
X	H	L	H	Q ₀
X	X	H	H	L
X	X	X	L	L

DC ELECTRICAL CHARACTERISTICS

VCCT = 5.0V ± 10%; VEE = -4.75V to -5.5V (10H Version); VEE = -4.2V to -5.5V (100H Version)

Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
IEE	Power Supply Current, ECL 10H 100H	—	125	—	125	—	125	mA	—
		—	122	—	123	—	132		
ICCH ICCL	Power Supply Current, TTL	—	48	—	48	—	48	mA	—
		—	50	—	50	—	50		

AC ELECTRICAL CHARACTERISTICS

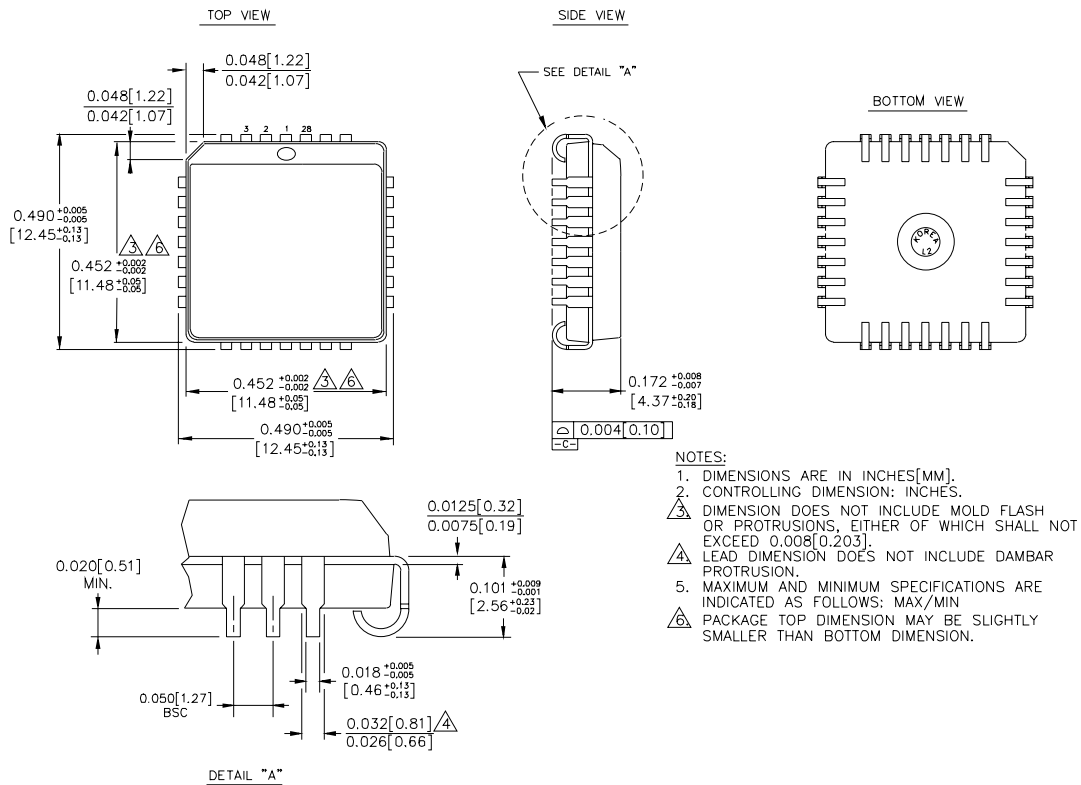
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Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
tPLH tPHL	Propagation Delay to Output D LEN MR ENECL	1.4 2.0 2.0 1.6	3.0 3.4 3.4 3.2	1.5 2.1 2.1 1.7	3.2 3.5 3.5 3.3	1.7 2.4 2.5 1.8	3.5 3.7 3.9 3.7	ns	—
ts	Set-up Time, D to LEN	2.0	—	2.0	—	2.0	—		
tH	Hold Time, D to LEN	1.0	—	1.0	—	1.0	—		
tw(L)	LEN Pulse Width, LOW	2.0	—	2.0	—	2.0	—		
tr tf	Output Rise/Fall Time 20% to 80%, 80% to 20%	0.5	1.5	0.5	1.5	0.5	1.5	ns	—

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10H602JC	J28-1	Commercial
SY10H602JCTR	J28-1	Commercial
SY100H602JC	J28-1	Commercial
SY100H602JCTR	J28-1	Commercial

28 LEAD PLCC (J28-1)



Rev. 03

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