

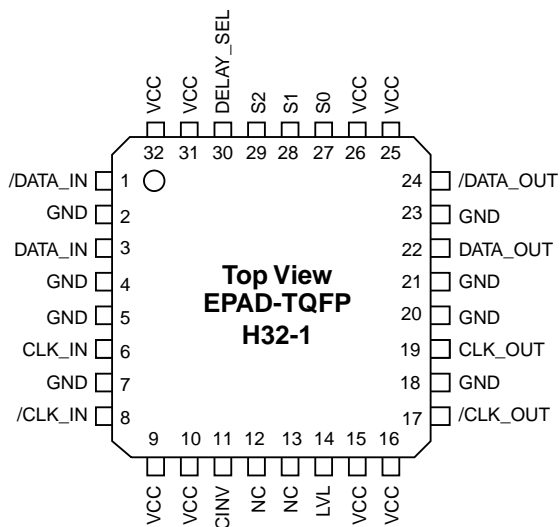
FEATURES

- **Guaranteed AC parameters over temp and voltage**
 - > 2.5GHz F_{MAX}
 - < 384ps prop delay
 - < 120ps T_r/T_f
- **Delay either clock or data**
- **50ps increments**
- **± 350ps total delay**
- **Delay either clock or data**
- **Source terminated CML outputs**
- **Full differential I/O**
- **Wide supply voltage spectrum: 2.3V to 3.6V**
- **Available in a tiny 32-pin EPAD-TQFP package**

APPLICATIONS

- **Data communications systems**
- **Telecom systems**
- **High-speed backplanes**
- **Signal de-skewing**
- **Pulse alignment**
- **Digitally controlled delay lines**

PIN CONFIGURATION



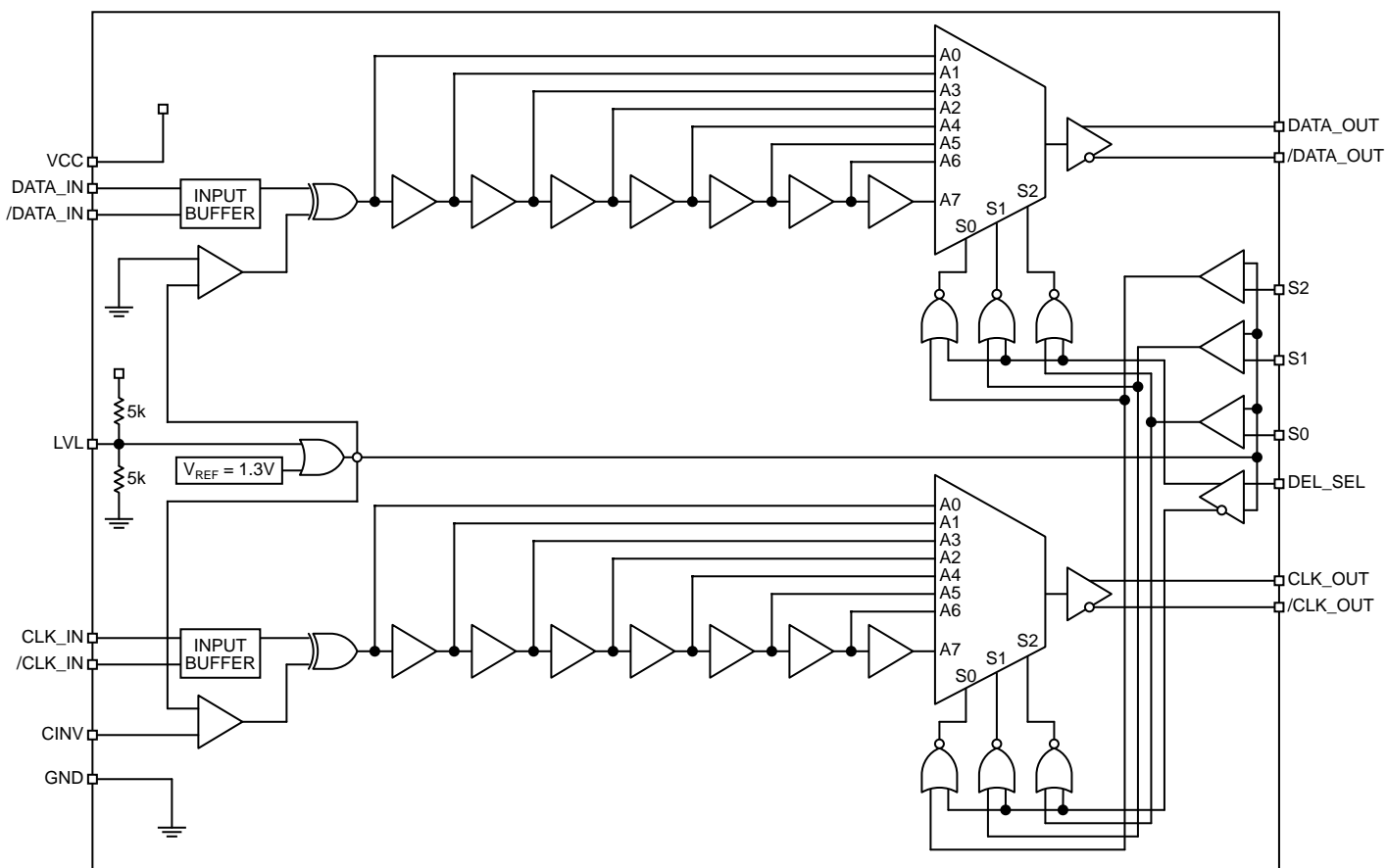
DESCRIPTION

The SY55856U is a 2.5GHz, two-channel, fully differential CML (Current Mode Logic) delay line. The device is optimized to adjust the relative delay between two channels, such as clock and data, in 50ps increments. Both inputs may be adjusted in either direction in 7 increments of 50ps, for a total adjustment range of ±350ps. In addition, the clock input maybe inverted through the CINV control pin.

The SY55856U inputs are designed to accept single-ended or differential CML signals. The differential CML outputs are optimized for 50Ω loads (50Ω source terminated), thus only requires a single 100Ω resistor across the output pair. Output rise and fall time is an extremely fast 110ps(max) and the differential swing is 400mV. The maximum throughput of the SY55856U is guaranteed to exceed 2.5GHz (1.25Gbps).

PIN NAMES

| Pin | Function |
|---------------------|---|
| CLK_IN, /CLK_IN | Differential Clock Input (CML compatible) |
| CLK_OUT, /CLK_OUT | Differential Clock Output (CML) |
| CINV | Clock Inversion Control (CML compatible) |
| DATA_IN, /DATA_IN | Differential Data Input (CML compatible) |
| DATA_OUT, /DATA_OUT | Differential Data Output (CML) |
| LVL | Control Level Select (CML compatible) |
| DELAY_SEL | Delay Path Control (CML compatible) |
| S2, S1, S0 | Delay Selection Control (LSB=S0) |
| GND | Ground |
| V _{cc} | V _{cc} |

BLOCK DIAGRAM**PIN DESCRIPTIONS****CLK_IN, /CLK_IN – CML Input (Differential)**

This is one of the differential CML inputs, the clock in signal. A delayed version of this input appears at CLK_OUT, /CLK_OUT.

CINV – VT Input (Single Ended)

This is the clock inversion select signal. This input optionally inverts the CLK_IN, /CLK_IN signal which results in an inverted CLK_OUT, /CLK_OUT. A voltage below the VT threshold results in no inversion. A voltage above the threshold value results in an inversion from the clock input to the clock output. Refer to the “VT input” section below.

CLK_OUT, /CLK_OUT – CML Output (Differential)

This is one of the CML outputs, the clock output. It is a delayed, copy of CLK_IN, /CLK_IN.

DATA_IN, /DATA_IN – CML Input (Differential)

This is one of the CML inputs, the data in signal. A delayed version of this signal appears at DATA_OUT, /DATA_OUT.

DATA_OUT, /DATA_OUT – CML Output (Differential)

This is one of the CML outputs, the data output. It is a delayed version of CLK_IN, /CLK_IN.

LVL – Analog Input

This input determines what level differentiates logic high from logic low. This input affects the behavior of the CINV, S0, S1 and S2 inputs. Please refer to the “VT input” section below for more details. For the control interface, see Figure 3b. For TTL control interface, see Figure 3b.

DELAY_SEL – VT Input (Single Ended)

CML compatible control logic. This is the delay path control input. Logic high delays the clock signal with respect to the data signal. A logic low delays the data signal with respect to the clock signal. Inputs S2, S1 and S0 control amount of delay.

S0, S1, S2 – VT Input (Single Ended)

CML compatible control logic. This is the delay selection control input. These three bits define how much relative delay will occur between the data and clock signals, as per the truth table shown in Table 2. For the control logic interface, see Figure 3b. For TTL control interface, see Figure 3b. S0=LSB.

FUNCTIONAL DESCRIPTION

Establishing Static Logic Inputs

The true pin of a CML input pair is internally biased to ground through a 75kΩ resistor. The complement pin of a CML input pair is internally biased halfway between V_{CC} and ground by a voltage divider consisting of two 75kΩ resistors. To keep a CML input at static logic zero at $V_{CC} > 3.0V$, leave both inputs unconnected. For $V_{CC} \leq 3.0V$, connect the complement input to V_{CC} and leave the true input unconnected. To make an input static logic one, connect the true input to V_{CC} , and leave the complement input unconnected. These are the only safe ways to cause CML inputs to be at a static value. In particular, no CML input should be directly connected to ground. All NC pins in the figures below should be left unconnected.

VT (Variable Threshold) Inputs

Five inputs to SY55856U, CINV, DELAY_SEL, S0, S1, and S2, are variable threshold inputs. The LVL input determines

the Voltage threshold that differentiates logic high from logic low for these five inputs only. If LVL is left unconnected, the

VT inputs will switch at about $\frac{V_{CC} + GND}{2}$ or V_{TCL} , whichever is higher. To obtain a logic switching threshold different from this, the LVL input must be driven with the actual desired threshold voltage. The user may drive the LVL pin with any voltage between $V_{CC} - 0.1V$ and ground. For example, driving LVL with a voltage set at $V_{CC} - 1.3V$ causes the VT inputs to accept single ended PECL outputs and switch appropriately.

Note that VT inputs are internally clamped so that the threshold will not fall below VTCL Volts. Since driving the LVL input to ground causes the threshold to be somewhere between V_{TCL} (min) and V_{TCL} (max), it is expected that the user will keep the Voltage at the LVL pin at or above V_{TCL} (max). Please refer to Figure 3 for clarification.

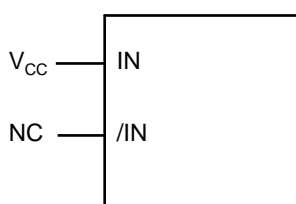


Figure 1. Hard Wiring a Logic "1"(1)

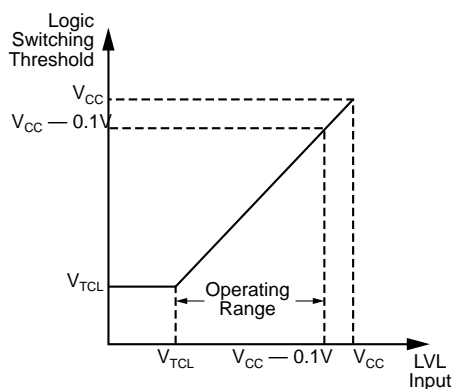


Figure 3a. Logic Switching Threshold

Note 1. IN is either the DATA_IN or the CLK_IN input. /IN is either the /DATA_IN or the /CLK_IN input.

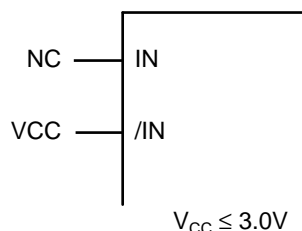
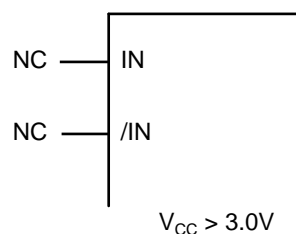


Figure 2. Hard Wiring a Logic "0"(1)

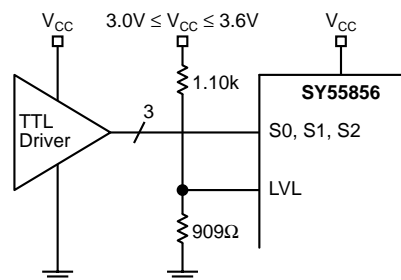


Figure 3b. Interfacing TTL-to-CML Select (CINV, DELAY_SEL, S0, S1, S2)

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Rating | Value | Unit |
|---------------|--|----------------------|--------------|
| V_{CC} | Power Supply Voltage | -0.5 to +6.0 | V |
| V_{IN} | Input Voltage | -0.5 to $V_{CC}+5.0$ | V |
| V_{OUT} | CML Output Voltage | -0.5 to $V_{CC}+5.0$ | V |
| T_A | Operating Temperature Range | -40 to +85 | °C |
| T_{store} | Storage Temperature Range | -55 to +125 | °C |
| θ_{JA} | Package Thermal Resistance (Junction-to-Ambient) Exposed pad soldered to PCB GND pin | 28 20 | °C/W °C/W |
| θ_{JC} | Package Thermal Resistance (Junction-to-Case) | 4 | °C/W |

Note 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

CML TERMINATION

All CML inputs accept a CML output from any other member of this family. All CML outputs are source terminated 50Ω differential drivers as shown in Figure 4. SY55856U expects its inputs to be externally terminated.

SY55856U inputs are designed to accept a termination resistor between the true and complement inputs of a CML differential input pair, as shown in Figure 4.

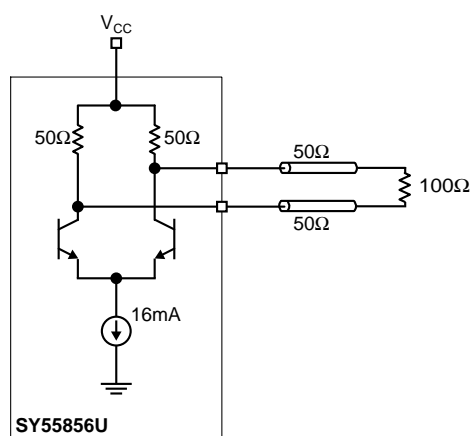


Figure 4. 50Ω Load CML Output

TRUTH TABLES

| DATA_IN | CLK_IN | CINV | DATA_OUT | /DATA_OUT | CLK_OUT | /CLK_OUT |
|---------|--------|------|----------|-----------|---------|----------|
| 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 |

Table 1. Input to Output Connectivity

| S2 | S1 | S0 | DATA_OUT (D_SEL=0) (ps) | CLK_OUT (D_SEL=1) (ps) | (CLK_OUT-CLK_IN) – (DATA_OUT-DATA_IN) (ps) |
|----|----|----|----------------------------|---------------------------|---|
| 0 | 0 | 0 | 350 | 0 | -350 |
| 0 | 0 | 1 | 300 | 50 | -250 |
| 0 | 1 | 0 | 250 | 100 | -150 |
| 0 | 1 | 1 | 200 | 150 | -50 |
| 1 | 0 | 0 | 150 | 200 | 50 |
| 1 | 0 | 1 | 100 | 250 | 150 |
| 1 | 1 | 0 | 50 | 300 | 250 |
| 1 | 1 | 1 | 0 | 350 | 350 |

Table 2. Nominal Differential Delay Values

- Note 1.** Table 2 defines the approximate relative delay between the two paths. For example, if S2, S1, S0 = 000, and an edge appears at CLK_IN at the same instant as an edge appears at DATA_IN, then an edge at CLK_OUT will appear about 350ps earlier than an edge at DATA_OUT. That is, negative values imply CLK_OUT being shifted early with respect to DATA_OUT. Likewise, a positive value in the third column implies that CLK_OUT is shifted late with respect to DATA_OUT. Please consult the “AC ELECTRICAL CHARACTERISTICS” section for more precise delay values.
- Note 2.** As another example, if an edge at CLK_IN appears 100ps before an edge at DATA_IN, and if S2, S1, S0 = 100, then an edge at CLK_OUT will appear about 50ps after an edge at DATA_OUT. This setting of the select inputs shifts CLK_IN to CLK_OUT about 150ps later than DATA_IN to DATA_OUT, moving the timing of the “C” side from 100ps early to 50ps late, as compared with the “D” channel, going through the part.

DC ELECTRICAL CHARACTERISTICS⁽¹⁾

| Symbol | Parameter | T _A = -40°C | | | T _A = +25°C | | | T _A = +85°C | | | Unit | Condition |
|-----------------|----------------------|------------------------|------|------|------------------------|------|------|------------------------|------|------|------|-----------|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| V _{CC} | Power Supply Voltage | 2.3 | — | 3.6 | 2.3 | — | 3.6 | 2.3 | — | 3.6 | V | |
| I _{CC} | Power Supply Current | — | — | 140 | — | 115 | 140 | — | — | 140 | mA | No Load |

Note 1. Specification for packaged product only.

VT INPUTS DC ELECTRICAL CHARACTERISTICS⁽¹⁾

V_{CC} = 2.3V to 3.6V; GND = 0V; T_A = -40°C to +85°C⁽²⁾

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|-------------------|---|-----------------------|------|-----------------------|------|
| V _{ILVL} | Analog Input ⁽³⁾ | V _{TCL} | — | V _{CC} - 0.1 | V |
| V _{IHVT} | V _T Input High Voltage ^(4,5) | V _{SW} + 0.1 | — | V _{CC} | V |
| V _{ILVT} | V _T Input High Voltage ^(4,5) | 0.0 | — | V _{SW} - 0.1 | V |
| V _{IST} | Input Switching Threshold Differential Voltage ⁽⁶⁾ | 100 | 50 | — | mV |
| V _{TCL} | Threshold Clamp Voltage | 1.2 | — | 1.4 | V |

Note 1. Specification for packaged product only.

Note 2. DC parameters are guaranteed after thermal equilibrium has been established.

Note 3. The LVL input determines the voltage switching threshold that differentiates logic high from logic low for the V_T inputs S0, S1, S2, S2, and CINV. LVL may be driven to V_{CC}, but this is not useful, as the V_T inputs could then not get high enough to reliably indicate logic high. Also, as shown in Figure 3, the LVL input internally clamps at V_{TCL}. If LVL is left unconnected, the V_T inputs will switch at about the maximum of

$$\frac{V_{CC} + GND}{2} \left(= \frac{V_{CC}}{2} \right) \text{ and } V_{TCL}.$$

Note 4. V_T inputs are S0, S1, S2, S3, and CINV.

Note 5. V_{SW} is the threshold switching voltage. It is equal to the voltage at the LVL pin, when this voltage is above V_{TCL} (max). V_{SW} is some value between V_{TCL} (min) and V_{TCL} (max) when the Voltage at the LVL pin is below V_{TCL} (max).

Note 6. V_{IST} is the voltage difference needed to guarantee a stable logic level. Logic high must be at least V_{IST} above V_{SW}. Logic low must be at most V_{IST} below V_{SW}. Thus, the minimum input swing on a given V_T input pin, that is, |V_{IHVT} - V_{ILVT}|, must be at least 2×V_{IST}.

CML DC ELECTRICAL CHARACTERISTICS^(1, 2)

V_{CC} = 2.3V to 3.6V; GND = 0V; T_A = -40°C to +85°C

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Condition |
|-----------------------------|---|-------------------------|-------------------------|------------------------|------|-----------------|
| V _{ID} | Differential Input Voltage | 100 | — | — | mV | |
| V _{IH} | Input HIGH Voltage | 1.6 | — | V _{CC} | V | |
| V _{IL} | Input LOW Voltage | 1.5 | — | V _{CC} - 0.1 | V | |
| V _{OH} | Output HIGH Voltage | V _{CC} - 0.040 | V _{CC} - 0.010 | V _{CC} | V | No Load |
| V _{OL} | Output LOW Voltage | V _{CC} - 1.00 | V _{CC} - 0.800 | V _{CC} - 0.65 | V | No Load |
| V _{OUT} (Swing) | Output Voltage Swing ⁽³⁾ | 0.650 | 0.800 | 1.00 | V | No Load |
| | | — | 0.400 | — | | 50Ω Environment |
| R _{OUT} | Output Source Impedance (CLK_OUT, /CLK_OUT and DATA_OUT, /DATA_OUT) | 40 | 50 | 60 | Ω | |

Note 1. Specification for packaged product only.

Note 2. DC parameters are guaranteed after thermal equilibrium has been established.

Note 3. V_{OUT(SWING)} is defined as the swing on one output of a differential pair, that is |V_{OH} - V_{OL}| on one pin. The swing for common mode noise immunity purposes is 2 × V_{OUT(SWING)}. Actual voltage levels and differential swing will depend on customer termination scheme. Typically, a 400mV swing is available in a 50Ω environment. Refer to "CML Termination" figures for more details.

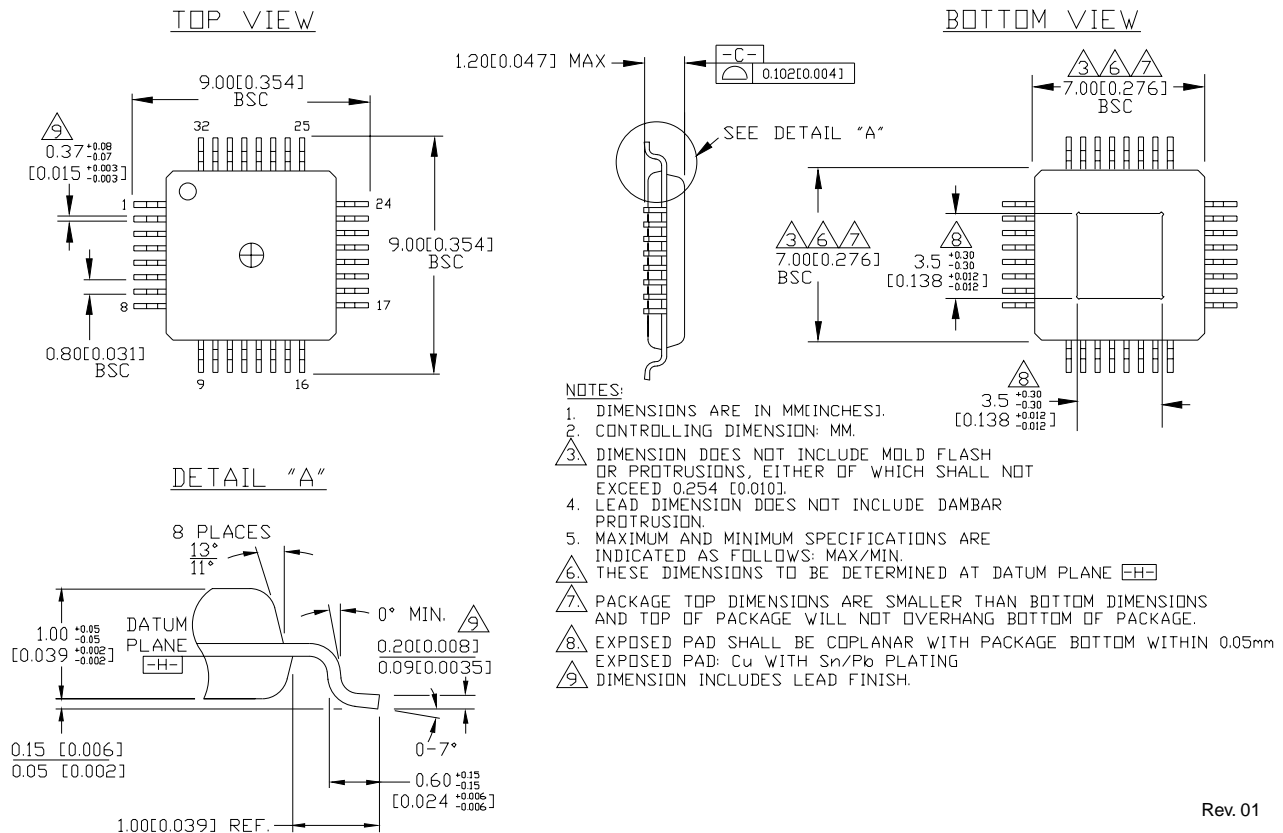
AC ELECTRICAL CHARACTERISTICS^(1, 2) $V_{CC} = 2.3V$ to $3.6V$; $GND = 0V$

| Symbol | Parameter | $T_A = -40^{\circ}C$ | | $T_A = +25^{\circ}C$ | | $T_A = +85^{\circ}C$ | | Unit |
|------------------------|--|----------------------|------|----------------------|------|----------------------|------|---------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| f_{MAX} | Maximum Frequency | 2.5 | — | 2.5 | — | 2.5 | — | GHz |
| Δt | Delay step size | 36 | 52 | 36 | 52 | 36 | 52 | ps |
| t_{PLH} t_{PHL} | Delay line insertion delay ⁽³⁾ | 232 | 384 | 232 | 384 | 232 | 384 | ps |
| t_{DELAY} | Delay line range | 250 | 365 | 290 | 420 | 335 | 465 | ps |
| t_{JITTER} | Output jitter | — | <1 | — | <1 | — | <1 | ps(rms) |
| t_{SKEW} | Delay line duty cycle skew ($ t_{PLH} - t_{PHL} $) | — | 50 | — | 50 | — | 50 | ps |
| DC | Duty cycle | 45 | 55 | 45 | 55 | 45 | 55 | % |
| t_r/t_f | CML Output rise/fall time (20% to 80%) | — | 100 | — | 110 | — | 120 | ps |

Note 1. Specification for packaged product only.**Note 2.** Tested using the 50W load, as shown in Figure 4.**Note 3.** Delay line insertion delay is the minimum input-to-output delay with select control set to S2:S0 = 0 for CLK_OUT and S2:S0 = 7 for DATA_OUT. This resulting delay is the inherent propagation delay.**PRODUCT ORDERING CODE**

| Ordering Code | Package Type | Operating Range | Package Marking |
|---------------|--------------|-----------------|-----------------|
| SY55856UHI | H32-1 | Industrial | SY55856UHI |
| SY55856UHITR* | H32-1 | Industrial | SY55856UHI |

*Tape and Reel

32 LEAD EPAD-TQFP (DIE UP) (H32-1)

Rev. 01

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