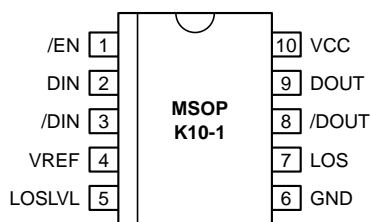


FEATURES

- 3.3V and 5V power supply options
- Up to 2.5Gbps operation
- Low noise
- Chatter-Free LOS Generation
- Open Collector TTL LOS Output
- TTL /EN Input
- Differential PECL inputs for data
- Single power supply
- Designed for use with (Micrel-Synergy laser diode driver and controller)
- Available in a tiny 10-pin (3mm) MSOP

PIN CONFIGURATION



DESCRIPTION

The SY88923V limiting post amplifier with its high gain and wide bandwidth is ideal for use as a post amplifier in fiber-optic receivers with data rates up to 2.5Gbps. Signals as small as 5mVp-p can be amplified to drive devices with PECL inputs. The SY88923V generates a chatter-free Loss of Signal (LOS) open collector TTL output.

The SY88923V incorporates a programmable level detect function to identify when the input signal has been lost. The LOS output will change from logic "LOW" to logic "HIGH" when input signal is smaller than the swing set by LOS_{LVL} . This information can be fed back to the EN input of the device to maintain stability under loss of signal condition. Using LOS_{LVL} pin, the sensitivity of the level detection can be adjusted. The LOS_{LVL} voltage can be set by connecting a resistor divider between V_{CC} and V_{REF} as shown in Figure 3. Figure 4, 5, 6, and 7 show the relationship between input level sensitivity and the voltage set on LOS_{LVL} .

The LOS output is a TTL open collector output that requires a pull-up resistor for proper operation, Figure 1.

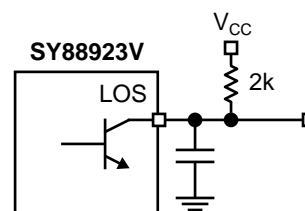
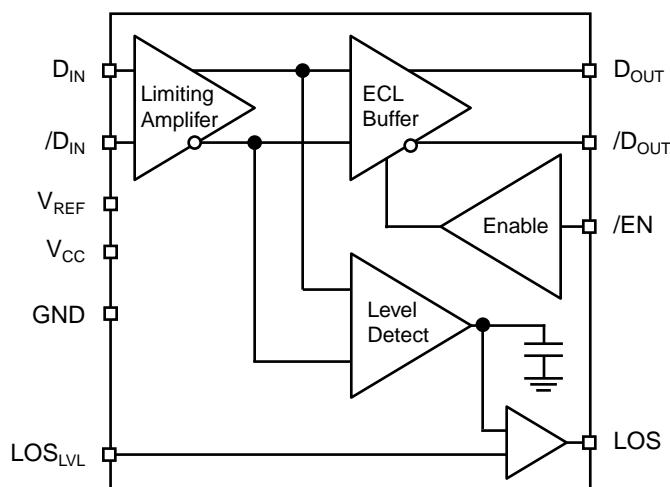


Figure 1. LOS Output with Desired Rise Time

APPLICATIONS

- 1.25Gbps and 2.5Gbps Gigabit Ethernet
- 531Mbps, 1062Mbps and 2.12Gbps Fibre Channel
- 622Mbps SONET
- Gigabit Interface Converter
- 2.5Gbps SDH/SONET
- 2.5Gbps Proprietary Links

BLOCK DIAGRAM



PIN NAMES

Pin	Type	Function
D _{IN}	Data Input	Data Input
/D _{IN}	Data Input	Inverting Data Input
LOS _{LVL}	Input	LOS Limit Set
/EN	TTL Input	Output Enable (Active Low)
LOS	TTL Output (Open Collector)	Loss of Signal Indicator (Active High)
GND	Ground	Ground
/D _{OUT}	PECL Output	Inverting Data Output
D _{OUT}	PECL Output	Data Output
V _{CC}	Power Supply	Positive Power Supply
V _{REF}	Output	Reference Voltage Output for LOS Level Set (see Fig. 3)

GENERAL DESCRIPTION**General**

The SY88923V is an integrated limiting amplifier intended for high-frequency fiber-optic applications. The circuit connects to typical trans-impedance amplifiers found within a fiber-optics link. The linear signal output from a trans-impedance amplifier can contain significant amounts of noise, and may vary in amplitude over time. The SY88923V limiting amplifier quantizes the signal and outputs a voltage-limited waveform.

The /EN pin allows the user to disable the output signal without removing the input signal.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Value	Unit
V _{CC}	Power Supply Voltage	0 to +7.0	V
D _{IN} , /D _{IN}	Input Voltage	0 to V _{CC}	V
D _{OUT} , /D _{OUT}	Output Voltage (with 50Ω load)	V _{CC} -2.5 to V _{CC} +0.3	V
/EN	Input Voltage	0 to V _{CC}	V
LOS _{LVL}	Input Voltage	0 to V _{CC}	V
V _{REF}	Output Voltage	V _{CC} -2.0 to V _{CC}	V
T _A	Operating Temperature Range	-40 to +85	°C
T _{store}	Storage Temperature Range	-55 to +125	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS
 $V_{CC} = +5V \pm 10\%$ or $+3.3V \pm 10\%$, $R_{LOAD} = 50\Omega$ to $V_{CC} - 2V$

Symbol	Parameter	$T_A = -40^\circ C$		$T_A = 0^\circ C$		$T_A = +25^\circ C$			$T_A = +85^\circ C$		Unit
		Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_{CC}	Power Supply Current ⁽¹⁾ 5V 3.3V	—	40	—	40	—	30	40	—	45	mA
I_{IL}	/EN Input LOW Current	-0.3 ⁽⁶⁾	—	-0.3 ⁽⁶⁾	—	-0.3 ⁽⁶⁾	—	—	-0.3 ⁽⁶⁾	—	mA
I_{IH}	/EN Input HIGH Current	—	20 ⁽⁴⁾ 100 ⁽⁵⁾	—	20 ⁽⁴⁾ 100 ⁽⁵⁾	—	—	20 ⁽⁴⁾ 100 ⁽⁵⁾	—	20 ⁽⁴⁾ 100 ⁽⁵⁾	μA
V_{CMR}	Common Mode Range	GND +2.0	V_{CC}	GND +2.0	V_{CC}	GND +2.0	—	V_{CC}	GND +2.0	V_{CC}	V
V_{offset}	Differential Output Offset	—	± 100	—	± 100	—	± 17	± 100	—	± 100	mV
LOS_{LVL}	LOS_{LVL} Level	V_{REF}	V_{CC}	V_{REF}	V_{CC}	V_{REF}	—	V_{CC}	V_{REF}	V_{CC}	V
V_{OL}	LOS Output Low Level ⁽²⁾	—	0.5	—	0.5	—	—	0.5	—	0.5	V
I_{OH}	LOS Output Leakage ⁽³⁾	—	100	—	100	—	—	100	—	100	μA
V_{OH}	D_{OUT} and $/D_{OUT}$ HIGH Output	$V_{CC} - 1085$	$V_{CC} - 880$	$V_{CC} - 1025$	$V_{CC} - 880$	$V_{CC} - 1025$	$V_{CC} - 955$	$V_{CC} - 880$	$V_{CC} - 1025$	$V_{CC} - 880$	mV
V_{OL}	D_{OUT} and $/D_{OUT}$ LOW Output	$V_{CC} - 1830$	$V_{CC} - 1555$	$V_{CC} - 1810$	$V_{CC} - 1620$	$V_{CC} - 1810$	$V_{CC} - 1705$	$V_{CC} - 1620$	$V_{CC} - 1810$	$V_{CC} - 1620$	mV
V_{REF}	Reference Supply	$V_{CC} - 1.38$	$V_{CC} - 1.26$	$V_{CC} - 1.38$	$V_{CC} - 1.26$	$V_{CC} - 1.38$	$V_{CC} - 1.32$	$V_{CC} - 1.26$	$V_{CC} - 1.38$	$V_{CC} - 1.26$	V
I_{REF}	V_{REF} Output Current	-0.8	0.5	-0.8	0.5	-0.8	—	0.5	-0.8	0.5	mA
V_{IH}	/EN Input HIGH Voltage	2.0	—	2.0	—	2.0	—	—	2.0	—	V
V_{IL}	/EN Input LOW Voltage	—	0.8	—	0.8	—	—	0.8	—	0.8	V

NOTES:

1. No output load
2. $I_{OL} = +2mA$
3. $V_{OH} = 5.5V$

4. $V_{IN} = 2.7V$ 5. $V_{IN} = V_{CC}$ 6. $V_{IN} = 0.5V$ **AC ELECTRICAL CHARACTERISTICS**
 $V_{CC} = +5V \pm 10\%$ or $+3.3V \pm 10\%$, $R_{LOAD} = 50\Omega$ to $V_{CC} - 2V$

Symbol	Parameter	$T_A = -40^\circ C$		$T_A = 0^\circ C$		$T_A = +25^\circ C$			$T_A = +85^\circ C$		Unit	Conditions
		Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
PSRR	Power Supply ⁽¹⁾ Rejection Ratio	—	—	—	—	—	35	—	—	—	dB	Input referred, 55MHz
V_{ID}	Input Voltage Range	5	1800	5	1800	5	—	1800	5	1800	mVp-p	
V_{OD}	Differential Output Voltage Swing ⁽²⁾	—	—	—	—	—	700 300	—	—	—	mV mV	$V_{ID} = 15mVp-p$ $V_{ID} = 5mVp-p$
t_{OFFL}	LOS Release Time ⁽³⁾ Minimum Input	—	0.5	—	0.5	—	0.1	0.5	—	0.5	μs	
t_{ONL}	LOS Assert Time ⁽³⁾	—	0.5	—	0.5	—	0.2	0.5	—	0.5	μs	
t_{OFFH}	LOS Release Time ⁽⁴⁾ Maximum Input	—	0.5	—	0.5	—	0.1	0.5	—	0.5	μs	
V_{SR}	LOS Sensitivity Range	5	50	5	50	5	—	50	5	50	mVp-p	2 ²³ -1 pattern
HYS	LOS Hysteresis	2	8	2	8	2	4.6	8	2	8	dB	2 ²³ -1 pattern
t_r, t_f	Output Rise/Fall Time	—	175	—	175	—	150 t_{rin}, t_{fin}	175	—	175	ps	$V_{ID} > 100mVp-p$ $V_{ID} < 100mVp-p$

NOTES:

1. Input referred noise = RMS output noise/low frequency gain.
2. Input is a 622MHz square wave.

3. Input is a 200MHz square wave, $t_r < 300ps$, 8mVp-p.4. Input is a 200MHz square wave, $t_r < 300ps$, 1.8Vp-p.

DESIGN PROCEDURE

Output Termination

The SY88923V outputs must be terminated with a 50Ω load to V_{CC} – 2V (or Thevenin equivalent).

Layout and PCB Design

Since the SY88923V is a high-frequency component, performance can largely be determined by board layout and design. A common problem with high-gain amplifiers is feedback from the large swing outputs to the input via the power supply.

The SY88923V ground pin should be connected to the circuit board ground. Use multiple PCB vias close to the part to connect to ground. Avoid long, inductive runs which can degrade performance.

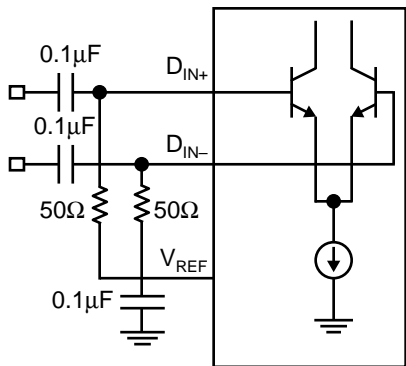


Figure 2. Differential Input Configuration

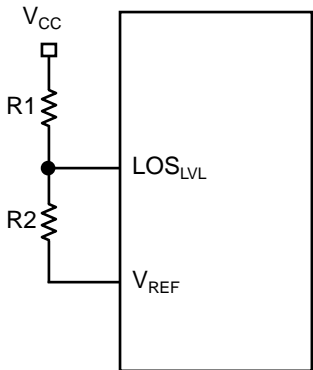


Figure 3. LOS_{LVL} Circuit

NOTES:
$$\text{LOS}_{\text{LVL}} = V_{\text{CC}} - 1.32\text{V} + \frac{R2 \times 1.32\text{V}}{R1 + R2}$$

$$R1 + R2 \geq 2.6\text{k}\Omega$$

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY88923VKC	K10-1	Commercial
SY88923VKCTR	K10-1	Commercial

PERFORMANCE CURVE

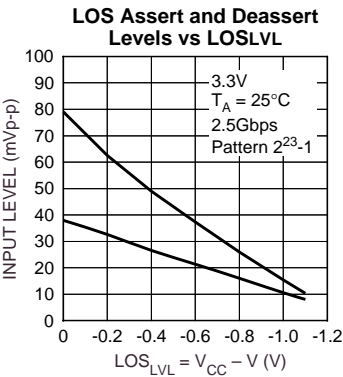


Figure 4.

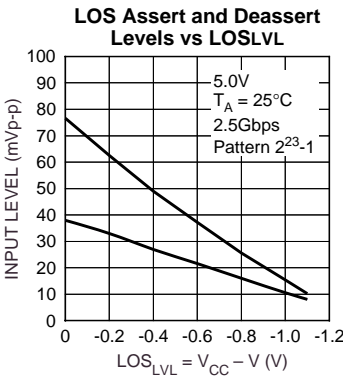


Figure 5.

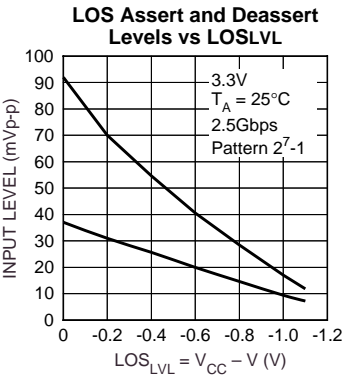


Figure 6.

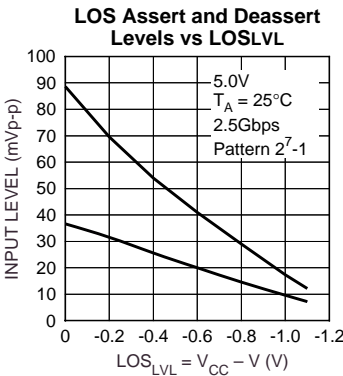
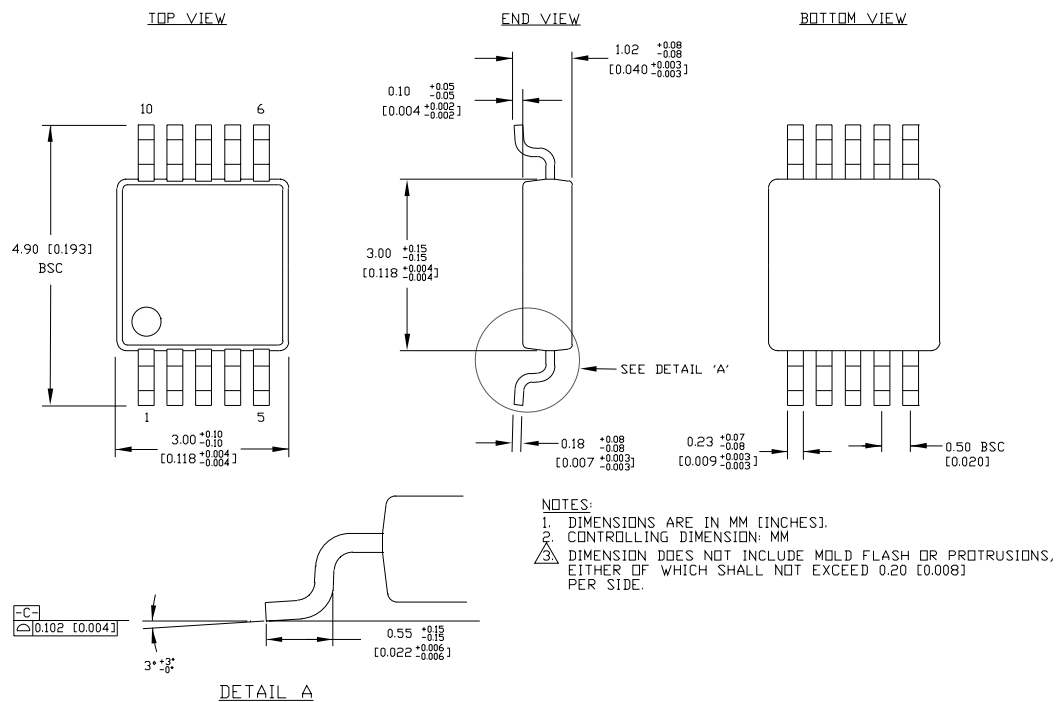


Figure 7.

10 LEAD MSOP (K10-1)



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